DATA HANDBOOK

I²C-bus compatible ICs
Types MAB84X1 family to PCF8579

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Philips Components

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I²C-BUS COMPATIBLE ICs

Part a

page

Selection guide
- Functional index 5
- Numerical index 9
- Associated publications 17

General
- Type designation 21
- Rating systems 23
- Handling MOS devices 25
- I²C-bus Specification 27
- I²C-bus Evaluation Board 57

Device data
- MAB84X1 family to PCF8579 61

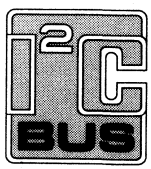
Part b

page

Selection guide
- Functional index 693
- Numerical index 697

Device data
- Types PCF8582A to UMA1010T 707

Package information
- Package outlines 1355
- Soldering 1383



SELECTION GUIDE

Functional index

Numerical index

Associated publications

FUNCTIONAL INDEX

type number	description	page
68000-based CMOS microprocessor		
SCC68070	68000 CPU/MMU/UART/DMA/timer	989
80C51-set based CMOS microcontrollers*		
PCB80C552	ROM-less version of PCB83C552	113
PCB80C652	ROM-less version of PCB83C652	163
PCB83C552	256-byte RAM/8 K ROM/ADC/UART	113
PCB83C652	256-byte RAM/8 K ROM	163
PCB83C654	256-byte RAM/16 K ROM	201
8048 instruction-set based CMOS microcontrollers		
PCF84C00	256-byte RAM/bond-out version for prototype development	375
PCF84C21	64-byte RAM/2 K ROM	375
PCF84C41	128-byte RAM/4 K ROM	375
PCF84C81	256-byte RAM/8 K ROM	375
PCF84C85	256-byte RAM/8 K ROM/extended I/O	401
PCF84C430	128-byte RAM/4 K ROM/96-segment LCD driver	441
8048 instruction-set based NMOS microcontrollers*		
MAB8401B	128-byte RAM/piggy-back version for prototype development	61
MAB8411	64-byte RAM/1 K ROM	61
MAB8421	64-byte RAM/2 K ROM	61
MAB8422	MAB8421 with reduced I/O; software I^2C	93
MAB8441	128-byte RAM/4 K ROM	61
MAB8442	MAB8421 with reduced I/O; software I^2C	93
MAB8461	128-byte RAM/6 K ROM	61

* Also available with extended and automotive temperature ranges.

type number	description	page
GENERAL-PURPOSE ICs		
LCD drivers		
PCF8566	96-segment LCD driver; 1:1 – 1:4 MUX	497
PCF8576	160-segment LCD driver; 1:4 – 1:4 MUX	567
PCF8577/A	64-segment LCD driver; 1:1 – 1:2 MUX	601
PCF8578	row/column LCD dot-matrix driver; 1:8 – 1:32	617
PCF8579	row/column LCD dot-matrix driver; 1:8 – 1:32	655
I/O expandors		
PCF8574/A	8-bit remote I/O port (I^2C-bus to parallel converter)	555
SAA1064	4-digit LED driver	753
SAA1300	5-bit high-current driver	763
Data converters		
PCF8591	4-channel, 8-bit MUX ADC + one DAC	735
TDA8442	quad 6-bit DAC	1155
TDA8444	octal 6-bit DAC	1177
Memory		
PCF8570	256-byte static RAM	527
PCF8570C	256-byte static RAM with alternative slave address	527
PCF8571	126-byte static RAM	527
PCF8582A	256-byte EEPROM	707
Clock/calendars		
PCF8573	clock/calendar	537
PCF8583	256-byte RAM/clock/calendar	717

type number	description	page
APPLICATION-ORIENTED ICs		
Video/radio/audio		
PCF8200	Voice synthesizer (male/female speech)	335
SAA1300	tuner switching circuit	763
SAA3028	transcoder (RC-5) for IR remote control	767
SAA4700	dataline processor for VPS	775
SAA5243	Enhanced Computer Controlled Teletext (ECCT) decoder	787
SAA5245	Enhanced Computer Controlled Teletext (USECCT) decoder	817
SAA9041	digital video teletext (DVTB) processor	839
SAA9050	digital PAL/NTSC colour decoder	859
SAA9055	digital SECAM decoder	891
SAA9068	picture-in-picture controller	913
SAB3035	digital tuning circuit for computer-controlled TV	929
SAB3036	digital tuning circuit for computer-controlled TV	945
SAB3037	digital tuning circuit for computer-controlled TV	961
SAF1135	dataline 16 decoder for VCR	977
TDA8370	synchronization processor for TV	1051
TDA8405	stereo/dual sound processor	1069
TDA8420	audio processor with a loudspeaker channel and a headphone channel	1079
TDA8421	audio processor with a loudspeaker channel and a headphone channel	1101
TDA8425	audio processor with a loudspeaker channel only	1123
TDA8440	video/audio switch	1145
TDA8442	interface for colour decoders	1155
TDA8443A	YUV/RGB matrix switch	1163
TDA8461	PAL/NTSC colour decoder and RGB processor	1185
TEA6000	FM/IF and digital tuning IC for computer-controlled radio	1209
TEA6100	FM/IF and digital tuning IC for computer-controlled radio	1221
TEA6300/T	sound fader control and preamplifier/source selector for car radio	1245
TEA6310T	sound fader control with tone and volume control for car radio	1261
TSA5510	PLL frequency synthesizer for TV and VCR	1279
TSA5510T	PLL frequency synthesizer for TV and VCR	1289
TSA6057/T	PLL frequency synthesizer for radio	1299

type number	description	page
APPLICATION-ORIENTED ICs		
Telecom		
PCD3311A	tone generator (DTMF)	239
PCD3311/3312	tone generator (DTMF/modem/music)	255
PCD3315C	microcontroller with 160-byte RAM/1.5 K ROM	273
PCD3341	advanced 10/110-number repertory pulse/DTMF dialler with LCD control	277
PCD3343	microcontroller with 224-byte RAM/3 K ROM	295
UMA1000T	data processor (DPROC) for mobile telephones	1309
UMA1010T	frequency synthesizer (0.45 to 1.1 GHz) for mobile telephones	1339

NUMERICAL INDEX

type no.	description	page
MAB8401B	microcontroller; 128 x 8 RAM; piggy-back version for MAB84XX family plus 8-bit LED driver; I²C-bus; 1.0 to 6 MHz; 0 to + 70 °C	61
MAB8401WP	microcontroller; 128 x 8 RAM; piggy-back version for MAB84XX family plus 8-bit LED driver; I²C-bus; 1.0 to 6 MHz; 0 to + 70 °C	61
MAB8411P	microcontroller; 64 x 8 RAM; 1 K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; 0 to + 70 °C	61
MAB8411T	microcontroller; 64 x 8 RAM; 1 K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; 0 to + 70 °C	61
MAB8421P	microcontroller; 64 x 8 RAM; 2 K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; 0 to + 70 °C	61
MAB8421T	microcontroller; 64 x 8 RAM; 2 K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; 0 to + 70 °C	61
MAB8422P	microcontroller; 64 x 8 RAM; 2 K x 8 ROM plus 8-bit LED driver; 15 I/O lines; I²C-bus; 1.0 to 6 MHz; 0 to + 70 °C	93
MAB8441P	microcontroller; 128 x 8 RAM; 4 K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; 0 to + 70 °C	61
MAB8441T	microcontroller; 128 x 8 RAM; 4 K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; 0 to + 70 °C	61
MAB8442P	microcontroller; 128 x 8 RAM; 4 K x 8 ROM plus 8-bit LED driver; 15 I/O lines; I²C-bus; 1.0 to 6 MHz; 0 to + 70 °C	93
MAB8461P	microcontroller; 128 x 8 RAM; 6 K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; 0 to + 70 °C	61
MAB8461T	microcontroller; 128 x 8 RAM; 6 K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; 0 to + 70 °C	61
MAF84A11P	microcontroller; 64 x 8 RAM; 1 K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 5.0 MHz; −40 to + 110 °C	61
MAF84A21P	microcontroller; 64 x 8 RAM; 2 K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 5.0 MHz; −40 to + 110 °C	61
MAF84A22P	microcontroller; 64 x 8 RAM; 2 K x 8 ROM plus 8-bit LED driver; 15 I/O lines; I²C-bus; 1.0 to 5.0 MHz; −40 to + 110 °C	93
MAF84A41P	microcontroller; 128 x 8 RAM; 4 K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 5.0 MHz; −40 to + 110 °C	61
MAF84A42P	microcontroller; 128 x 8 RAM; 4 K x 8 ROM plus 8-bit LED driver; 15 I/O lines; I²C-bus; 1.0 to 5.0 MHz; −40 to + 110 °C	93

type no.	description	page
MAF84A61P	microcontroller; 128 x 8 RAM; 6 K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 5.0 MHz; −40 to + 110 °C	61
MAF8411P	microcontroller; 64 x 8 RAM; 1 K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; −40 to + 85 °C	61
MAF8421P	microcontroller; 64 x 8 RAM; 2 K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; −40 to + 85 °C	61
MAF8422P	microcontroller; 64 x 8 RAM; 2 K x 8 ROM plus 8-bit LED driver; 15 I/O lines; I²C-bus; 1.0 to 6 MHz; −40 to + 85 °C	93
MAF8441P	microcontroller; 128 x 8 RAM; 4 K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; −40 to + 85 °C	61
MAF8442P	microcontroller; 128 x 8 RAM; 4 K x 8 ROM plus 8-bit LED driver; 15 I/O lines; I²C-bus; 1.0 to 6 MHz; −40 to + 85 °C	93
MAF8461P	microcontroller; 128 x 8 RAM; 6 K x 8 ROM plus 8-bit LED driver; 20 I/O lines; I²C-bus; 1.0 to 6 MHz; −40 to + 85 °C	61
PCA83C652P	microcontroller; 256 x 8 RAM; 8 K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; −40 to + 125 °C	163
PCA83C652WP	microcontroller; 256 x 8 RAM; 8 K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; −40 to + 125 °C	163
PCB80C552WP	microcontroller; 256 x 8 RAM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; two pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I²C-bus; 1.2 to 12 MHz; 0 to + 70 °C	113
PCB80C652P	microcontroller; 256 x 8 RAM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; 0 to + 70 °C	163
PCB80C652WP	microcontroller; 256 x 8 RAM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; 0 to + 70 °C	163
PCB83C552WP	microcontroller; 256 x 8 RAM; 8 K x 8 ROM; 80C31 CPU plus 16-bit capture/compare timer/counter; watch-dog timer; two pulse-width modulated signals; 10-bit ADC with 8 multiplexed input lines; I²C-bus; 1.2 to 12 MHz; 0 to + 70 °C	113
PCB83C652P	microcontroller; 256 x 8 RAM; 8 K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; 0 to + 70 °C	163
PCB83C652WP	microcontroller; 256 x 8 RAM; 8 K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; 0 to + 70 °C	163
PCB83C654P	microcontroller; 256 x 8 RAM; 16 K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; 0 to + 70 °C	201
PCB83C654WP	microcontroller; 256 x 8 RAM; 16 K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; 0 to + 70 °C	201
PCD3311AT	DTMF/32-single tone generator with parallel data inputs; I²C-bus	239
PCD3311P	DTMF generator with parallel data inputs; I²C-bus	255
PCD3311T	DTMF generator with parallel data inputs; I²C-bus	255
PCD3312P	DTMF generator; I²C-bus	255
PCD3312T	DTMF generator; I²C-bus	255

type no.	description	page
PCD3315CP	microcontroller for telephone sets; 160 x 8 RAM; 1.5 K x 8 ROM; 20 I/O lines; I²C-bus	273
PCD3315CT	microcontroller for telephone sets; 160 x 8 RAM; 1.5 K x 8 ROM; 20 I/O lines; I²C-bus	273
PCD3341P	advanced 10-100 number repertory pulse/DTMF dialler; LCD control; I²C-bus	277
PCD3341T	advanced 10-100 number repertory pulse/DTMF dialler; LCD control; I²C-bus	277
PCD3343D	microcontroller for telephone sets; 224 x 8 RAM; 3 K x 8 ROM; 20 I/O lines; I²C-bus	295
PCD3343P	microcontroller for telephone sets; 224 x 8 RAM; 3 K x 8 ROM; 20 I/O lines; I²C-bus	295
PCD3343T	microcontroller for telephone sets; 224 x 8 RAM; 3 K x 8 ROM; 20 I/O lines; I²C-bus	295
PCF80C652P	microcontroller; 256 x 8 RAM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; −40 to + 85 °C	163
PCF80C652WP	microcontroller; 256 x 8 RAM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; −40 to + 85 °C	163
PCF8200	voice synthesizer (CMOS); I²C-bus	335
PCF83C652P	microcontroller; 256 x 8 RAM; 8 K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; −40 to + 85 °C	163
PCF83C652WP	microcontroller; 256 x 8 RAM; 8 K x 8 ROM; serial I/O; UART; I²C-bus; 1.2 to 12 MHz; −40 to + 85 °C	163
PCF84C00B	microcontroller; 256 x 8 RAM; bond-out version PCF84CXXX family; I²C-bus	375
PCF84C00T	microcontroller; 256 x 8 RAM; bond-out version PCF84CXXX family; I²C-bus	375
PCF84C21P	microcontroller; 64 x 8 RAM; 2 K x 8 ROM; plus 8-bit LED driver; I²C-bus; −40 to + 85 °C	375
PCF84C21T	microcontroller; 64 x 8 RAM; 2 K x 8 ROM; plus 8-bit LED driver; I²C-bus; −40 to + 85 °C	375
PCF84C41P	microcontroller; 128 x 8 RAM; 4 K x 8 ROM; plus 8-bit LED driver; I²C-bus; −40 to + 85 °C	375
PCF84C41T	microcontroller; 128 x 8 RAM; 4 K x 8 ROM; plus 8-bit LED driver; I²C-bus; −40 to + 85 °C	375
PCF84C81P	microcontroller; 256 x 8 RAM; 8 K x 8 ROM; plus 8-bit LED driver; I²C-bus; −40 to + 85 °C	375
PCF84C81T	microcontroller; 256 x 8 RAM; 8 K x 8 ROM; plus 8-bit LED driver; I²C-bus; −40 to + 85 °C	375
PCF84C85P	microcontroller; 256 x 8 RAM; 8 K x 8 ROM; 32 I/O; plus 8-bit LED driver; I²C-bus; −40 to + 85 °C	401
PCF84C85T	microcontroller; 256 x 8 RAM; 8 K x 8 ROM; 32 I/O; plus 8-bit LED driver; I²C-bus; −40 to + 85 °C	401
PCF84C430H	microcontroller; 128 x 8 RAM; 4 K x 8 ROM; plus 96-segment LCD driver; I²C-bus	441

type no.	description	page
PCF8566P	universal LCD driver for low multiplex rates (1:1 to 1:4); max. 96 elements; I²C-bus	497
PCF8566T	universal LCD driver for low multiplex rates (1:1 to 1:4); max. 96 elements; I²C-bus	497
PCF8570P	256 x 8-bit static RAM; I²C-bus	527
PCF8570T	256 x 8-bit static RAM; I²C-bus	527
PCF8570CP	256 x 8-bit static RAM; I²C-bus; different slave address	527
PCF8570CT	256 x 8-bit static RAM; I²C-bus; different slave address	527
PCF8571P	128 x 8-bit static RAM; I²C-bus	527
PCF8571T	128 x 8-bit static RAM; I²C-bus	527
PCF8573P	clock calendar; I²C-bus	537
PCF8573T	clock calendar; I²C-bus	537
PCF8574P	remote 8-bit I/O expander; I²C-bus	555
PCF8574T	remote 8-bit I/O expander; I²C-bus	555
PCF8574AP	remote 8-bit I/O expander; I²C-bus; different slave address	555
PCF8574AT	remote 8-bit I/O expander; I²C-bus; different slave address	555
PCF8576T	universal LCD driver for low multiplex rates (1:1 to 1:4); max. 160 segments; I²C-bus	567
PCF8576U	universal LCD driver for low multiplex rates (1:1 to 1:4); max. 160 segments; I²C-bus	567
PCF8576U/10	universal LCD driver for low multiplex rates (1:1 to 1:4); max. 160 segments; I²C-bus	567
PCF8577P	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	601
PCF8577T	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	601
PCF8577AP	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus; different slave address	601
PCF8577AT	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus; different slave address	601
PCF8577U/5	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	601
PCF8577AU/5	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus; different slave address	601
PCF8577U/10	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	601
PCF8577AU/10	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus; different slave address	601
PCF8578T	LCD row/column driver for dot matrix graphic displays; 40 outputs, of which 24 are programmable; I²C-bus	617
PCF8578U	LCD row/column driver for dot matrix graphic displays; 40 outputs, of which 24 are programmable; I²C-bus	617
PCF8578V	LCD row/column driver for dot matrix graphic displays; 40 outputs, of which 24 are programmable; I²C-bus	617

type no.	description	page
PCF8579T	LCD column driver for dot matrix graphic displays; 40 column outputs; I²C-bus	655
PCF8579U	LCD column driver for dot matrix graphic displays; 40 column outputs; I²C-bus	655
PCF8579V	LCD column driver for dot matrix graphic displays; 40 column outputs; I²C-bus	655
PCF8582AP	256 x 8-bit EEPROM; I²C-bus	707
PCF8582AT	256 x 8-bit EEPROM; I²C-bus	707
PCF8583P	clock calendar with 256 x 8-bit static RAM; I²C-bus	717
PCF8583T	clock calendar with 256 x 8-bit static RAM; I²C-bus	717
PCF8591P	8-bit ADC/DAC; I²C-bus	735
PCF8591T	8-bit ADC/DAC; I²C-bus	735
SAA1064P	4-digit LED driver; I²C-bus	753
SAA1300	tuner switching circuit; I²C-bus	763
SAA3028	high performance transcoder (RC-5) for infrared remote control; I²C-bus	767
SAA4700	VPS dataline processor	775
SAA5243E	enhanced computer-controlled teletext circuit (ECCT); 625-line system; I²C-bus (West European language version)	787
SAA5243H	enhanced computer-controlled teletext circuit (ECCT); 625-line system; I²C-bus (East European language version)	787
SAA5243K	enhanced computer-controlled teletext circuit (ECCT); 625-line system; I²C-bus (Arabic and English version)	787
SAA5243L	enhanced computer-controlled teletext circuit (ECCT); 625-line system; I²C-bus (Arabic and Hebrew version)	787
SAA5245A	525-line system enhanced computer-controlled teletext circuit (USECCT); I²C-bus (West European language version)	817
SAA9041AP	digital video teletext (DVTB) processor for Philips digital TV system (525 and 625-line systems); I²C-bus (West European language version)	839
SAA9050	digital multistandard TV decoder; I²C-bus	859
SAA9055	digital SECAM colour decoder; I²C-bus	891
SAA9068WP	picture-in-picture controller (PIPCO); I²C-bus	913
SAB3035	computer interface for tuning and control (CITAC); without DACs; I²C-bus	929
SAB3036	computer interface for tuning and control (CITAC); without DACs; I²C-bus	945
SAB3037	computer interface for tuning and control (CITAC); 4 DACs; I²C-bus	961
SAF1135	dataline decoder	977

type no.	description	page
SCC68070CAA84	microprocessor; 16/32-bit MPU; 68000 CPU; MMU; DMA; timer; UART; I²C-bus; 10 MHz; 0 to + 70 °C	989
SCC68070CBA84	microprocessor; 16/32-bit MPU; 68000 CPU; MMU; DMA; timer; UART; I²C-bus; 12.5 MHz; 0 to + 70 °C	989
SCC68070CCA84	microprocessor; 16/32-bit MPU; 68000 CPU; MMU; DMA; timer; UART; I²C-bus; 15 MHz; 0 to + 70 °C	989
SCC68070AAA84	microprocessor; 16/32-bit MPU; 68000 CPU; MMU; DMA; timer; UART; I²C-bus; 10 MHz; −40 to + 85 °C	989
SCC68070ABA84	microprocessor; 16/32-bit MPU; 68000 CPU; MMU; DMA; timer; UART; I²C-bus; 12.5 MHz; −40 to + 85 °C	989
SCC68070ACA84	microprocessor; 16/32-bit MPU; 68000 CPU; MMU; DMA; timer; UART; I²C-bus; 15 MHz; −40 to + 85 °C	989
SCC68070CAB	microprocessor; 16/32-bit MPU; 68000 CPU; MMU; DMA; timer; UART; I²C-bus; 10 MHz; 0 to + 70 °C	989
SCC68070CBB	microprocessor; 16/32-bit MPU; 68000 CPU; MMU; DMA; timer; UART; I²C-bus; 12.5 MHz; 0 to + 70 °C	989
SCC68070CCB	microprocessor; 16/32-bit MPU; 68000 CPU; MMU; DMA; timer; UART; I²C-bus; 15 MHz; 0 to + 70 °C	989
SCC68070AAB	microprocessor; 16/32-bit MPU; 68000 CPU; MMU; DMA; timer; UART; I²C-bus; 10 MHz; −40 to + 85 °C	989
SCC68070ABB	microprocessor; 16/32-bit MPU; 68000 CPU; MMU; DMA; timer; UART; I²C-bus; 12.5 MHz; −40 to + 85 °C	989
SCC68070CCACB	microprocessor; 16/32-bit MPU; 68000 CPU; MMU; DMA; timer; UART; I²C-bus; 15 MHz; −40 to + 85 °C	989
TDA8370	synchronization processor for TV; I²C-bus	1051
TDA8405	TV and video recorder stereo/dual sound processor; I²C-bus	1069
TDA8420	hi-fi stereo audio processor; I²C-bus	1079
TDA8421	hi-fi stereo audio processor; I²C-bus	1101
TDA8425	hi-fi stereo audio processor; I²C-bus	1123
TDA8440	video/audio switch for CTV receivers; I²C-bus	1145
TDA8442	I²C-bus interface for colour decoders	1155
TDA8443A	I²C-bus-controlled YUV/RGB interface circuit	1163
TDA8444	octuple 6-bit DAC; I²C-bus	1177
TDA8461	PAL/NTSC decoder; I²C-bus	1185
TEA6000	FM/IF system and microcomputer-based tuning interface; I²C-bus	1209
TEA6100	FM/IF system and microcomputer-based tuning interface; I²C-bus	1221
TEA6300	car radio preamplifier and source selector with sound and fader controls; I²C-bus	1245
TEA6300T	car radio preamplifier and source selector with sound and fader controls; I²C-bus	1245
TEA6310T	sound fader control circuit; I²C-bus	1261
TSA5510	1.3 GHz I²C-bus controlled frequency synthesizer	1279
TSA5510T	1.3 GHz I²C-bus controlled frequency synthesizer	1289
TSA6057	radio tuning PLL frequency synthesizer; I²C-bus	1299
TSA6057T	radio tuning PLL frequency synthesizer; I²C-bus	1299

type no.	description	page
UMA1000T	data processor for cellular radio (DPROC); I^2C-bus	1309
UMA1010T	low-power universal frequency synthesizer for radio communications; 400 to 1150 MHz; I^2C-bus	1339

ASSOCIATED PUBLICATIONS

The following Philips Components publications are available on request.

Title	Order Number
I^2C-bus compatible ICs clip together	9398 350 50011
The I^2C-bus in consumer applications	9398 358 20011
User's Guide to I^2C-bus Control Programs	9398 065 60011
I^2C-bus Control Programs for TV ICs	9398 353 40011

GENERAL

Type designation

Rating systems

Handling MOS devices

I^2C-bus Specification

I^2C-bus Evaluation Board

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : { Microcomputer / Central processing unit }
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : −55 to + 125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and D.C. lines.

I²C-bus Specification

Contents - The I²C-bus Specification

1.0 **Introduction**

2.0 **The I²C-bus concept**

3.0 **General characteristics**

4.0 **Bit transfer**
- 4.1 Data validity
- 4.2 START and STOP conditions

5.0 **Transferring data**
- 5.1 Byte format
- 5.2 Acknowledge

6.0 **Arbitration and clock generation**
- 6.1 Synchronization
- 6.2 Arbitration
- 6.3 Use of the clock synchronizing mechanism as a handshake

7.0 **Formats**

8.0 **Addressing**
- 8.1 Definition of bits in the first byte
  - 8.1.1 General call address
  - 8.1.2 Start byte
  - 8.1.3 CBUS compatibility

9.0 **Electrical specifications of inputs and outputs of I²C-bus interfaces**

10.0 **Timing**

11.0 **'Low-speed' mode**
- 11.1 START and STOP conditions
- 11.2 Data format and timing

Appendix A - Values of resistors R_p and R_s

Appendix B - Note to section 6.2

1.0 Introduction

For 8-bit applications, such as those requiring single-chip microcomputers, certain design criteria can be established:

- A complete system usually consists of at least one microcomputer and other peripheral devices such as memories and I/O expanders.
- The cost of connecting the various devices within the system must be kept to a minimum.
- Such a system usually performs a control function and doesn't require high-speed data transfer.
- Overall efficiency depends on the devices chosen and the interconnecting bus structure.

To produce a system to satisfy these criteria, a serial bus structure is needed. Although serial buses don't have the throughput capability of parallel buses, they do require less wiring and fewer connecting pins. However, a bus is not merely an interconnecting wire, it embodies all the formats and procedures for communication within the system.

ICs communicating with each other on a serial bus must have some form of protocol which avoids all possibilities of confusion, data loss and blockage of information. Fast ICs must be able to communicate with slow ICs. The system must not be dependent on the ICs connected to it, otherwise modifications or improvements would be impossible. A procedure has also to be devised to decide which IC will be in control of the bus and when. And if different ICs with different clock speeds are connected to the bus - the bus clock source must be defined.

All these criteria are involved in the specification of the I²C-bus.

2.0 The I²C-bus concept

The I²C-bus supports ICs manufactured with any process (NMOS, CMOS, I²L). Two wires, serial data (SDA) and serial clock (SCL) carry information between the ICs connected to the bus. Each IC is recognised by a unique address - whether it's a microcomputer, LCD driver, memory or keyboard interface - and can operate as either a transmitter or receiver, depending on the function of the ICs we're considering. Obviously an LCD driver is only a receiver, while a memory can both receive and transmit data. In addition to transmitters and receivers, ICs can also be considered as masters or slaves when performing data transfers (see Table 1). A master is the IC which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any IC addressed is considered a slave.

The I²C-bus is a multi-master bus. This means that more than one IC capable of controlling the bus can be connected to it. As masters are usually microcomputers, let's consider the case of a data transfer between two microcomputers connected to the I²C-bus (Fig.1). This highlights the master-slave and receiver-transmitter relationships to be found on the I²C-bus. It should be noted that these relationships are not permanent, but only depend on the direction of data transfer at that time. The transfer of data would proceed as follows:

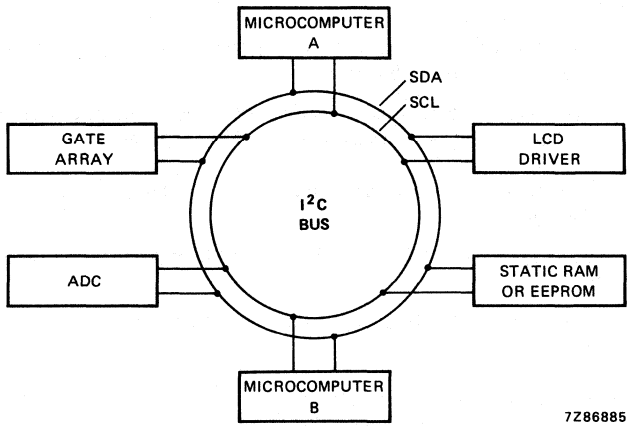


Fig.1 Typical I²C-bus configuration.

1) Suppose microcomputer A wants to send information to microcomputer B:
   - microcomputer A (master), addresses microcomputer B (slave)
   - microcomputer A (master transmitter), sends data to microcomputer B (slave receiver)
   - microcomputer A terminates the transfer.

2) If microcomputer A wants to receive information from microcomputer B:
   - microcomputer A (master) addresses microcomputer B (slave)
   - microcomputer A (master receiver) receives data from microcomputer B (slave transmitter)
   - microcomputer A terminates the transfer.

Even in this case, the master (microcomputer A) generates the timing and terminates the transfer.

The possibility of connecting more than one microcomputer to the I²C-bus means that more than one master could try to initiate a data transfer at the same time. To avoid the chaos that might ensue from such an event - an arbitration procedure has been developed. This procedure relies on the wired-AND connection of all I²C interfaces to the I²C-bus.

If two or more masters try to put information onto the bus, the first to produce a 'one' when the other produces a 'zero' will lose the arbitration. The clock signals during arbitration are a synchronised combination of the clocks generated by the masters using the wired-AND connection to the SCL line (for more detailed information concerning arbitration see section 6.0).

Generation of clock signals on the I²C-bus is always the responsibility of master ICs; each master generates its own clock signals when transferring data on the bus. Bus clock signals from a master can only be altered when they are stretched by a slow-slave IC holding-down the clock line, or by another master when arbitration takes place.

Table 1 Definition of I²C-bus terminology

Transmitter:	the IC which sends data to the bus
Receiver:	the IC which receives data from the bus
Master:	the IC which initiates a transfer, generates clock signals and terminates a transfer
Slave:	the IC addressed by a master
Multi-master:	more than one master can attempt to control the bus at the same time without corrupting the message
Arbitration:	procedure to ensure that if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
Synchronization:	procedure to synchronize the clock signals of two or more ICs

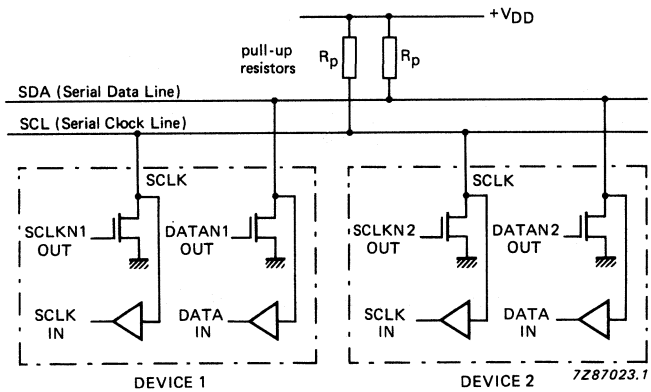


Fig.2 Connection of I²C interfaces to the I²C-bus.

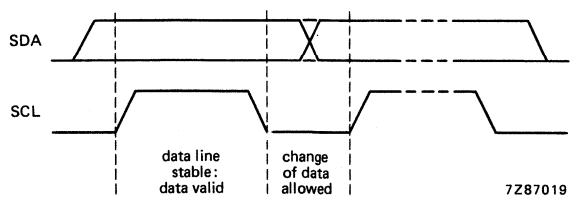


Fig.3 Bit transfer on the I²C-bus.

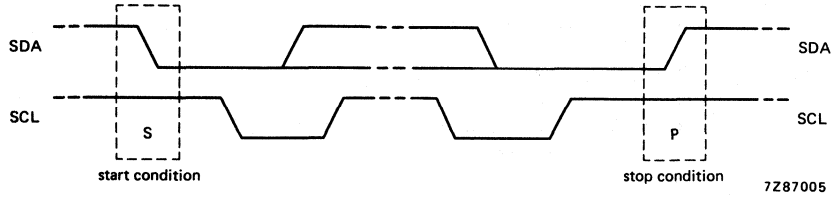


Fig.4 START and STOP conditions.

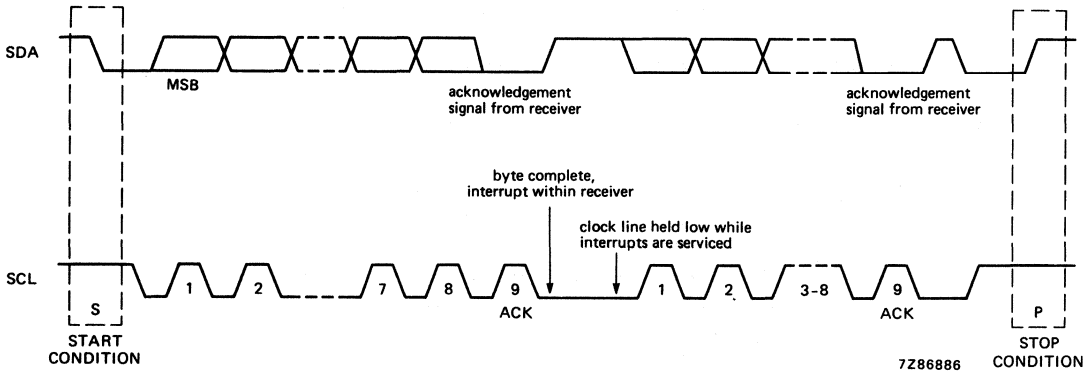


Fig.5 Data transfer on the I²C-bus.

3.0 General characteristics

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor (see Fig.2). When the bus is free, both lines are HIGH. The output stages of I^2C interfaces connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I^2C-bus can be transferred at a rate up to 100 kbit/s. The number of interfaces connected to the bus is solely dependent on the limiting bus capacitance of 400 pF.

4.0 Bit transfer

Due to the variety of different technology ICs (CMOS, NMOS, I^2L) which can be connected to the I^2C-bus, the levels of the logical '0' (LOW) and '1' (HIGH) are not fixed and depend on the associated level of V_{DD} (see section 9.0 for Electrical specifications). One clock pulse is generated for each data bit transferred.

4.1 Data validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Fig.3).

4.2 START and STOP conditions

Within the procedure of the I^2C-bus, unique situations arise which are defined as START and STOP conditions (see Fig.4).

A HIGH to LOW transition of the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition.

A LOW to HIGH transition of the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition. This bus free situation will be described in detail later (in section 10.0).

Detection of START and STOP conditions by ICs connected to the bus is easy if they incorporate the necessary interfacing hardware. However, microcomputers with no such interface have to sample the SDA line at least twice per clock period to sense the transition.

5.0 Transferring data

5.1 Byte format

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (Fig.5). If a receiver can't receive another complete byte of data until it has performed some other function, for example, servicing an internal interrupt, it can hold the clock line SCL LOW to force the transmitter into a wait state. Data transfer then continues when the receiver is ready for another byte of data and releases clock line SCL.

In some cases, it's permissible to use a different format from the I^2C-bus format (for CBUS compatible ICs for example). A message which starts with such an address can be terminated by generation of a STOP condition, even during the transmission of a byte. In this case, no acknowledge is generated (see section 8.4).

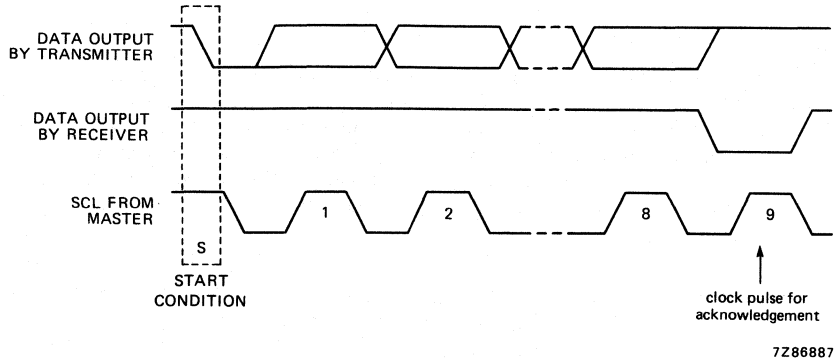


Fig.6 Acknowledge on the I²C-bus.

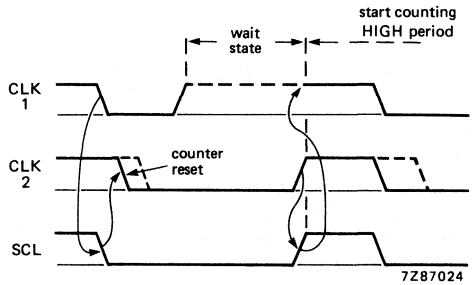


Fig.7 Clock synchronization during the arbitration procedure.

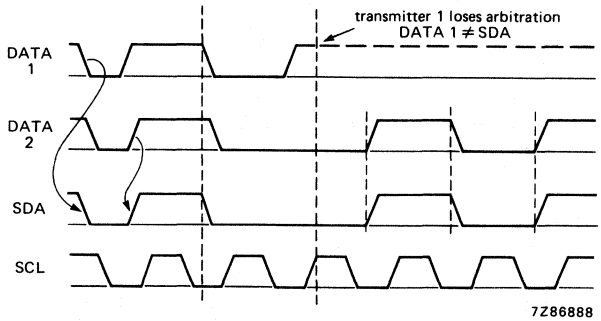


Fig.8 Arbitration procedure of two masters.

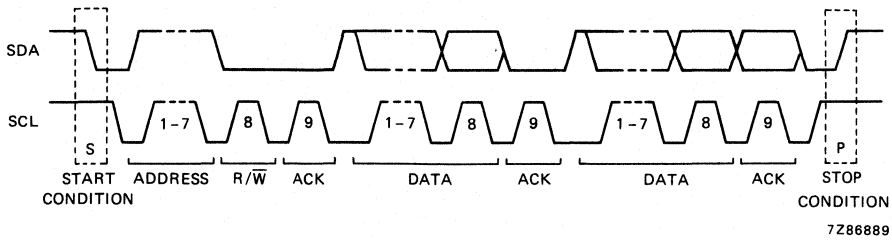


Fig.9 A complete data transfer.

5.2 Acknowledge

Data transfer with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmittier releases the SDA line (HIGH) during the acknowledge clock pulse.

The receiver has to pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the high period of this clock pulse (Fig.6). Of course, set-up and hold times must also be taken into account and these will be described in section 10.0.

Usually, a receiver which has been addressed is obliged to generate an acknowledge after each byte has been received (except when the message starts with an RC-5 or CBUS address - see section 8.1.3).

When a slave receiver doesn't acknowledge on the slave address (for example, it's unable to receive because it's performing some real-time function), the data line has to be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer.

If a slave receiver acknowledges the slave address but, some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the salve not generating the acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

If a master receiver is involved in a transfer, it must signal the end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate the STOP condition.

6.0 Arbitration and clock generation

6.1 Synchronization

All masters generate their own clock on the SCL line to transfer messages on the I²C-bus. Data is only valid during the clock HIGH period. A defined clock is therefore needed for the bit-by-bit arbitration procedure to take place.

Clock synchronization is performed using the wired-AND connection of I²C interfaces to the SCL line. This means that a HIGH to LOW transition on the SCL line will cause the ICs concerned to start counting off their LOW period and, once an IC clock has gone LOW, it will hold the SCL line in that state until the clock HIGH state is reached (Fig.7). However, the LOW to HIGH transition of this clock may not change the state of the SCL line if another clock is still within its LOW period. The SCL line will therefore be held LOW by the IC with the longest LOW period. ICs with shorter LOW periods enter a HIGH wait-state during this time.

When all ICs concerned have counted off their LOW period, the clock line will be released and go HIGH. There will then be no difference between the IC clocks and the state of the SCL line and all the ICs will start counting their HIGH periods. The first IC to complete its HIGH period will again pull the SCL line LOW.

In this way, a synchronized SCL clock is generated with its LOW period determined by the IC with the longest clock LOW period, and its HIGH period determined by the one with the shortest clock HIGH period.

6.2 Arbitration (see also Appendix B)

Arbitration takes place on the SDA line in such a way that the master which transmits a HIGH level, while another master is transmitting a LOW level will switch off its DATA output stage because the level on the bus doesn't correspond to its own level.

Arbitration can continue for many bits. Its first stage is comparison of the address bits (addressing information is in section 8.0). If the masters are each trying to address the same IC, arbitration continues with comparison of the data. Because address and data information on the I²C-bus is used for arbitration, no information is lost during this process.

A master which loses the arbitration can generate clock pulses until the end of the byte in which it loses the arbitration.

If a master loses arbitration during the addressing stage, it's possible that the winning master is trying to address it. The losing master must therefore switch over immediately to its slave receiver mode.

Figure 8 shows the arbitration procedure for two masters. Of course, more may be involved (depending on how many masters are connected to the bus). The moment there is a difference between the internal data level of the master generating DATA 1 and the actual level on the SDA line, its data output is switched off, which means that a HIGH output level is then connected to the bus. This will not affect the data transfer initiated by the winning master. Since control of the I²C-bus is decided solely on the address and data sent by competing masters, there is no central master, nor any order of priority on the bus.

6.3 Use of the clock synchronizing mechanism as a handshake

In addition to being used during the arbitration procedure, the clock synchronization mechanism can be used to enable receivers to cope with fast data transfers, on either a byte level or a bit level.

On the byte level, an IC may be able to receive bytes of data at a fast rate, but needs more time to store a received byte or prepare another byte to be transmitted. Slaves can then hold the SCL line LOW after reception and acknowledgement of a byte to force the master into a wait state until the slave is ready for the next byte transfer in a type of handshake procedure.

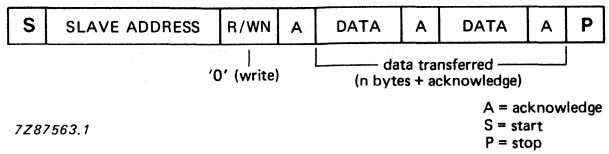
On the bit level, an IC such as a microcomputer without a hardware I²C interface on-chip can slow down the bus clock by extending each clock LOW period. In this way, the speed of any master is adapted to the internal operating rate of this IC.

7.0 Formats

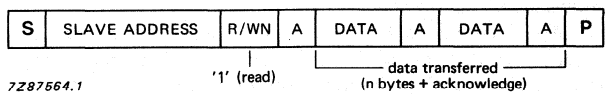
Data transfers follow the format shown in Fig.9. After the START condition, a slave address is sent. This address is 7 bits long, the eighth bit is a data direction bit ($R/\overline{W}$) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition generated by the master. However, if a master still wishes to communicate on the bus, it can generate another START condition and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such a transfer.

Possible data transfer formats are:

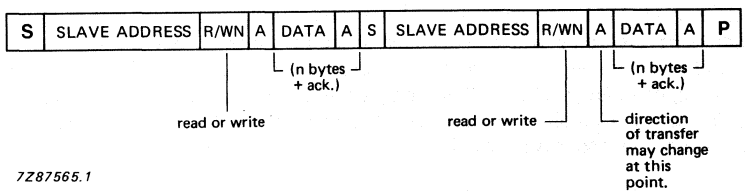
a) Master transmitter transmits to slave receiver. Direction is not changed.



b) Master reads slave immediately after first byte.



At the moment of the first acknowledge, the master transmitter becomes a master receiver and teh slave receiver becomes a slave transmitter. This acknowledge is still generated by the slave.
The STOP condition is generated by the master.



slave address are both repeated, but with the R/ W bit reversed.

During a change of direction within a transfer, the START condition and the

NOTES:

1) Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the START condition is repeated, data can be transferred.
2) All decisions on auto-increment or decrement of previously accessed memory locations etc. are taken by the designer of the IC.
3) Each byte is followed by an acknowledge as indicated by the A blocks in the sequence.
4) I²C-bus compatible ICs must reset their bus logic on receipt of a START condition such that they all anticipate the sending of a slave address.

8.0 Addressing

The addressing procedure for the I²C-bus is such that the first byte after the START condition determines which slave will be selected by the master. Usually, this first byte follows that start procedure. The exception is the 'general call' address which can address all ICs. When this address is used, all ICs should, in theory, respond with an acknowledge. However, ICs can be made to ignore this address. The second byte of the general call address then defines the action to be taken.

8.1 Definition of bits in the first byte

The first seven bits of the first byte make up the slave address (Fig.10). The eighth bit is the LSB (least significant bit). It determines the direction of the message. A 'zero' in the least significant position of the first byte means that the master will write information to a selected slave. A 'one' in this position means that the master will read information from the slave.

When an address is sent, each IC in a system compares the first 7 bits after the START condition with its address. If they match, the IC considers itself addressed by the master as a slave receiver or slave transmitter, depending on the R/$\overline{W}$ bit.

A slave address can be made-up of a fixed and a programmable part. Since it's likely that there will be several identical ICs in a system, the programmable part of the slave address enables the maximum possible number of such ICs to be connected to the I²C-bus. The number of programmable address bits of an IC depends on the number of pins available. For example, if an IC has 4 fixed and 3 programmable address bits, a total of 8 identical ICs can be connected to the same bus.

The I²C-bus committee coordinates allocation of I²C addresses. The bit combination 1111XXX of the slave address is reserved for future extension purposes. Address 1111111 is reserved as the extension address. This means that the addressing procedure will be continued in the next byte(s). ICs that don't use the extended addressing don't react on reception of this byte. The seven other possibilities in group 1111 will also only be used for extension purposes but are not yet allocated. Combination 0000XXX has been defined as a special group. The following addresses have been allocated (also see notes on next page):

first byte: SLAVE ADDRESS	first byte: R/$\overline{W}$		
0000 000	0	general call address	see NOTES on next page
0000 000	1	start byte	see NOTES on next page
0000 001	X	CBUS address	see NOTES on next page
0000 010	X	Address reserved for different bus format	see NOTES on next page
0000 011	X	to be defined	
0000 100	X	to be defined	
0000 101	X	to be defined	
0000 110	X	to be defined	
0000 111	X	to be defined	

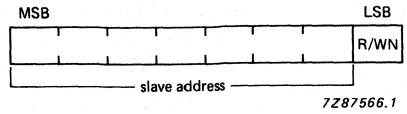


Fig.10 The first byte after the start procedure.

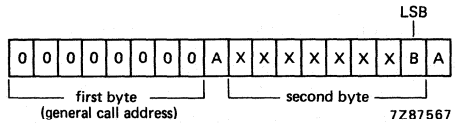


Fig.11 General call address format.

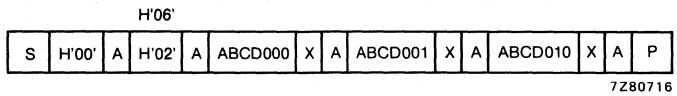


Fig.12 Sequence of a programming master.

NOTES:

1) No IC is allowed to acknowledge at the reception of the START byte.

2) The CBUS address has been reserved to enable the inter-mixing of CBUS compatible and I²C-bus compatible ICs in the same system. I²C-bus compatible ICs are not allowed to respond on reception of this address.

3) The address reserved for a different bus format is included to enable I²C and other protocols to be mixed. Only I²C-bus compatible ICs that can work with such formats and protocols are allowed to respond to this address.

8.1.1 General call address

The general call address should be used to address every IC connected to the I²C-bus. However, if an IC doesn't need any of the data supplied within the general call structure, it can ignore this address by not acknowledging. If an IC does require data from a general call address, it will acknowledge this address and behave as a slave receiver. The second and following bytes will be acknowledged by every slave receiver capable of handling this data. A slave which cannot process one of these bytes must ignore it by not acknowledging. The meaning of the general call address is always specified in the second byte (Fig.11).

There are two cases to consider:

- When the least significant bit B is a 'zero'.
- When the least significant bit B is a 'one'.

When B is a 'zero'; the second byte has the following definition:

00000110 (H'06') Reset and write programmable part of slave address by software and hardware. On receiving this 2-byte sequence, all ICs designed to respond to the general call address will reset and take in the programmable part of their address. Precautions have to be taken to ensure that an IC is not pulling down the SDA or SCL line after applying the supply voltage, since these low levels would block the bus.

00000010 (H'02') Write slave address by software only. All ICs which obtain the programmable part of their address by software (and which have been designed to respond to the general call address) will enter a mode in which they can be programmed. The IC will not reset. An example of a data transfer of a programming master is shown in Fig.12 (ABCD represents the fixed part of the address).

00000100 (H'04') Write slave address by hardware only. All ICs which define the programmable part of their address by hardware (and which respond to the general call address) will latch this programmable part at the reception of this two byte sequence. The IC will not reset.

00000000 (H'00') This code is not allowed to be used as the second byte. Sequences of programming procedure are published in the appropriate IC data sheets.

The remaining codes have not been fixed and ICs must ignore them.

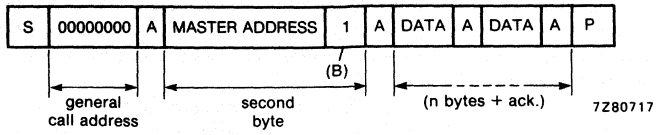


Fig.13 Data transfer from a hardware master transmitter.

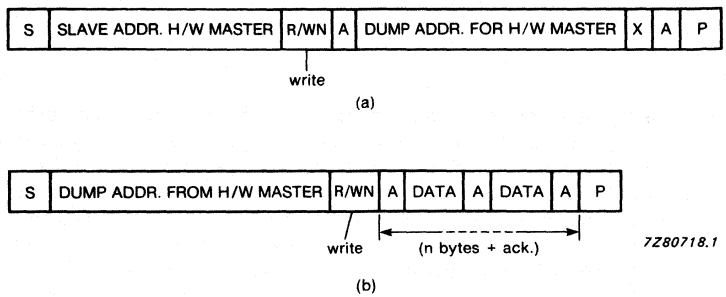


Fig.14 Data transfer by a hardware transmitter capable of dumping data directly to slave ICs:
(a) Configuring master sends dump address to hardware master
(b) Hardware master dumps data to selected slave

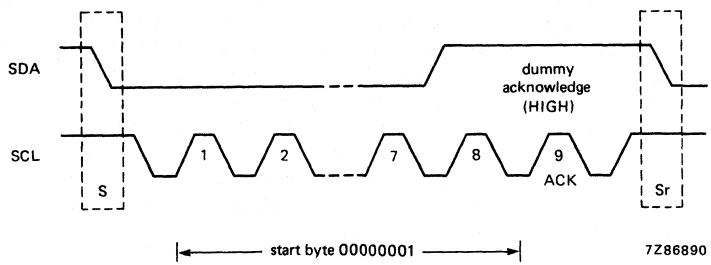


Fig.15 Start byte procedure.

When B is a 'one'; the 2-byte sequence is a 'hardware general call'. This means that the sequence is transmitted by a hardware master IC, such as a keyboard scanner, which cannot be programmed to transmit a desired slave address. Since a hardware master doesn't know in advance to which IC the message has to be transferred, it can only generate this hardware general call and its own address - identifying itself to the system (Fig.13).

The seven bits remaining in the second byte contain the address of the hardware master. This address is recognised by an intelligent IC, such as a microcomputer, connected to the bus which will then direct the information from the hardware master. If the hardware master can also act as a slave, the slave address is identical to the master address.

In some systems, an alternative could be that the hardware master transmitter is set in the slave receiver mode after the system reset. In this way, a system configuring master can tell the hardware master transmitter (which is now in slave receiver mode) to which address data must be sent (Fig.14). After this programming procedure, the hardware master remains in the master transmitter mode.

8.1.2 start byte

Microcomputers can be connected to the I²C-bus in two ways. A microcomputer with an on-chip hardware I²C-bus interface can be programmed to be only interrupted by requests from the bus. When the IC doesn't have such an interface, it must constantly monitor the bus via software. Obviously, the more times the microcomputer monitors, or polls, the bus the less time it can spend carrying out its intended function. There is therefore a speed difference between fast hardware ICs and a relatively slow microcomputer which relies on software polling.

In this case, data transfer can be preceded by a start procedure which is much longer than normal (Fig.15). The start procedure consists of:

a) A START condition S

b) A start byte 00000001

c) An acknowledge clock pulse

d) A repeated START condition Sr

After the START condition S has been transmitted by a master which requires bus access, the start byte (00000001) is transmitted. Another microcomputer can therefore sample the SDA line at a low sampling rate until one of the seven zeros in the start byte is detected. After detection of this LOW level on the SDA line, the microcomputer can switch to a higher sampling rate to find the repeated START condition Sr which is then used for synchronization.

A hardware receiver will reset on receipt of the repeated START condition Sr and will therefore ignore the start byte.

An acknowledge-related clock pulse is generated after the start byte. This is present only to conform with the byte handling format used on the bus. No IC is allowed to acknowledge the start byte.

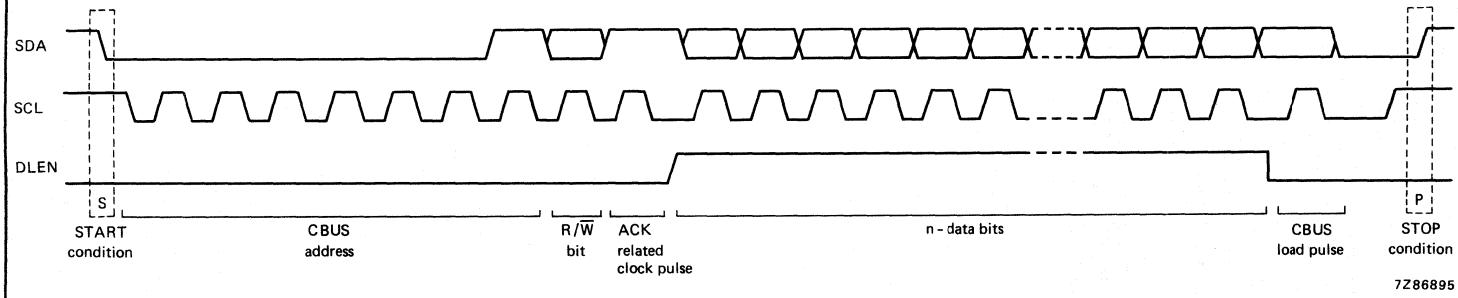


Fig.16 Data format of transmissions with CBUS receiver/transmitter.

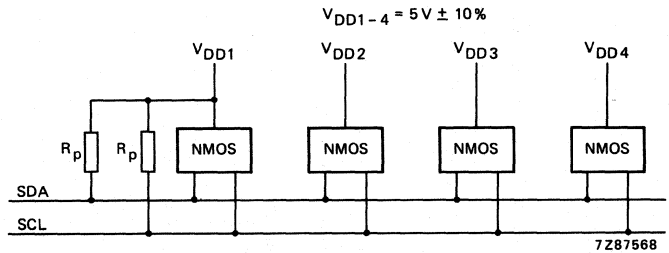


Fig.17 Fixed input level ICs connected to the I²C-bus.

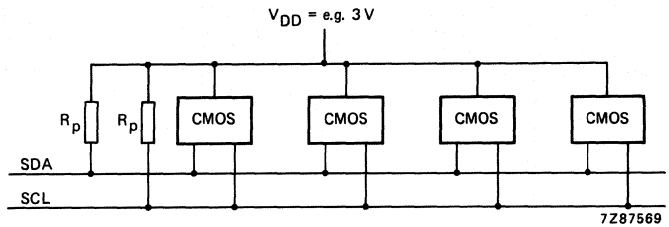


Fig.18 ICs with a wide range of supply voltages connected to the I²C-bus.

8.1.3 CBUS compatibility

Existing CBUS receivers can be connected to the I²C-bus. However, in this case, a third line called DLEN has to be connected and the acknowledge bit omitted. Normally, I²C transmissions are sequences of 8-bit bytes; CBUS compatible ICs have different formats however.

In a mixed bus structure, I²C-bus compatible ICs are not allowed to respond to the CBUS message. For this reason, a special CBUS address (0000001X) to which no I²C-bus compatible IC will respond, has been reserved. After transmission of the CBUS address, the DLEN line can be made active and transmission, according to the CBUS format, can be performed (Fig.16). After the STOP condition, all ICs are again ready to accept data.

Master transmitters are allowed to generate CBUS formats after having sent the CBUS address. Such a transmission is terminated by a STOP condition, recognised by all ICs. In the 'low speed' mode (see Section 11.0), full 8-bit bytes must always be transmitted and the timing of the DLEN signal adapted.

NOTE: If the CBUS configuration is known, and expansion with CBUS compatible ICs isn't foreseen, the designer is allowed to adapt the hold time to the specific requirements of IC(s) used.

9.0 Electrical specifications of inputs and outputs of I²C interfaces

The I²C-bus allows communication between ICs fabricated in different technologies which might also operate from different supply voltages. For interfaces with fixed input levels, operating on a supply voltage of 5 V ± 10%, the following levels have been defined:

$V_{IL\ max}$ = 1.5 V (maximum input LOW voltage)

$V_{IH\ min}$ = 3.0 V (minimum input HIGH voltage)

Interfaces in ICs operating from a fixed supply voltage other than 5 V (e.g. I²L ICs), must also have these input levels of 1.5 V and 3.0 V for V_{IL} and V_{IH} respectively.

For ICs capable of operating from a wide range of supply voltages (e.g. CMOS ICs), the following levels have been defined:

$V_{IL\ max}$ = 0.3 V_{DD} (maximum input LOW voltage)

$V_{IH\ min}$ = 0.7 V_{DD} (minimum input HIGH voltage)

The maximum output LOW level for both groups is:

$V_{OL\ max}$ = 0.4 V at 3 mA sink current.

The maximum LOW level input current at $V_{OL\ max}$ of both the SDA and SCL pin of an I²C-bus compatible IC is -10 μA, including the leakage current of a possible output stage.

The maximum HIGH level input current at 90% V_{DD} for both the SDA and SCL pin of an I²C-bus compatible IC is 10 μA, including the leakage current of a possible output stage.

The maximum capacitance of both the SDA and SCL pin of an I²C-bus compatible IC is 10 pF.

I²C interfaces with fixed input levels can each have their own power supply of 5 V ± 10%. Pull-up resistors can be connected to any supply (Fig.17). However, I²C interfaces with input levels related to V_{DD} must have one common supply line to which the pull-up resistor is also connected (Fig.18).

When ICs having interfaces with fixed input levels are mixed with ICs which have interfaces with input levels related to V_{DD}, the latter ICs must be connected to one common supply line of 5 V ± 10% and must have pull-up resistors connected to their SDA and SCL pins as shown in Fig.19.

Input levels are defined in such a way that:

1) The noise margin on the LOW level is 0.1 V_{DD}.
2) The noise margin on the HIGH level is 0.2 V_{DD}.
3) Series resistors (R_S) up to 300 Ω can be used for protection against high voltage spikes on the SDA and SCL line due to flash-over of a TV picture tube, for example (Fig.20).

The maximum bus capacitance per wire is 400 pF. This includes the capacitance of the wire itself and the capacitance of the pins connected to it.

10.0 Timing

The clock on the I²C-bus has a minimum LOW period of 4.7 μs and a minimum HIGH period of 4 μs. Masters in this mode can generate a bus clock with a frequency up to 100 kHz.

All ICs connected to the bus must be able to follow transfers with frequencies up to 100 kHz, either by being able to transmit or receive at that speed or by applying the clock synchronization procedure which will force the master into a wait state and stretch the LOW periods. Of course, in the latter case the frequency is reduced.

Figure 21 shows the timing requirements in detail, a description of the abbreviations used is shown in the following Table. All timing references are at $V_{IL\ max}$ and $V_{IH\ min}$.

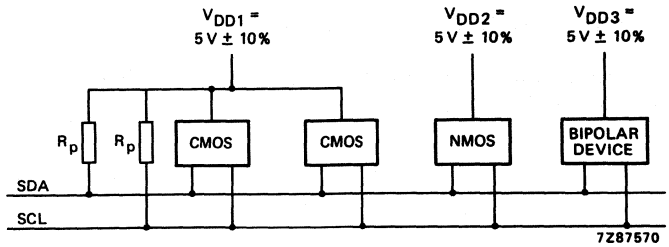


Fig.19 Interfaces with input levels related to V_{DD} mixed with fixed input level interfaces on the I²C-bus.

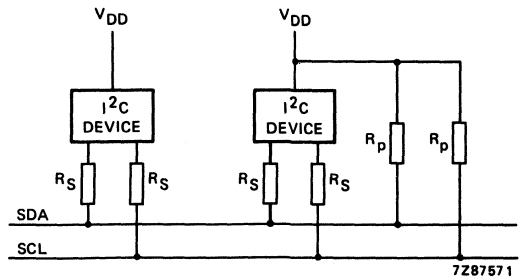


Fig.20 Series resistors (R_S) for protection against high-voltage spikes.

parameter	symbol	min.	max.	units
SCL clock frequency	f_{SCL}	0	100	kHz
Time the bus must be free before a new transmission can start	t_{BUF}	4.7	–	μs
Hold time START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	μs
LOW period of the clock	t_{LOW}	4.7	–	μs
HIGH period of the clock	t_{HIGH}	4.0	–	μs
Set-up time for START condition (Only relevant for a repeated START condition)	$t_{SU;STA}$	4.7	–	μs
Hold time DATA	$t_{HD;DAT}$			
for CBUS compatible masters (see NOTE, Section 8.1.3)		5	–	μs
for I²C ICs		0*	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	ns
Rise time of both SDA and SCL lines	t_R	–	1	μs
Fall time of both SDA and SCL lines	t_F	–	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.7	–	μs

All values referred to V_{IH} and V_{IL} levels (see section 9.0).

* Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.

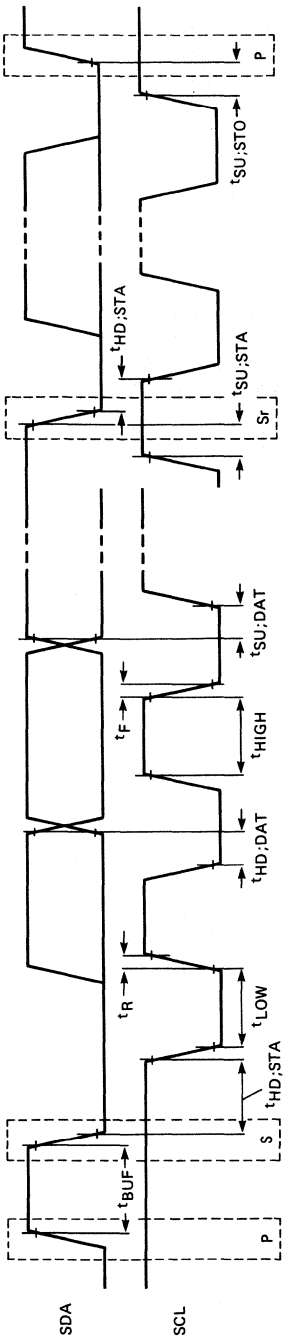


Fig.21 Timing requirements for the I²C-bus.

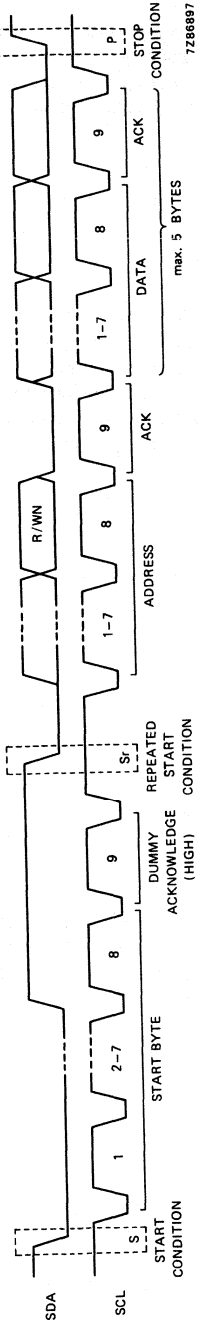


Fig.22 Data transfer in the 'low speed' mode.

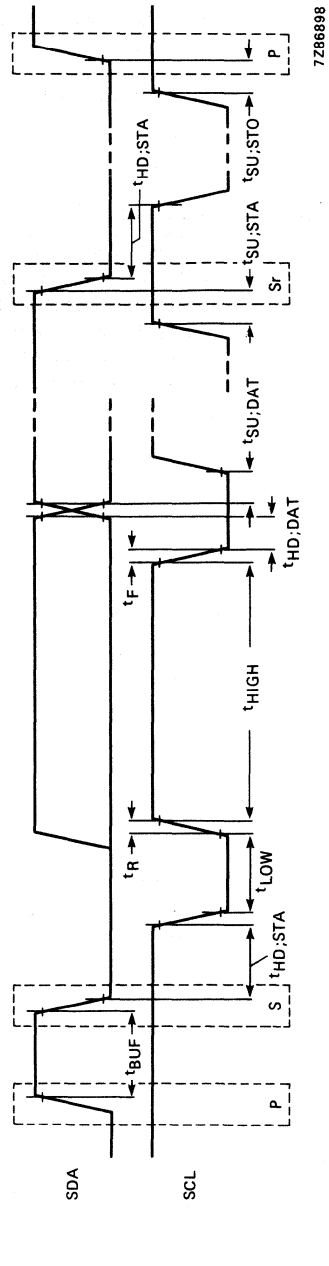


Fig.23 Timing in the 'low speed' mode.

11.0 'Low speed' mode

As explained in section 8.1.2, there is a difference in speed on the I²C-bus between fast hardware interfaces and a relatively slow microcomputer which relies on software polling. For this reason a 'low speed' mode is available on the I²C-bus to allow these microcomputers to poll the bus less often.

11.1 START and STOP conditions

In the 'low speed' mode, data transfer is preceded by the start procedure of section 8.1.2.

11.2 Data format and timing

The bus clock in this mode has a LOW period of 130 μs ± 25 μs and a HIGH period of 390 μs ± 25 μs, resulting in a clock frequency of about 2 kHz. This clock duty cycle allows for more efficient use of microcomputers without an on-chip hardware I²C-bus interface. Also in this mode, data transfer with acknowledge is obligatory. the maximum number of bytes transferred is unlimited (Fig.22).

In this mode, a transfer cannot be terminated during the transmission of a byte.

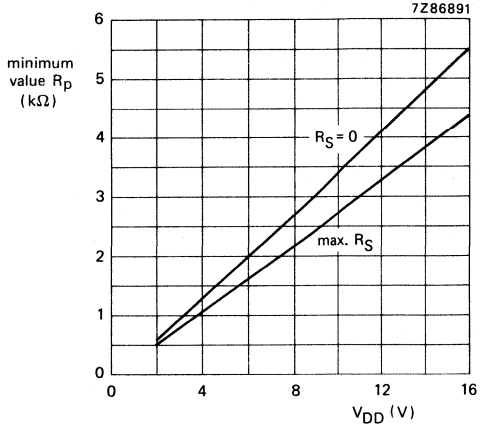
Clock	t_{LOW} = 130 μs ± 25 μs t_{HIGH} = 390 μs ± 25 μs
Duty cycle	1:3 LOW to HIGH (Duty cycle of clock generator)
Start byte	0000 0001
Max. number of bytes	unrestricted
premature termination of transfer	not allowed
acknowledge clock bit	always provided
acknowledgement of slaves	obligatory

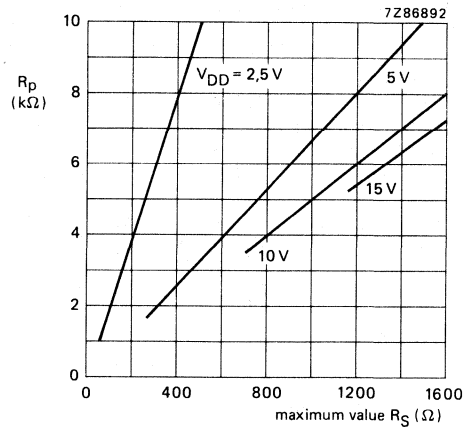
The bus is considered to be busy after the first START condition. It is considered to be free again one minimum clock LOW period (105 μs) after detection of the STOP condition. Figure 23 shows the timing requirements in detail and the following Table explains the abbreviations.

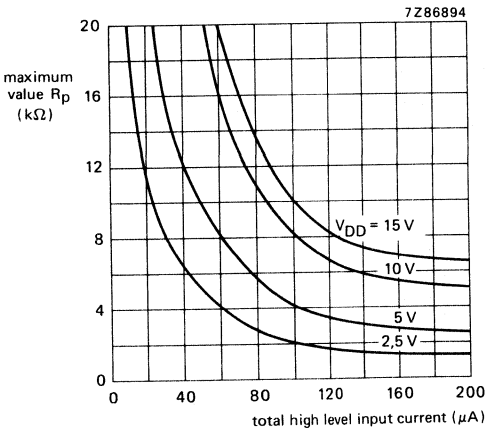
parameter	symbol	min.	max.	units
Time the bus must be free before a new transmission can start	t_{BUF}	105	–	μs
IHold time START condition. After this period the first clock pulse is generated	$t_{HD;STA}$	365	–	μs
Hold time (repeated START condition only)	$t_{HD;STA}$	210	–	μs
LOW period of the clock	t_{LOW}	105	155	μs
HIGH period of the clock	t_{HIGH}	365	415	μs
Set up time for START condition (Only relevant for a repeated START condition)	$t_{SU;STA}$	105	155	μs
Hold time DATA	$t_{HD;DAT}$			
for CBUS compatible masters (see also NOTE, Section 8.1.3)		5	–	μs
for I²C ICs		0*	–	μs
Set-up time DATA	$t_{SU;DAT}$	250	–	ns
Rise time of both SDA and SCL lines	$t_{Rñ}$	–	1	μs
Fall time of both SDA and SCL lines	t_F	–	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	105	155	μs

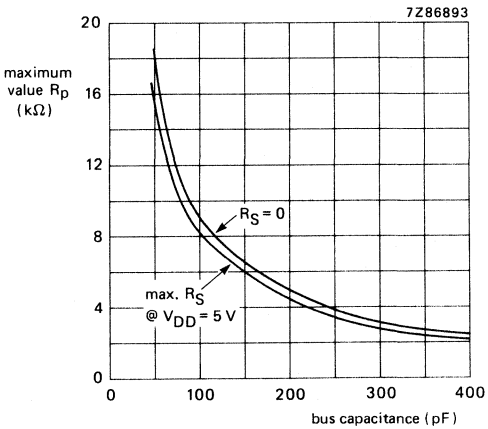
All values referred to V_{IH} and V_{IL} levels (see section 9.0).

* Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.


7Z86891
minimum value R_p (kΩ)
$R_S = 0$
max. R_S
V_{DD} (V)


7Z86892
R_p (kΩ)
V_{DD} = 2,5 V
5 V
15 V
10 V
maximum value R_S (Ω)


7Z86894
maximum value R_p (kΩ)
V_{DD} = 15 V
10 V
5 V
2,5 V
total high level input current (μA)


7Z86893
maximum value R_p (kΩ)
$R_S = 0$
max. R_S @ V_{DD} = 5 V
bus capacitance (pF)

Appendix A - Values of resistors R_p and R_s in Fig.20

In an I²C-bus system these values depend on the following parameters:

1) Supply voltage

2) Bus capacitance

3) Number of connected ICs (input current + leakage current)

1) The supply voltage limits the minimum value of resistor R_p due to the specified minimum sink current of 3 mA at V_{OLmax} = 0.4 V for the output stages. V_{DD} as a function of $R_{p\ min}$ is shown in a graph on the facing page. The desired noise margin of 10% 0f V_{DD} for the LOW level limits the maximum value of R_s. $R_{S\ max}$ as a function of R_p is shown in another graph on the facing page.

2) The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of R_p due to the specified rise time of 1 µsec. A graph on the facing page shows $R_{p\ max}$ as a function of bus capacitance.

3) The maximum HIGH level input current of each input/output connection has a specified maximum value of 10 µA. Due to the desired noise margin of 20% of V_{DD} for the HIGH level, this input current limits the maximum value of R_p. This limit depends on V_{DD}. The total HIGH level input current is shown as a function of R_p max in a graph on the facing page.

Appendix B - Note to section 6.2

Special attention must be paid if, during a serial transfer, the arbitration procedure is still in progress at the moment when a repeated START condition or a STOP condition is transmitted to the I²C-bus. If it's possible for such a situation to occur, the masters involved must send this repeated START condition or STOP condition at the same position in the format frame. In other words, arbitration isn't allowed between:

- a repeated START condition and a data bit,
- a STOP condition and a data bit,
- a repeated START condition and a STOP condition.

I²C-BUS EVALUATION BOARD

I²C-bus Evaluation Board.

MICROCONTROLLER
The PCF84C00T has an I²C Bus enhanced 8048 architecture. A 27C64 CMOS EPROM is provided with sample software to execute a clock calendar plus A/D and D/A demonstration. Alternatively, this module may be used to emulate many of the mask programmed members of the 84CXX family.

CLOCK CALENDAR RAM
The PCF8583 provides real time clock calendar functions and also incorporates 256 bytes of RAM. The circuit is battery backed with a single 1.5 volt silver cell and draws only 2uA of back-up current. The I.C. has an interrupt output and may be configured as a timer /counter with internal or external source.

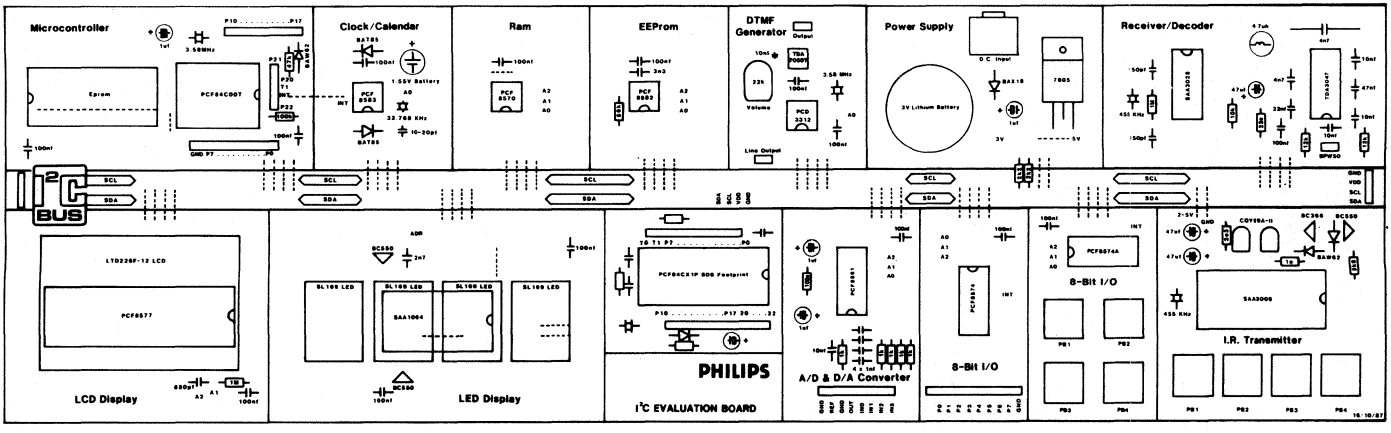
RAM
This module uses the PCF8570 256 byte CMOS RAM. It should be noted that the PCF8583 clock/calendar, PCF8570/71 RAMs and the PCF8572/82 EEPROMs are pin compatible and thus allow a manufacturer to configure his product with the required functions without PCB changes.

EEPROM
The PCF8582 EEPROM provides 256 bytes of non-volatile memory on the Bus. It operates from a single 5V power supply and incorporates EEPROM, Erase/Write circuitry and I²C interface in a single 8 pin package.

D.T.M.F. TONE GENERATOR
The PCD3312 module provides all standard DTMF tones, Modem tones and two octaves of audio tones. These are available either directly from the line output socket or from the TDA7050T SMD audio amplifier.

POWER SUPPLY
This module accepts an unregulated 9 volt DC input from an external power supply and provides regulated 5 volts to the board. Alternatively power may be sourced from the Lithium cell on board if the incompatible peripherals (LEDs etc.) are disconnected.

I.R. RECEIVER DECODER
This module uses the BPW50 to receive the I.R. Signal. It is then amplified and detected by the TDA3047 and converted from RC5 to I²C protocol by the SAA3028 decoder I.C.



LCD DISPLAY
This module features a PCF8577 32/64 segment LCD display driver coupled to an LTD226F-12 32 segment LCD. On the evaluation board the I.C. is mounted under the LCD display and drives the display in direct 1:1 mode.

LED DISPLAY
The SAA1064 four digit 7 segment LED display I.C. provides drive for 32 segments without external current limiting resistors and offers software controllable brightness. These features are shown by the demonstration software.

SDS EMULATION FOOTPRINT
This footprint is provided to allow a microcontroller development system with a MAB84X1 or PCF84CX1 probe to interface with the I²C Evaluation Board. Alternatively this space may be used with the MAB8400B or the PCF84C00B piggyback microcontrollers.

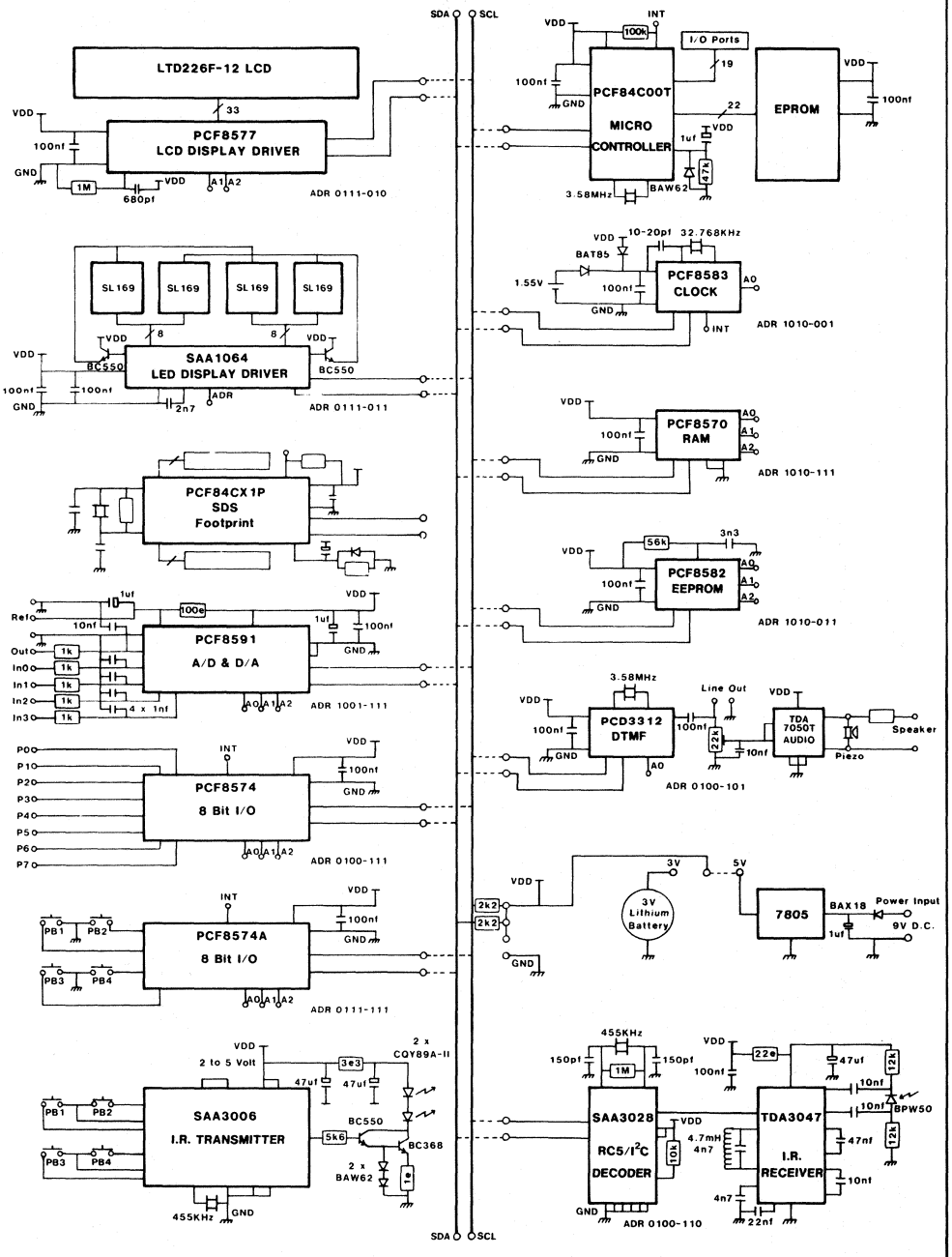
A/D - D/A CONVERTER
The PCF8591 8-Bit A/D-D/A converter has four multiplexed analogue inputs and one D/A output. The analogue multiplexer may be programmed to provide single ended, mixed single-ended and differential inputs or two differential inputs.

8-BIT I/O PORT
The PCF8574 (address 0100XXX) 8-Bit I/O port is identical to the PCF8574A (address 0111XXX) except for its mask defined slave address. Three pin definable address bits on each device allows a total of sixteen 8-Bit ports to be resident on the bus.

8 BIT I/O PORT
The PCF8574A has 8 quasi-bidirectional I/O lines with high current sinking capability. An open drain interrupt line signals a change of state on any input. On the evaluation board the PCF8574A is configured with four push button inputs for use with the demonstration software.

I.R. TRANSMITTER
The SAA3006 encodes up to 64 keys and allows 2048 different codes to be transmitted via an infra-red RC-5 encoded data link. The evaluation board is supplied with four push buttons and two I.R. transmit LED's. The module may run off a 2 to 5 volt supply.

I²C Evaluation Board



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DEVICE DATA

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB84X1 family of microcontrollers is fabricated in NMOS. The family consists of 5 devices:

- MAB8401 – 128 bytes RAM, external program memory, with 8-bit LED-driver (10mA), emulation of MAB/F8422/42* possible
- MAB/MAF8411 – 1K byte ROM/64 bytes RAM plus 8-bit LED-driver
- MAB/MAF8421 – 2K bytes ROM/64 bytes RAM plus 8-bit LED-driver
- MAB/MAF8441 – 4K bytes ROM/128 bytes RAM plus 8-bit LED-driver
- MAB/MAF8461 – 6K bytes ROM/128 bytes RAM plus 8-bit LED-driver

Each version has 20 quasi-bidirectional I/O port lines, one serial I/O line, one single-level vectored interrupt, an 8-bit timer/event counter and on-board clock oscillator and clock circuits. Two 20-pin versions, MAB/F8422 and MAB/F8442* are also available.

This microcontroller family is designed to be an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048. The microcontrollers have extensive bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information see the "8-bit Single-chip Microcontrollers user manual".

* See data sheet on MAB/F8422/42.

Features

- 8-bit: CPU, ROM, RAM and I/O in a single 28-lead DIL package
- 1K, 2K, 4K or 6K ROM bytes plus a ROM-less version
- 64 or 128 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two testable inputs: one of which can be used to detect zero cross-over, the other is also the external interrupt input
- Single level vectored interrupts: external, timer/event counter, serial I/O
- Serial I/O that can be used in single or multi-master systems (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Internal oscillator, generated with inductor, crystal, ceramic resonator or external source
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single 5 V power supply (± 10%)
- Operating temperature ranges:

0 to + 70 °C	MAB84X1 family
−40 to + 85 °C	MAF84X1 family only
−40 to + 110 °C	MAF84AX1 family only

PACKAGE OUTLINES

MAB8401B: 28-lead 'Piggy-back' package (with up to 28-pin EPROM on top).
MAB8401WP: 68-lead plastic leaded chip-carrier (PLCC) (SOT-188).
MAB/MAF8411/21/41/61P: 28-lead DIL; plastic (SOT-117).
MAF84A11/21/41/61P: 28-lead DIL; plastic (SOT-117).
MAB8411/21/41/61T: 28-lead mini-pack; plastic (SO-28; SOT-136A).

PINNING

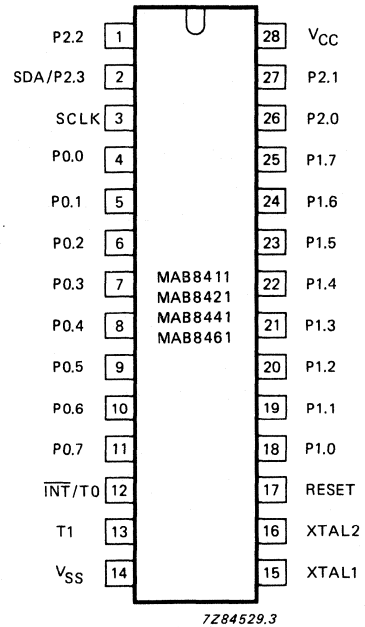
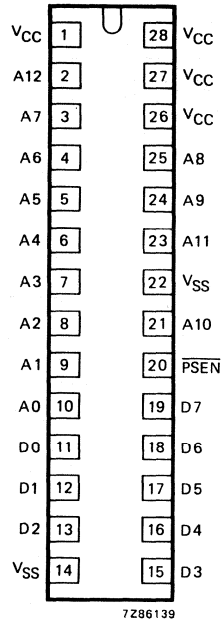


Fig. 1 Pinning diagram for mask-programmable devices MAB8411, MAB8421, MAB8441, MAB8461 and for MAB8401 'Piggy-back' version bottom pinning (for top pinning see Fig. 2).

PINNING DESIGNATION

V_{SS}	14	**Ground**
V_{CC}	28	**Power supply,** + 5 V
P0.0 – P0.7	4 – 11	**Port 0,** 8-bit quasi-bidirectional I/O port
P1.0 – P1.7	18 – 25	**Port 1,** 8-bit quasi-bidirectional I/O port with 8-bit LED driver
P2.0 – P2.3	26, 27, 1, 2	**Port 2,** 4-bit quasi-bidirectional I/O port; SDA/P2.3 is the serial data I/O in serial I/O mode
SCLK	3	Bidirectional clock for serial I/O
$\overline{INT}$/T0	12	External interrupt input (sensitive to a negative-going edge min LOW > 7 clock pulses, min HIGH > 4 clock pulses), testable using the JT0 or JNT0 instructions.
T1	13	Input pin, testable using the JT1 or JNT1 instructions. It can be designated as event counter input using the STRT CNT instruction. It can also be used to detect zero cross-over of slowly moving a.c. inputs.
RESET	17	Input to initialize the processor (active HIGH).
XTAL1	15	Connection to timing component (crystal) that determines the frequency of the internal oscillator. It is also the input for an external clock source.
XTAL2	16	Connection to other side of the timing component.

MAB8401B (top pinning)



PIN DESIGNATION

designation	pin	function
V_{SS}	14, 22	**Ground**
V_{CC}	1, 26–28	**Power supply,** + 5 V
A0–A12	10–3, 25, 24, 21, 23, 2	Address outputs
D0–D7	11–13, 15–19	Data inputs
$\overline{PSEN}$	20	Program store enable

Fig. 2 Pinning diagram for MAB8401B 'Piggy-back' version top pinning (for bottom pinning see Fig. 1); to access a 2732 or 2764 EPROM.

Note

Access times for ROMS/EPROMS to be below 1 μs.

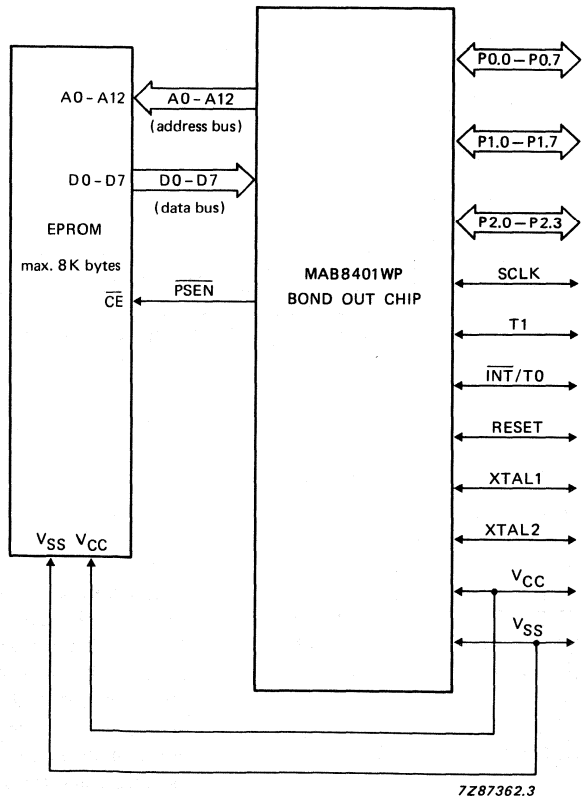


Fig. 2a Connection of EPROM to 'Piggy-back' package MAB8401B.

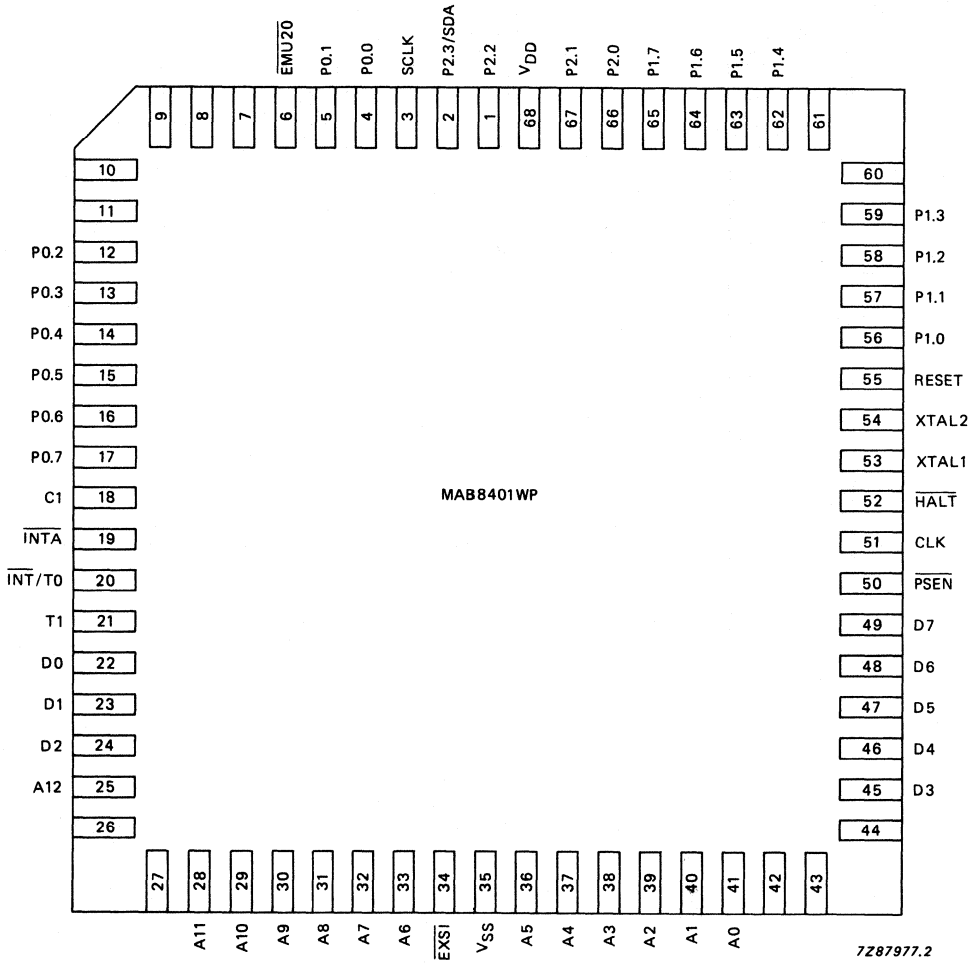


Fig. 3 Pinning diagram; PLCC.

CHIP CARRIER DESIGNATION

designation	pad no.	function
V_{SS}	35	**Ground**
V_{CC}	68	**Power supply,** + 5 V
P0.0 – P0.7	4–5, 12–17	**Port 0,** 8-bit quasi-bidirectional I/O port
P1.0 – P1.7	56–59, 62–65	**Port 1,** 8-bit quasi-bidirectional I/O port with 8-bit LED driver
P2.0 – P2.3	66, 67, 1, 2	**Port 2,** 4-bit quasi-bidirectional I/O port; SDA/P2.3 is the serial data I/O in serial I/O mode
SCLK	3	Bidirectional clock for serial I/O
$\overline{INT}$/T0	20	External interrupt input (sensitive to a negative-going edge), testable using the JT0 or JNT0 instructions

T1	21	Input pin, testable using the JT1 or JNT1 instructions. It can be designated as event counter input using the STRT CNT inctruction. It can also be used to detect zero cross-over of slowly moving a.c. inputs.
RESET	55	Input to initialize the processor (active HIGH)
XTAL1	53	Connection to timing component (e.g. crystal) that determines the frequency of the internal oscillator. It is also the input for an external clock source.
XTAL2	54	Connection to other side of the timing component
$\overline{\text{EXSI}}$	34	External serial I/O interrupt (active-LOW) for emulation of MAB/F8422/42.
A0–A12	41–36, 33–28 25	Program memory address outputs (active HIGH); A0 = LSB, A12 = MSB. Address output change after begin ϕ3 of TS8.
D0–D7	22–24, 45–49	Data input lines (active HIGH) used for reading external program memory. D0 = LSB, D7 = MSB.
CLK	51	Clock output buffered from XTAL2. On the positive-going edge the (internal) ϕ clock goes HIGH.
$\overline{\text{PSEN}}$	50	Program store enable. This signal is used for enabling the external EPROM (e.g. on the 'Piggy-back' version). For emulation, it enables the emulation memory and it indicates machine cycles. Active LOW during TS9,*TS10 of each machine cycle and TS1 of the following machine cycle.
$\overline{\text{C1}}$	18	Cycle 1 indication output (active LOW). During emulation, this signal indicates the opcode fetch cycle (useful for external instruction decoding, real-time trace). Active from start of TS10 of the cycle preceding cycle 1, until the start of TS10 of cycle 1.
$\overline{\text{HALT}}$	52	Halt input (active LOW). If activated, the current instruction is finished and the microcontroller stops execution (HALT mode). The next program counter address is available on the address bus. Program counter and timer/event counter are no longer updated. The serial I/O finishes the current transmit/receive action and goes into the idle state. Interrupts are *not* sampled in the HALT mode, they are only sampled when the microcontroller is running. Interrupt routines can be single-stepped as a normal program.
$\overline{\text{INTA}}$	19	Interrupt acknowledge output (active LOW). It indicates any interrupt acception. Active from start of TS8 of the interrupted cycle, until start of TS7 of the second cycle of the (internally forced 'CALL vector address' instruction. During $\overline{\text{INTA}}$ active, the address bus shows the address that has been saved in the stack (return address); the C1 output indicates opcode fetch cycles as if a user CALL was executed.
$\overline{\text{EMU20}}$	6	Emulate 20-pin version MAB/F8422/42 (active-LOW).

*TS = Time slot, where 10 TS = 1 cycle

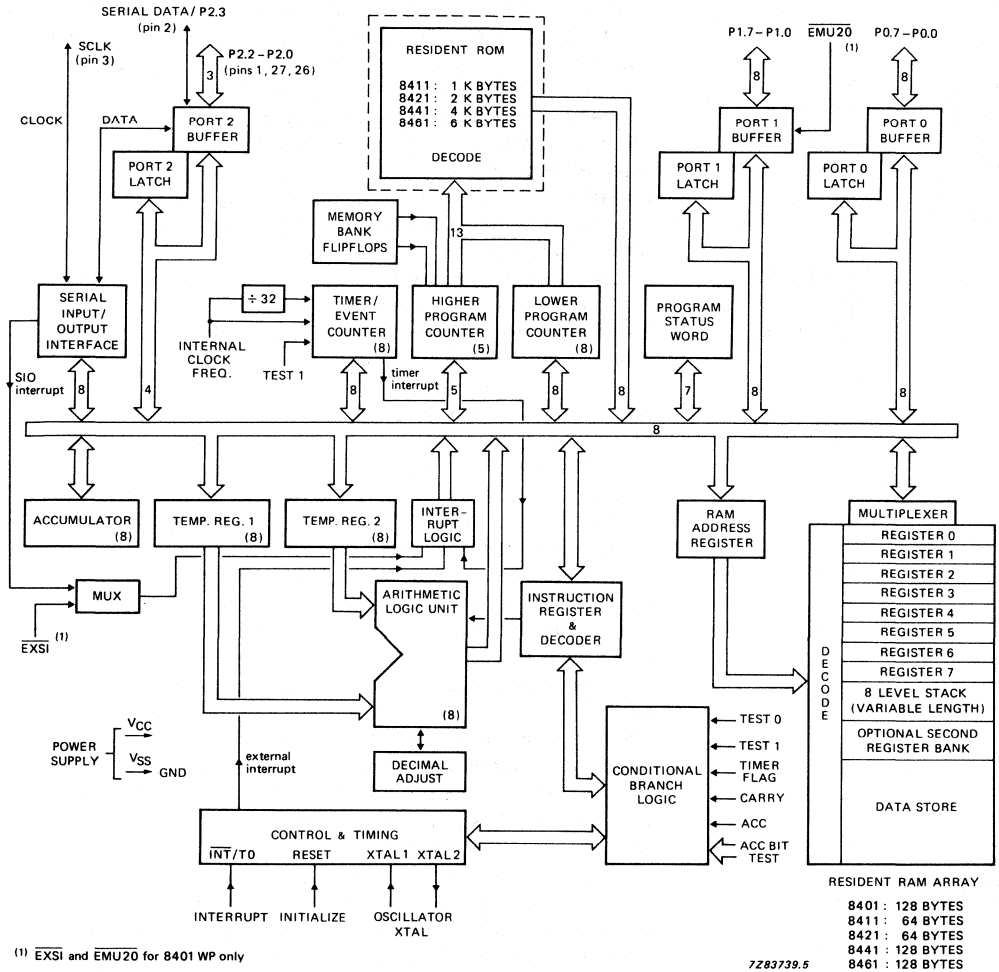


Fig. 4a Block diagram of the MAB84X1 family.

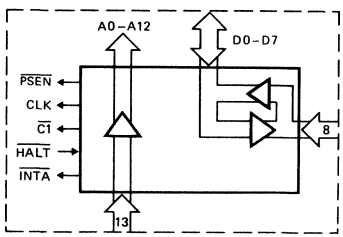


Fig. 4b Replacement for dotted part in Fig. 4a for the MAB8401WP bond-out version.

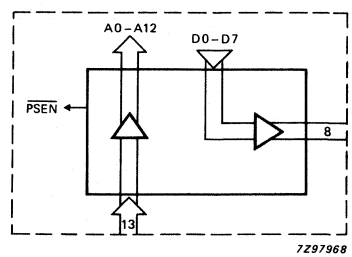


Fig. 4c Replacement of dotted part in Fig. 4a for the MAB8401B 'Piggy-back' version.

FUNCTIONAL DESCRIPTION (for more detail see Microcontroller Users Manual)

Bond-out version MAB8401WP

The bond-out version is a microcontroller that contains no on-board ROM, but has all address and data lines brought out to access an external ROM or EPROM. Thus, this version has more pins than the standard microcontrollers with on-board ROM. It has all the features of the other members of the MAB84X1 family, including emulation facilities for the MAB/F8422/42 (20-pin version). It can address 8K bytes of external ROM. The RAM has 128 bytes.

Piggy-back version MAB8401B

The Piggy-back version is a special package that has standard pinning to the bottom which facilitates insertion as a mask-programmed device. An EPROM is mounted on top in an additional socket. Thus, the total package height is greater than the standard DIL package. Emulation of the 8422/42 is not possible.

Program and data memory

The program memory (ROM) is mask-programmed at our factory. Because the MAB84X1 family offers a range of ROM capacities to suit the application, ROM expansion is not required. Figure 5 shows the program memory map. Program memory is arranged in banks of 2K bytes, that are selected by SEL MB instructions.

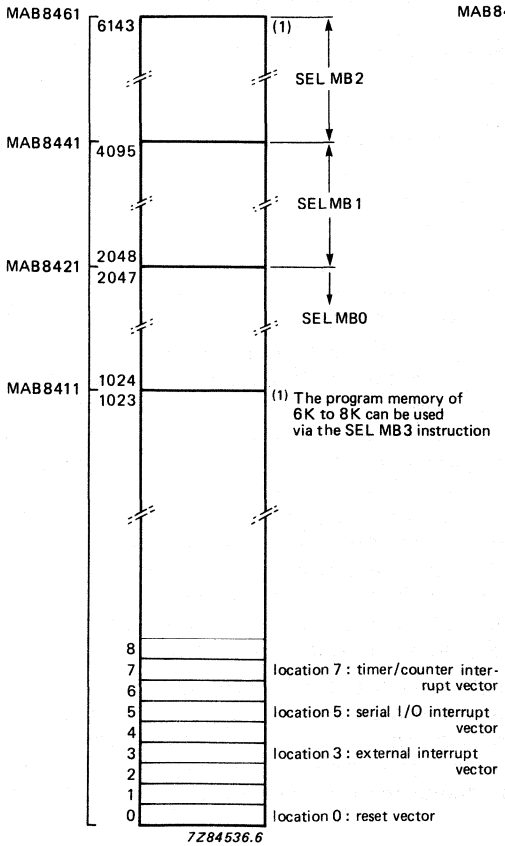


Fig. 5 The program memory map.

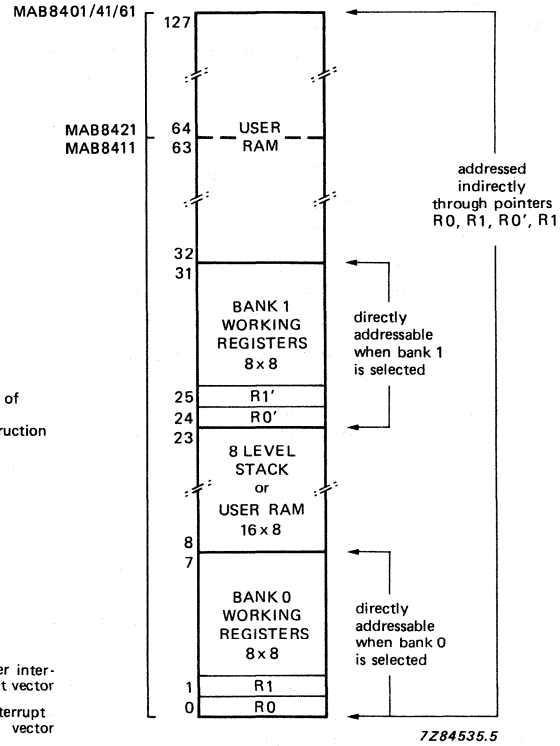


Fig. 6 The data memory map.

FUNCTIONAL DESCRIPTION (continued)

The data memory (RAM) consists of 64 or 128 bytes (8-bit words). All locations are indirectly addressable using RAM pointer registers and up to 16 designated location can be addressed directly. The memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 6 shows the data memory map.

On-chip peripheral functions

In addition to the CPU and memories, an interrupt system, I/O facilities, and an 8-bit timer/event counter are integrated on-chip to assist the CPU in repetitions, complicated or time-critical tasks. The I/O facilities include the I/O pins, parallel ports and a serial I/O port, consisting of a data line SDA shared with a parallel port line (P2.3), and a dedicated clock line SCLK.

I/O facilities

The MAB84XX family has 23 I/O lines arranged as:

- Two parallel ports of 8 lines (P0.0–P0.7, P1.0–P1.7). Each line of Port 1 can sink 10 mA.
- A parallel port of 4 lines (P2.0–P2.3).
- A serial I/O consisting of a data line shared with a parallel port line (P2.3) and a separate clock line SCLK;
- An external interrupt and test input $\overline{\text{INT}}$/T0, which when used as a test input can be tested by the conditional jump instructions JT0 or JNT0;
- A test input T1, which can alter program sequences when tested by conditional jump instructions JT1 or JNT1. T1 can also be used as an input to the timer/event counter or to detect zero cross-over of slowly moving AC signals.

All parallel port lines are available in three optional output configurations (except P2.3 – option 1 only):

- Option 1; open drain output without pull-up transistor (Fig. 7(a))
- Option 2; open drain output with pull-up transistor (Fig. 7(b))
- Option 3; push-pull output with pull-up transistor (Fig. 7(c))

If the inputs and outputs on a port are mixed (mixed-mode), the inputs should be options 1 or 2 but not option 3. This prevents cross-currents via TR2 and an external connection to ground, while switching the output on the same port and in parallel, masking the inputs with logic 1 s.

The MAB84X1 family serial I/O interface has been designed to eliminate the heavy processing load imposed upon a normal microcontroller performing serial data transfer. Whereas a normal microcontroller must regularly monitor the serial data bus for the presence of data, the serial I/O interface detects, receives and converts the serial data stream into a parallel format without interrupting the execution of the current program. An interrupt is sent to the microcontroller only when a complete byte is received. Then, the microcontroller reads the data byte in one instruction. Likewise, for transmission, the serial I/O interface performs parallel to serial conversion and subsequent serial output of the data and the microcontroller is only interrupted in the execution of its programmed tasks when a complete byte has been transmitted. The design of the serial I/O interface allows any number of MAB84X1 family devices and peripheral circuits with I^2C bus compatibility to be interconnected by the two-line serial bus. This is achieved by allocating a specific 7-bit address to each device and ensuring that a device reacts only to a message preceded by its own address or the 'general call' address.

Address recognition is performed by the interface hardware so that the microcontroller need only be interrupted when a valid address is received. This saves significant processing time and memory space compared to a conventional microcontroller with a software serial interface. When the address facility is not required, for instance in a system with only two microcontrollers, direct data transfer is possible. In multi-master systems, an automatically invoked arbitration procedure prevents two or more devices transmitting simultaneously.

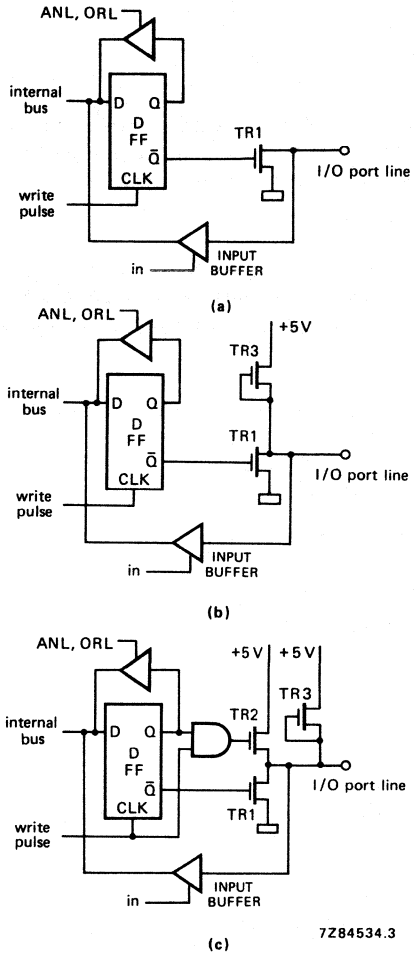


Fig. 7 Quasi-bidirectional I/O interface with (a) open drain output without pull-up transistor, (b) open drain output with pull-up transistor, (c) push-pull output with pull-up transistor.

Serial I/O interface

Figure 8 shows the serial I/O interface. The clock line of the serial bus has exclusive use of pin 3 (SCLK) while the data line shares pin 2 (serial data) with the I/O line P2.3 of port 2. When the serial I/O is enabled, P2.3 is disabled as a parallel port line (P2.3 and SCLK only open drain).

The microcontroller and interface communicate via the internal microcontroller bus and the Serial Interrupt Request line. Data and information controlling the operation of the interface are stored in four registers:

- data shift register S0,
- serial I/O interface status word S1,
- serial clock control word S2,
- address register S0'

FUNCTIONAL DESCRIPTION (continued)

Serial I/O interface (continued)

Data shift register S0

S0 is the shift register that converts serial data to parallel format and vice versa. A pending interrupt is generated only after a complete byte has been transmitted, or after a complete data byte, specific or general call address has been received. The most significant bit is transmitted first.

Serial I/O interface status word S1

S1 provides information about the state of the interface and stores interface control information from the microcontroller. The four most significant bits are common to both read and write instructions, with a separate 4 read-only control bits and 4 write-only interface status bits.

MST and TRX

These bits determine the operating mode of the serial I/O interface (Table 2).

Table 1 Operating modes of the serial I/O interface.

MST	TRX	mode
0	0	slave receiver
1	0	master receiver
0	1	slave transmitter
1	1	master transmitter

BB: Bus Busy

This bit indicates the status of the bus.

PIN: Pending Interrupt Not

PIN = '0' indicates that there is an interrupt pending. This causes a Serial Interrupt Request when the serial interrupt mechanism is enabled.

ESO: Enable Serial Output

The ESO flag enables/disables the serial I/O interface: ESO = logic 1 enables
ESO = logic 0 disables

BC0, BC1 and BC2

These bits indicate the number of bits received or transmitted in a serial data stream.

Bits ES0, BC0, BC1 and BC2 can only be written via software.

AL: Arbitration Lost

The AL flag is set via the hardware when the serial I/O interface, as a master transmitter, loses the bus arbitration procedure.

AAS: Addressed As Slave

This flag is set via the hardware when the interface detects either its own address or the 'general call' address as the first byte of a transfer and if the interface has been programmed to operate in the address recognition mode.

AD0: Address Zero

This flag is set via the hardware after the general call address is detected when the interface is operating in the address recognition mode.

LRB: Last Received Bit

This contains either the last data bit received or, for a transmitting device in the acknowledge mode, the acknowledge from the receiving device.

Bits AL, AAS, AD0 and LRB can only be read via software.

Serial clock control register S2

Bits 0 to 4 of S2 are used to set the frequency of the serial clock signal. When a 4,43 MHz crystal is used, the frequency of the serial clock can be varied between 100 kHz and 720 Hz. An asymmetrical clock with a HIGH to LOW ratio of 3 to 1 is produced by setting bit 5. The asymmetrical clock allows a microcontroller more time per clock period for sampling the data line, making the timing of this action less critical. Bit 6 is used to activate the acknowledge mode of the serial I/O. S2 is a write-only register.

Address register S0'

The address register contains the 7-bit address back-up latches and the bit (ALS) used to enable/disable the address recognition mode. Only when ES0 = 0 can the address register be written using the MOV S0,A and MOV S0,#data instructions.

Serial I/O interrupt logic

The interrupt logic is enabled by the EN SI instruction and disabled by DIS SI. When the interrupt logic is enabled, a pending interrupt results in a serial I/O interrupt to the controller, causing a jump to location 5 in the ROM. When the logic is disabled, the presence of an interrupt is still indicated by the PIN bit in register S1. Therefore, an interrupt can still be serviced but a vectored interrupt will not occur.

Interrupt system

External events and real-time on-chip peripherals require servicing by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution, three single-level nested interrupts are provided.

Each interrupt vectors to a separate location in the program memory for its service program. Each source can be individually enabled or disabled. When more than one interrupt occurs simultaneously, their priority will be: (1) external, (2) serial I/O and, (3) timer/event counter. An additional external interrupt can be created using the timer/event counter interrupt.

FUNCTIONAL DESCRIPTION (continued)

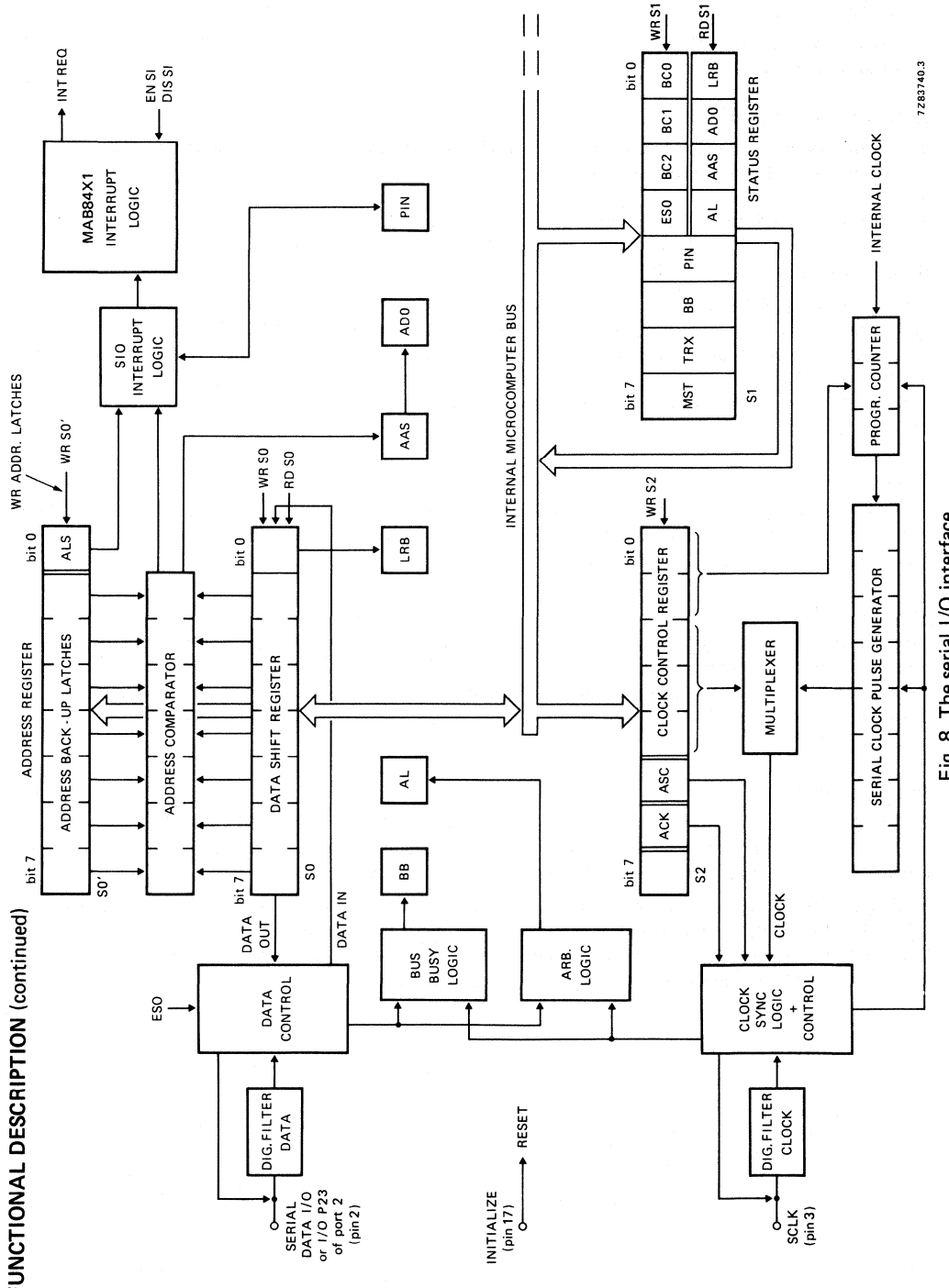


Fig. 8 The serial I/O interface.

Test input T1

The T1 input line can be used as:

- a test input for branch instructions,
- an input for zero voltage cross-over detection,
- an external input to the event counter.

An internal pull-up transistor is provided as a ROM mask option. This is useful when the input is from a switch or standard TTL output.

When T1 is used as a test input, the JT1 or JNT1 instructions test for a HIGH or a LOW respectively.

When used for zero-cross detection purposes, the T1 input must be coupled through a capacitor of typical value 1 μF and operation carried out using the T1 input without the pull-up transistor. The maximum input voltage amplitude is 3 V (peak-to-peak), with a maximum operational frequency of 1 kHz. The T1 input has an on-chip DC offset circuit which self-biases the input to its exact switching level of 1 V. As a consequence a small change will cause a digital transition to occur. The switching level of the T1 input circuit is within the bias voltage of ± 135 mV. Upon each positive cycle on the pin, the event counter is incremented and an overflow will set the timer flag TF. Zero cross-over detection used in conjunction with the timer/event counter interrupt, is useful in thyristor control of power equipment. Figure 9 illustrates, (a) the input waveform, (b) the input diagram and (c) the on-chip self-stabilized bias.

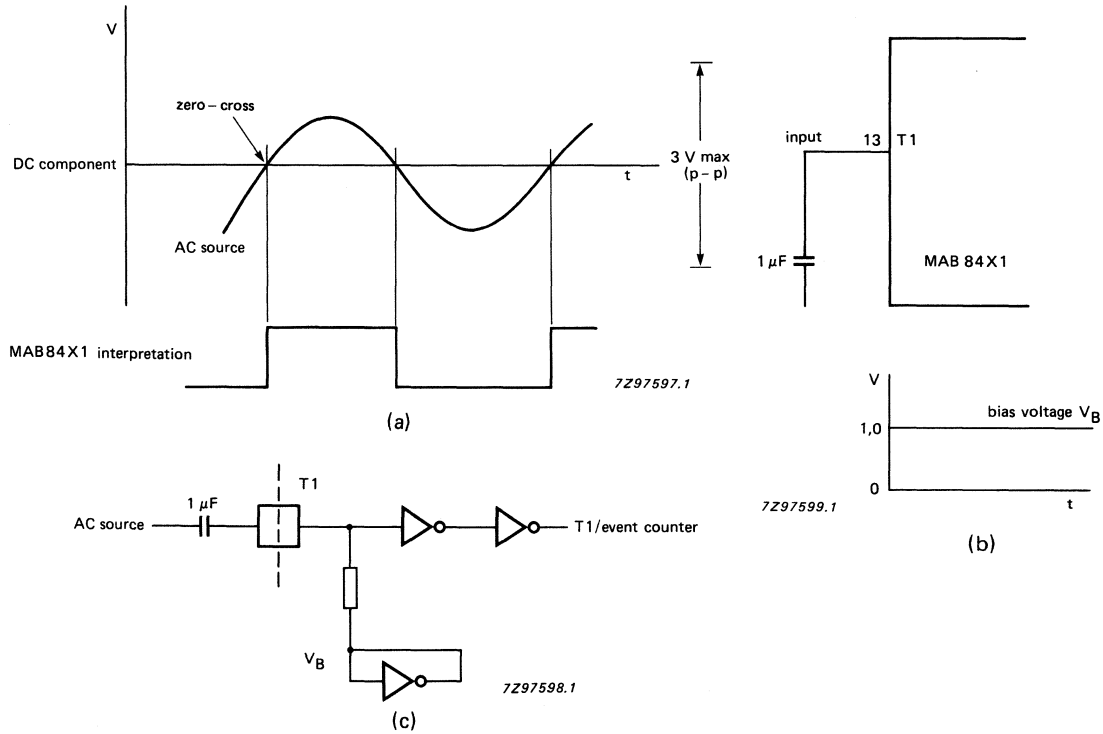


Figure 9 Zero-cross detection circuitry; (a) input waveform, (b) input diagram, (c) on-chip self-stabilized bias.

The operation of T1 as an input to the timer/event counter is described under the heading Timer/event counter.

High current outputs

Ten pins are provided that can sink high currents:

– P2.3 (serial data), pin 2	5 mA at 0,45 V (open drain),
– SCLK, pin 3	5 mA at 0,45 V (open drain),
– P1.0 – P1.7 *	10 mA at 1 V

* P1.0 to P1.7 may be connected in parallel if their logic outputs are always the same.

FUNCTIONAL DESCRIPTION (continued)

Timer/event counter

An 8-bit binary up-counter is provided. This can count external events, machine cycles divided by 32, or machine cycles directly. When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW to HIGH transitions on T1 (pin 13) are counted. The maximum rate at which the counter may be incremented is once every machine cycle (200 kHz for a 5 μs machine cycle). Figure 10 illustrates the timer/event counter.

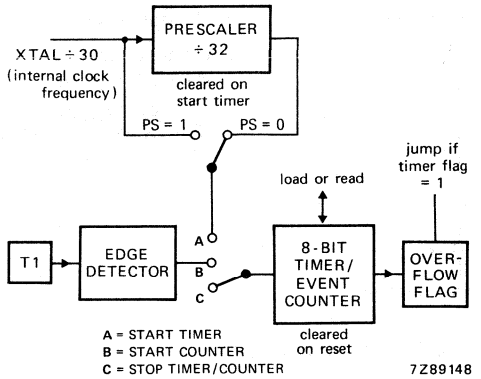


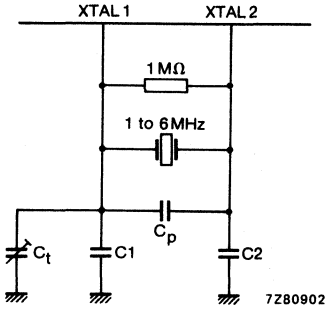
Fig. 10 The timer/event counter.

Differences between the MAB8021 and MAB8048 microcontrollers, and the MAB84X1 family.

	8021	8048	8401, 8411 8421, 8441, 8461
ROM capacity (bytes)	1K	1K	ROMless, 1K, 2K, 4K, 6K
RAM capacity (bytes)	64	64	128, 64, 64, 128, 128
paralel I/O lines	8 + 8 + 4	8 + 8 + 8	8 + 8 + 4
single inputs	1	3	2
serial I/O	no	no	yes, 2-line multi-transmitter
timer	8 bit	8 bit	8 bit
prescaler	mod. 32	mod. 32	mod. 1 & mod. 32
machine cycle time (μs)	10	2,5	5
for clock (MHz)	3	6	6
instruction set	8021	8048	8048 with omissions; 5 new serial I/O instructions; 2 new register instructions; 2 new control instructions; 1 new cond. branch instruction
interrupts	none	2 external timer/ event counter	3 external serial I/O timer/event counter
no. of pins (DIL)	28	40	68 (PLCC), 28

OSCILLATOR CIRCUITRY

Clock frequency is determined by using the internal oscillator or by connecting an external clock to XTAL1. Where the internal oscillator is used, the frequency is set by a crystal between XTAL1 and XTAL2, or by a ceramic resonator or an inductor, each with two associated capacitors, between XTAL1 and XTAL2 (see Fig. 11a). A machine cycle consists of 10 states, each state being 3 oscillator periods. The common 6 MHz crystal gives a 5 μs machine cycle. The MAB84X1 family has dynamic logic, and therefore, for adequate refreshing the oscillator frequency must be at least 1 MHz.



1. Crystal – AT-cut
2. Ceramic resonator
   C1 = C2 = 27 pF
   C1 may be trimmed
   $C_p \leqslant 6{,}75$ pF (parasitic capacitance)

Fig. 11a Quartz crystal or ceramic resonator mode.

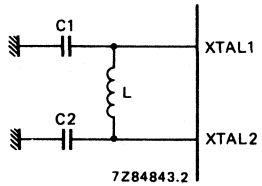


Fig. 11b LC pi-network.

LC oscillator timing

frequency	C1 = C2	L
3,0 MHz	33 pF	100 μH
4,0 MHz	33 pF	56 μH
4,4 MHz	33 pF	47 μH
5,0 MHz	33 pF	33 μH
6,0 MHz	33 pF	22 μH

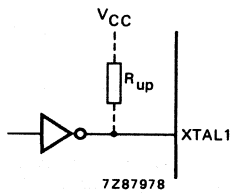


Fig. 11c External drive.

Drive XTAL1
Leave XTAL2 open

Driver may be high-speed CMOS or any TTL
t_r, $t_f < 10$ ns

PROGRAM STATUS WORD

The program status word (PSW) is an 8-bit word in the CPU which stores information about the current status of the microcontroller (Fig. 12). The PSW bits are:

bits 0, 1 and 2 – stack pointer bits (SP_0, SP_1, SP_2);

bit 3 – prescaler select (PS); 0 = divide-by-32; 1 = no prescaling;

bit 4 – working register bank select (RBS):
0 = register bank 0
1 = register bank 1;

bit 5 – not used (1);

bit 6 – auxiliary carry (AC):
half-carry bit is generated by an ADD instruction and used by the decimal adjust instruction DA A;

bit 7 – carry (CY):
the carry flag indicates that the previous operation has resulted in an overflow of the accumulator.

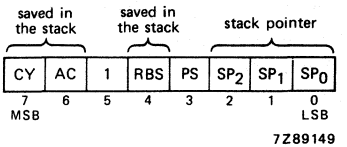


Fig. 12 Program status word.

All bits can be read using MOV A, PSW and bit 3 can be written with MOV PSW, A.

Bits 6 and 7 can be set and cleared by CPU operation. Bit 4 is changed by the SEL RB instruction, bit 3 by the MOV PSW,A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions and when an interrupt occurs. Bits 4, 6 and 7 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored to the PSW with RETR (return and restore) instruction.

Note: The RET instruction has no restore feature and should not be used at the end of an interrupt because this would leave any further interrupts disabled.

The MAB84X1 family has arithmetic, logical and branching capabilities. The DA A, SWAP A, and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look up from the current ROM page.

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program. Table 2 lists the conditional branch instructions used to change the program execution sequence. The DJNZ instruction decrements a designated register and branches if the contents are not zero. This instruction makes the register an efficient program loop counter. The JMPP @A instruction allows multiway branches to destinations indirectly addressed by the contents of the accumulator.

Table 2 Conditional branches

TEST	JUMP CONDITION	JUMP INSTRUCTION
accumulator	0 or non-zero	JZ, JNZ
accumulator bit test	1	JB0 to JB7
carry flag	0 or 1	JNC, JC
timer overflow flag	1	JTF
test input $\overline{INT}$	0 or 1	JNT0, JT0
test input T1	0 or 1	JNT1, JT1
test flag 0	1	JF0
test flag 1	1	JF1
register	non-zero	DJNZ

RESET

A positive-going signal on the RESET input:

- sets the program counter to zero,
- selects location 0 of memory bank 0, and register bank 0,
- sets the stack pointer to zero ('000'B); pointing to RAM address 8,
- disable the interrupts (external, timer and serial I/O),
- stops the timer/event counter, then sets it to zero,
- sets the timer prescaler to divide-by-32,
- resets the timer flag,
- sets all ports to logic '1' (input mode),
- sets the serial I/O to slave receiver mode and disables serial I/O.

Automatic reset at power-up may be obtained by connecting the RESET pin to V_{CC} through a 1 μF capacitor C, together with a diode to V_{SS} (cathode to RESET pin). This arrangement is satisfactory, if both the voltage (V_{CC}) rise time and the oscillator start-up time do not exceed either 1 or 10 ms respectively.

The power-on reset circuit is shown in figure 13. At power-on the current drawn by RESET commences to charge the capacitor C. The difference between this increasing capacitor voltage and V_{CC} is known as V_{RESET}. The charging circuit is designed to hold V_{RESET} above the lower threshold of a Schmitt trigger arrangement long enough to effect a complete reset. The minimum time required; is the oscillator start-up time plus two machine cycles.

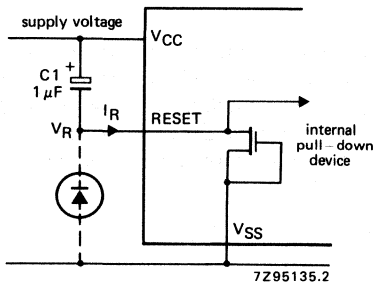


Fig. 13 Typical power-on reset circuitry.

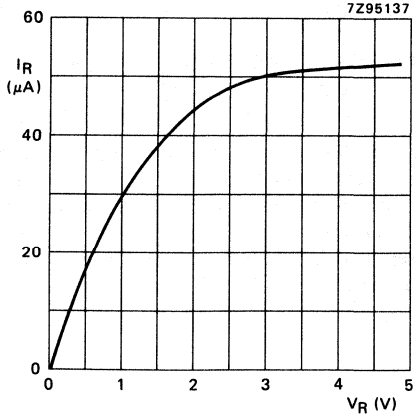


Fig. 14 Power-on reset input characteristics (typical).

INSTRUCTION SET

The instruction set consists of over 80 one and two byte instructions and is based on the MAB8048 instruction set. New instructions include those for serial I/O operation and memory bank selection. Program code efficiency is high because all ROM locations on a 256 byte page require only a single byte address.

Table 3 gives the instruction set of the MAB84X1 family and Table 4 shows the instruction map. The following symbols and abbreviations are used.

Note: During development of software on a PMDS or similar system, it is important to ensure that no jump instruction (direct or indirect), outreaches the final address range of the device.

symbol	description
A	the accumulator
AC	the auxiliary carry flag
addr	program memory address (11-bits)
Bb	bit designation (b = 0–7)
BS	the bank switch
C	carry flag
CLK	clock signal
CNT	event counter
D	nibble designation (4-bits)
DBF	program memory bank flip-flop
data	number or expression (8-bits)
F0, F1	flags 0 and 1
I	interrupt
$\overline{\text{INT}}$	external interrupt
P	'in-page' operation designation
Pp	port designation (p = 1, 2 or 4–7)
PSW	program status word
Rr	register designation (r = 0, 1 or 0–7)
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
$	current value of program counter
←	is replaced by
↔	is exchanged with

Table 3 MAB84XX family instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) – 1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1})\leftarrow A_n$ $(A_0)\leftarrow(C)$, $(C)\leftarrow(A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(C)$, $(C)\leftarrow(A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7})\leftrightarrow(A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data		
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3})\leftrightarrow((R0_{0-3}))$ $(A_{0-3})\leftrightarrow((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3)\leftarrow(A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7})\leftarrow(A)$, $(A)\leftarrow((PC))$		

FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1	r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1		
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1	r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1		
BRANCH	JMP addr	● 4 address	2/2	unconditional jump within a 2K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1		
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))		
	DJNZ Rr, addr	E* address	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 if (Rr) not zero (PC_{0-7})←addr	r = 0–7	
	DJNZ @Rr, addr	E0 address	2/2	decrement RAM data, addressed by Rr, by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr		
		E1 address			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr		
	JBb addr	▲ 2 address	2/2	jump to addr if Acc. bit b = 1	if b = 1: (PC_{0-7})←addr	b = 0–7	
	JC addr	F6 address	2/2	jump to addr if C = 1	if C = 1: (PC_{0-7})←addr		
	JNC addr	E6 address	2/2	jump to addr if C = 0	if C = 0: (PC_{0-7})←addr		
	JZ addr	C6 address	2/2	jump to addr if A = 0	if A = 0: (PC_{0-7})←addr		
	JNZ addr	96 address	2/2	jump to addr if A is NOT zero	if A≠0: (PC_{0-7})←addr		
	JT0 addr	36 address	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr		
	JNT0 addr	26 address	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr		
	JT1 addr	56 address	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr		
	JNT1 addr	46 address	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr		
	JTF addr	16 address	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr		4
	JNTF addr	06 address	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr		

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
SUBROUTINE	CALL addr	▲ 4 address	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4, 6, 7}$) (SP)←(SP) + 1 (PC_{9-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) – 1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) – 1 ($PSW_{4, 6, 7}$) + (PC)←((SP))	6

PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 data 99 data 9A data	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 data 89 data 8A data	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
	OUTL PO,A	90	1/2	Output accumulator data to port ϕ	(P0)←(A)	9
SERIAL INPUT/OUTPUT	MOV A, S_n	0C 0D	1/2	move serial I/O register contents to accumulator	(A)←(S0) (A)←(S1)	8
	MOV S_n, A	3C 3D 3E	1/2	move accumulator contents to serial I/O register	(S0)←(A) (S1)←(A) (S2)←(A)	
	MOV S_n, #data	9C data 9D data 9E data	2/2	move immeidate date to serial I/O register	(S0)←data (S1)←data (S2)←data	
	EN SI	85	1/1	enable serial I/O interrupt		
	DIS SI	95	1/1	disable serial I/O interrupt		
	NOP	00	1/1	no operation		

Notes to Table 3.

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF).
5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 1111 P2.3, P2.2, P2,1, P2,0.
8. (S1) has a different meaning for read and write operation, see serial I/O interface.
9. Only for software-transfer from the MAB8021.

* : 8, 9, A, B, C, D, E, F
● : 0, 2, 4, 6, 8, A, C, E
▲ : 1, 3, 5, 7, 9, B, D, F

Table 4 MAB84X1 family instruction set

first hexadecimal chracter of opcode ↓ / second hexadecimal chracter of opcode →

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP			ADD A, # data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0	1	2		0	MOV A,Sn 1		
1	INC @Rr 0	1	JB0 addr	ADDC A, # data	CALL page 0	DIS I	JTF addr	INC A	0	1	2	INC Rr 3	4	5	6	7
2	XCH A, @Rr 0	1		MOV A, # data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	0	1	2	XCH A,Rr 3	4	5	6	7
3	XCHD A, @Rr 0	1	JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	OUTL Pp,A 0	1	2		0	MOV Sn,A 1	2	
4	ORL A, @Rr 0	1	MOV A, T	ORL A, # data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	0	1	2	ORL A,Rr 3	4	5	6	7
5	ANL A, @Rr 0	1	JB2 addr	ANL A, # data	CALL page 2	STRT T	JT1 addr	DA A	0	1	2	ANL A,Rr 3	4	5	6	7
6	ADD A, @Rr 0	1	MOV T, A		JMP page 3	STOP TCNT		RRC A	0	1	2	ADD A,Rr 3	4	5	6	7
7	ADDC A, @Rr 0	1	JB3 addr		CALL page 3			RR A	0	1	2	ADDC A,Rr 3	4	5	6	7
8				RET	JMP page 4	EN SI			ORL Pp, # data 0	1	2					
9	OUTL PO, A		JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp, # data 0	1	2		0	MOV Sn, # data 1	2	
A	MOV @Rr, A 0	1		MOVP A, @A	JMP page 5	SEL MB2		CPL C	0	1	2	MOV Rr, A 3	4	5	6	7
B	MOV @Rr, # data 0	1	JB5 addr	JMPP @A	CALL page 5	SEL MB3			0	1	2	MOV Rr, # data 3	4	5	6	7
C	DEC @Rr 0	1			JMP page 6	SEL RB0	JZ addr	MOV A, PSW	0	1	2	DEC Rr 3	4	5	6	7
D	XRL A, @Rr 0	1	JB6 addr	XRL A, # data	CALL page 6	SEL RB1		MOV PSW, A	0	1	2	XRL A, Rr 3	4	5	6	7
E	DJNZ @Rr, addr 0	1			JMP page 7	SEL MB0	JNC addr	RL A	0	1	2	DJNZ Rr, addr 3	4	5	6	7
F	MOV A, @Rr 0	1	JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	0	1	2	MOV A, Rr 3	4	5	6	7

Table 5 shows the additional MAB84X1 family instructions (including the five for serial I/O operation) that are not part of the MAB8048 instruction set.

Table 5 MAB84X1 family instructions not in the MAB8048 instruction set

serial I/O	register	control	conditional branch

MOV A, S_n
MOV S_n, A
MOV S_n, #data
EN SI
DIS SI
	DEC @Rr
	DJNZ @Rr, addr
		SEL MB2
		SEL MB3
			JNTF addr

Table 6 shows the MAB8048 instructions omitted from the MAB84X1 family instruction set.

Table 6 MAB8048 instructions not in the MAB84X1 family instruction set

data moves	flags	branch	control

MOVX A, @R
MOVX @R, A
MOVP3 A, @A
MOVD A, P
MOVD P, A
ANLD P, A
ORLD P, A
	CLR F0
	CPL F0
	CLR F1
	CPL F1
		* JNI addr
		JF0 addr
		JF1 addr
		
		* replaced by
		JT0 JNT0.
			ENT0 CLK

ABSOLUTE MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Stress above those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device, at these, or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

parameter	symbol	min.	max.	unit
Input voltage on any pin with respect to ground (V_{SS})	V_I	−0,5	+7	V
Total power dissipation				
SOT-117, 28-lead DIL	P_{tot}	–	1	W
SOT-136, 28-lead DIL	P_{tot}	–	0,6	W
Input/output current for all pins except port 1	I_I, I_O	–	10	mA
Input/output current for port 1	I_I, I_O	–	20	mA
Storage temperature	T_{stg}	−65	+150	°C
Operating temperature				
standard	T_{amb}	0	+70	°C
extended	T_{amb}	−40	+85	°C
automotive	T_{amb}	−40	+110	°C

DC CHARACTERISTICS

V_{CC} = 5 V (10%); V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified

parameter	conditions	symbol	min.	max.	unit
Supply current					
MAB	0 to + 70 °C	I_{CC}	–	85	mA
MAF	–40 to + 85 °C	I_{CC}	–	100	mA
MAF84A	–40 to + 110 °C	I_{CC}	–	100	mA
Inputs					
Input voltage LOW (except P2.3 and SCLK)		V_{IL}	–0,5	0,8	V
Input voltage LOW (P2.3 and SCLK)		V_{IL1}	–0,5	1,5	V
Input voltage HIGH (all inputs except XTAL1, P2.3 and SCLK)		V_{IH}	2	V_{CC} + 0,5	V
Input voltage HIGH (XTAL1, P2,3 and SCLK)		V_{IH1}	3,0	V_{CC} + 0,5	V
Outputs					
Output voltage LOW (P0.0–P0.7)	I_{OL} = 1,6 mA	V_{OL}	–	0,45	V
Output voltage LOW (P1.0–P1.7 for 8401/11/21/41/61)	I_{OL12} = 10 mA	V_{OL12}	–	1,0	V
Output voltage LOW (P2.0–P2.2)	I_{OL2} = 1,6 mA	V_{OL2}	–	0,45	V
Output voltage LOW (P2.3, SCLK)	I_{OL3} = 5 mA	V_{OL3}	–	0,45	V
Output voltage LOW (non-standard pins of bond-out versions)	I_{OL4} = 0,4 mA	V_{OL4}	–	0,45	V
Output voltage HIGH (all outputs unless open drain)	I_{OH} = –50 μA	V_{OH}	2,4	–	V
Output leakage current	$V_{SS} < V_I < V_{CC}$	± I_{OL}	–	10	μA

AC CHARACTERISTICS (all versions except bond-out)

V_{CC} = 5 V ± 10%; V_{SS} = 0 V.

parameter	symbol		min.	max.	unit
Frequency	f_{XTAL}	MAB/MAF84X1	1	6	MHz
		MAF84AX1	1	5	MHz
Cycle time	t_{CY}	MAB/MAF84X1	5	30	μs
		MAF84AX1	6	30	μs

AC CHARACTERISTICS (bond-out versions)

V_{CC} = 5 V ± 10%; V_{SS} = 0 V.

parameter	symbol	min.	max.	unit
f_{CL} = 6 MHz				
Control pulse duration $\overline{PSEN}$ (9CP)	t_{CC}	1,5	9	μs
Address to $\overline{PSEN}$ L set-up (1CP)	t_{AS}	167	–	ns
Data to $\overline{PSEN}$ H set-up (1CP + 120 ns)	t_{DS}	600	–	ns
Data hold time	t_{DR}	0	–	ns
Address to data-in (10CP–t_{DS})	t_{AD}	–	1,07	μs
Time from $\overline{PSEN}$ L to C1 (3CP)	t_{PC}	500	–	ns
Time from $\overline{INTA}$ L to $\overline{PSEN}$ (3CP)	t_{IP0}	500	–	ns
Time from $\overline{INTA}$ H to $\overline{PSEN}$ (6CP)	t_{IP1}	1	–	μs
$\overline{HALT}$ set-up to $\overline{PSEN}$ (15CP)	t_{HS}	2,5	–	μs
$\overline{HALT}$ hold time from $\overline{PSEN}$ (3CP)	t_{HH}	500	–	ns

Note: CP = clock pulse.

T1 ZERO-CROSS CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{CC} = 5 V ± 10%, V_{SS} = 0 V; C_L = 80 pF

parameter	conditions	symbol	min.	max.	unit
Zero-cross detection input (T1) peak-topeak	AC coupled, C = 1,0 μF	$V_{ZX(p-p)}$	1	3	V
Zero-cross accuracy	50 Hz sine wave	A_{ZX}	–	± 135	mV
Zero-cross detection input frequency (T1)		F_{ZX}	0,05	1	kHz

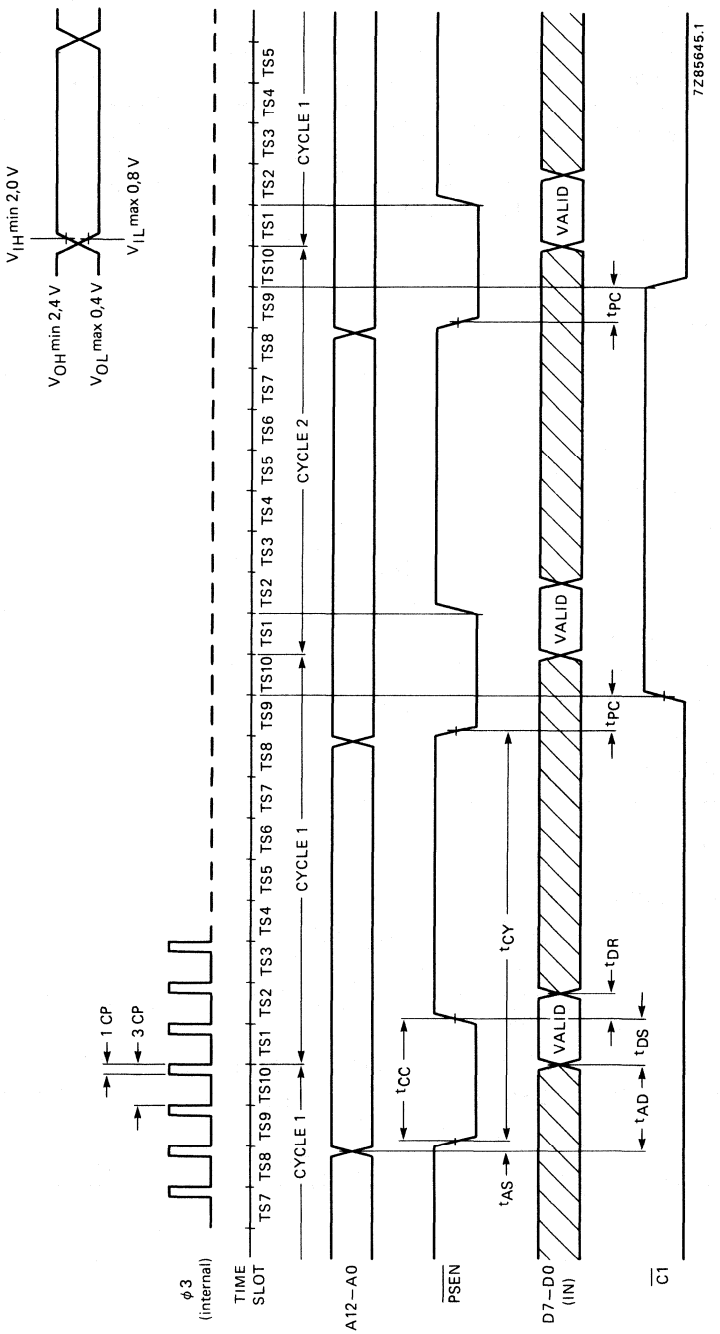


Fig. 15 Memory access timing MAB8401B/WP and I/O voltage parameters.

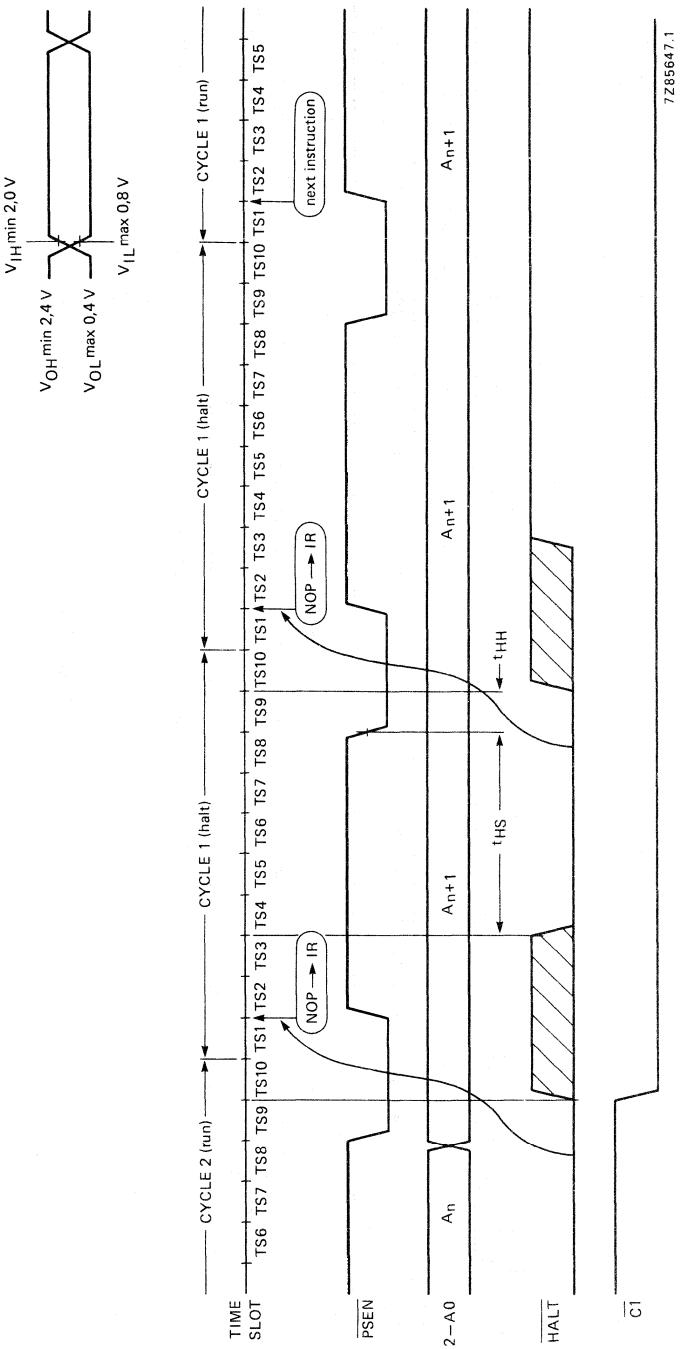


Fig. 16 $\overline{HALT}$ timing MAB8401WP and I/O voltage parameters.

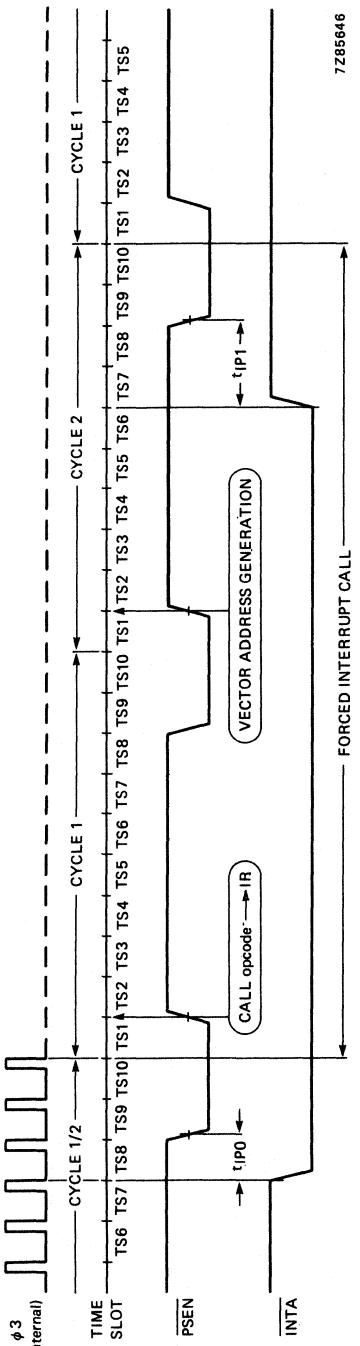


Fig. 17 $\overline{\text{INTA}}$ timing MAB8401WP.

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

The MAB8422/8442 is a high-performance microcontroller incorporating dedicated hardware, memory capacity and I/O lines. This dedication means a microcontroller can be economically installed in high-volume products where its main function is control.

The MAB8422/8442 is a 20 pin, single-chip 8-bit microcontroller that has been developed from the 28 pin MAB8421/8441 microcontrollers. The versions are:

- MAB8422 - 2K x 8 ROM/64 bytes RAM
- MAB8442 - 4K x 8 ROM/128 bytes RAM

Each version has 15 I/O port lines comprising one 8-bit parallel port (P0), one 2-bit parallel port (P1.0 and P1.1 that are shared with the serial I/O lines SDA and SCL), one 3-bit parallel port (P2.0 - P2.2) and two input lines ($\overline{INT}$/T0 and T1).

The serial I/O interface is I^2C compatible and therefore the MAB8422/8442 can operate as a slave or a master in single and multi-master systems. Conversion from parallel to serial data when transmitting, and vice versa when receiving, is done mainly in software. There is a minimum of hardware for the serial I/O implemented. This hardware is controlled by the status of the SDA and SCL lines and can be read or written under software control. Standard software for I^2C-bus control is available upon request. For detailed information see the user manual 'Single-chip 8-bit microcontrollers'.

Features

- 8-bit: CPU, ROM, RAM and i/O
- 20 pin package
- MAB8422: 2K x 8 ROM/64 bytes RAM
- MAB8442: 4K x 8 ROM/128 bytes RAM
- 13 quasi-bidirectional I/O port lines
- Two testable inputs T1 and $\overline{INT}$/T0
- High current output on P0 (I_{OL} = 10 mA at V_{OL} = 1 V)
- One interrupt line combined with the testable input line $\overline{INT}$/T0
- Single-level interrupts: external, timer/event counter, serial I/O
- I^2C-compatible serial I/O that can be used in single or multi-master systems (serial I/O data and clock via P1.0 and P1.1 port lines, respectively)
- 8-bit programmable timer/event counter
- Internal oscillator, generated with inductor, crystal, ceramic resonator or external source
- Over 80 instructions (based on MAB8048)
- All instructions 1 or 2 cycles, cycle time dependent on oscillator frequency
- Single power supply
- Operating temperature ranges: 0 to +70 °C (MAB84X2)
  −40 to +85 °C (MAF84X2)
  −40 to +110 °C (MAF84AX2)

PACKAGE OUTLINES

MAB/MAF84X2, MAF84AX2: 20-lead DIL; plastic (SOT-146).

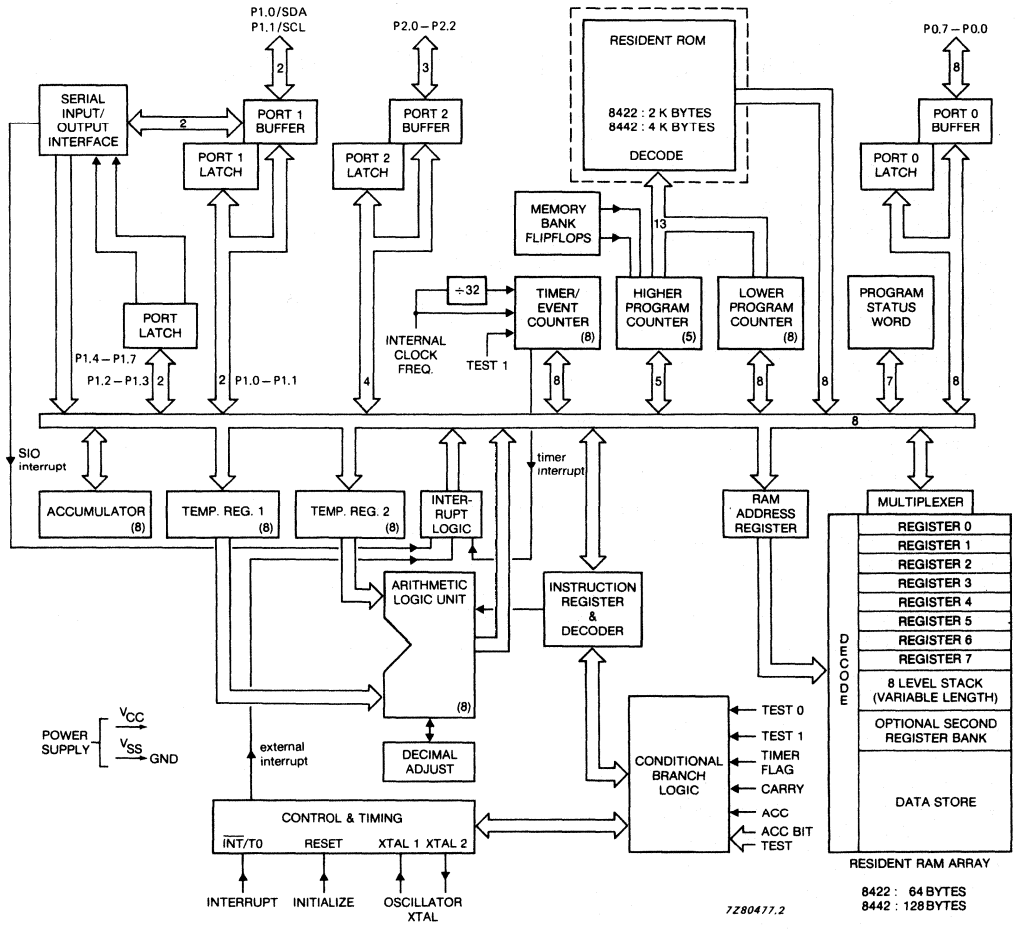


Fig. 1 Block diagram of the MAB8422/8442.

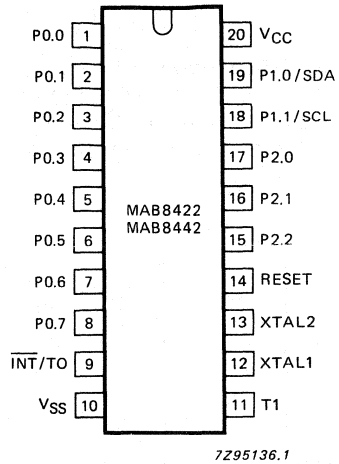


Fig. 2 Pinning diagram.

PINNING

Designation	Pin number	Function
P0.0 - P0.7	1-8	8-bit quasi-bidirectional I/O port (Port 0 high current output).
$\overline{INT}$/T0	9	External interrupt input (sensitive to a negative going edge) and/or input, testable using the JT0 or JNT0 instructions.
V_{SS}	10	Ground.
T1	11	Input pin, testable using the JT1 or JNT1 instructions. It can be designated as event counter input using the STRT CNT instruction. It can also be used to detect zero cross-over of slowly moving a.c. inputs.
XTAL1	12	Connection to timing component that determines the frequency of the internal oscillator. It is also the input for an external clock source.
XTAL2	13	Connection to the other side of the timing component.
RESET	14	Input to initialize the processor (active HIGH).
P2.0-P2.2	17-15	Quasi-bidirectional port.
P1.1/SCL	18	Quasi-bidirectional port in parallel port mode. Serial clock in serial I/O mode.
P1.0/SDA	19	Quasi-bidirectional port in parallel port mode. Serial data I/O in serial I/O mode.
V_{CC}	20	Power supply.

FUNCTIONAL DESCRIPTION

Program and data memory

The non-volatile program memory (ROM), as shown in Fig. 3, is arranged in two banks of 2K bytes, that are selected by SEL MB instructions, and each bank is further divided into 256-byte pages. Only the unconditional jump instructions (JMP and CALL) can be used to cross page boundaries. Memory bank boundaries can also be crossed using these instructions provided that the appropriate memory bank has been selected.

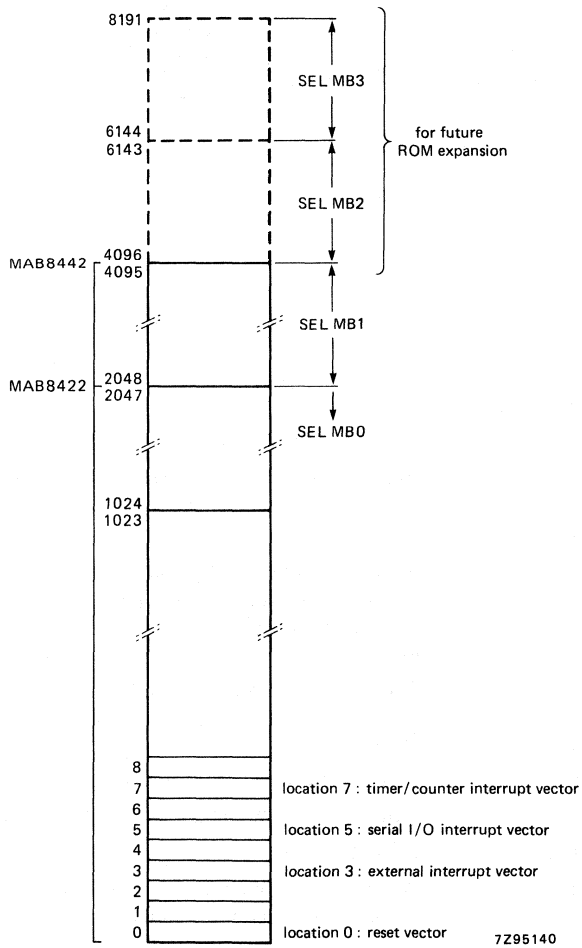


Fig. 3 Program memory map.

In the volatile data memory (RAM), all locations are indirectly addressable using RAM pointer registers and up to 16 designated locations can be addressed directly. The memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer and two register banks, each with 8 registers. The data memory is shown in Fig. 4.

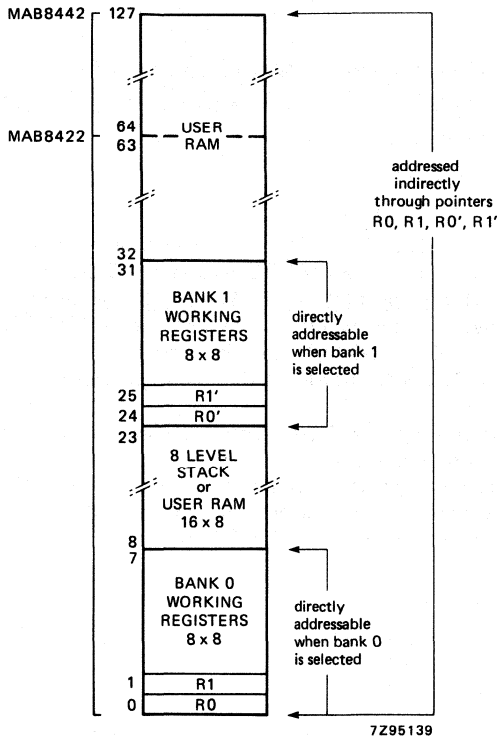


Fig. 4 Data memory map.

Instruction set

The instruction set consists of over 80 one and two byte instructions. It is identical to the MAB84X1 instruction set except that the instructions MOV Sn, A, MOV A, Sn and MOV Sn, #data are not used. Program code efficiency is high because all RAM locations on a 256 byte page require only a single byte address.

On-chip peripheral functions

In addition to the CPU and memories, an interrupt system, I/O facilities, and an 8-bit timer/event counter are integrated on-chip to assist the CPU in repetitious, complicated or time-critical tasks. The I/O facilities include the I/O pins, parallel ports and a serial I/O port sharing the two pins of the parallel port P1.

FUNCTIONAL DESCRIPTION (continued)

I/O facilities (see Fig. 5)

The MAB8422/8442 has 13 I/O lines and 2 testable inputs arranged as:

- An 8 line parallel port P0.0-P0.7, high current outputs with three optional output configurations:
  - A push-pull output with pull-up (Fig. 5 (a))
  - Open drain with pull-up (Fig. 5 (b))
  - Open drain without pull-up (Fig. 5 (c))
- A 2 line parallel/serial port P1.0/SDA and P1.1/SCL, open-drain without pull-up, as output configuration. Schmitt-trigger input. After RESET, P1.0/SDA and P1.1/SCL will be in the parallel port mode. To stay in this mode the internal port latches, P1.4 and P1.3 must be kept in the logic '1' state. Inputs P1.2-P1.7 are not valid in the parallel port mode. After a RESET, the microcontroller remains in the parallel port mode until the serial I/O mode is enabled.
- A 3 line parallel port P2.0-P2.2 with the same output configurations as P0.0-P0.7 but without high-current output;
- An external interrupt and test input INT/T0, which when used as a test input can be tested by the conditional jump instructions JT0 and JNT0;
- A test input T1, tested by the conditional jump instructions JT1 and JNT1. T1 can also be used as an input to the timer/event counter or to detect zero cross-over of slowly moving AC signals. This test or input line can be ordered with port option 5(b) or 5(c).

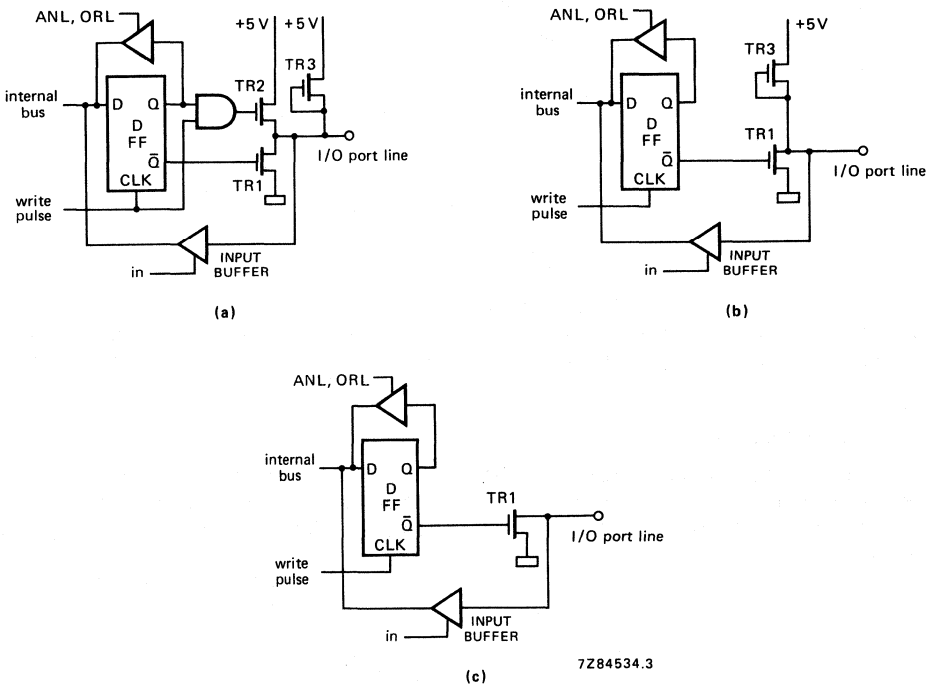


Fig. 5 Port option configurations.

Test input T1

The T1 input line can be used as:

- a test input for branch instructions,
- an input for zero voltage cross-over detection,
- an external input to the event counter.

An internal pull-up transistor is provided as a ROM mask option. This is useful when the input is from a switch or standard TTL output.

When T1 is used as a test input, the JT1 or JNT1 instructions test for a HIGH or a LOW respectively.

Zero cross-over detection

When used for zero-cross detection purposes, the T1 input must be coupled through a capacitor of typical value 1 μF and operation carried out using the T1 input without the pull-up transistor. The maximum input voltage amplitude is 3 V (peak-to-peak), with a maximum operational frequency of 1 kHz. The T1 input has an on-chip DC offset circuit which self-biases the input near to its exact switching level of 1 V. As a consequence a small change will cause a digital transition to occur. The switching level of the T1 input circuit is within the bias voltage of ±135 mV. Upon each positive cycle on the pin, the event counter is incremented and an overflow will set the timer flag TF. Zero cross-over detection used in conjunction with the timer/event counter interrupt, is useful in thyristor control of power equipment. Figure 6 illustrates, (a) the input waveform, (b) the input diagram and (c) the on-chip self-stabilized bias.

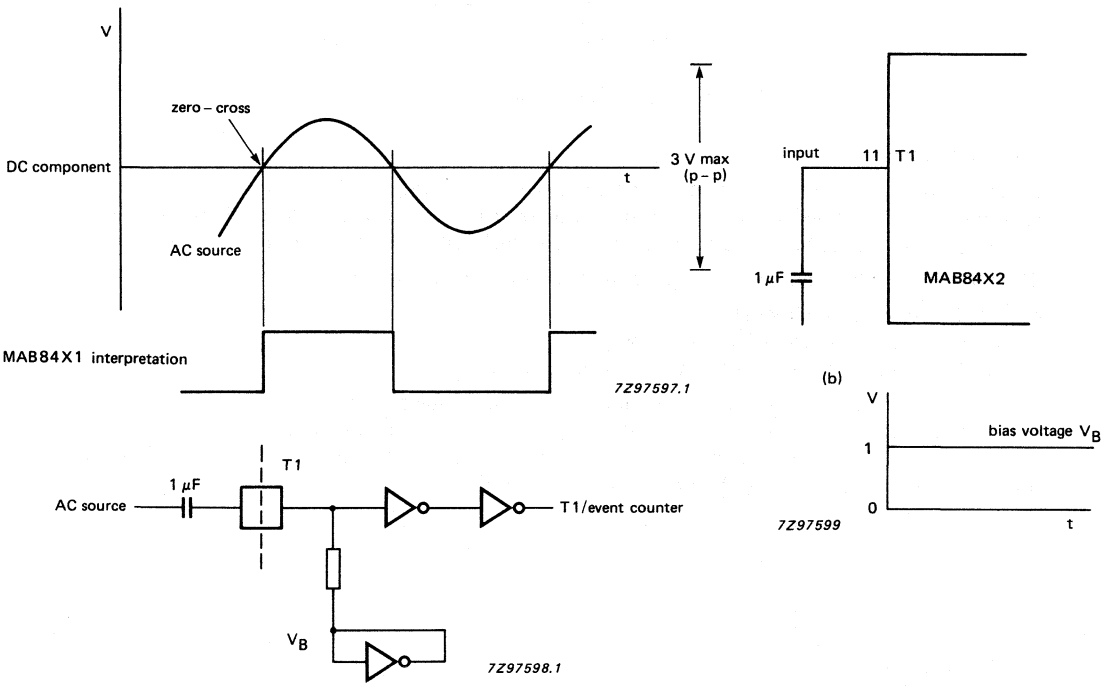


Fig. 6 Zero-cross voltage detection circuitry.

FUNCTIONAL DESCRIPTION (continued)

Timer/event counter

An 8-bit binary up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW to HIGH transitions on T1 (pin 13) are counted. The maximum rate at which the counter may be incremented is once every machine cycle (200 kHz for a 5 μs machine cycle). Fig. 7 illustrates the timer/event counter.

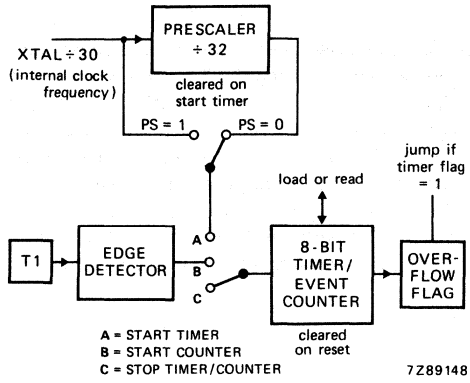


Fig. 7 Timer/event counter.

Interrupt system

External events and real-time on-chip peripherals require servicing by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution a multiple-source, single-level nested interrupt system is provided.

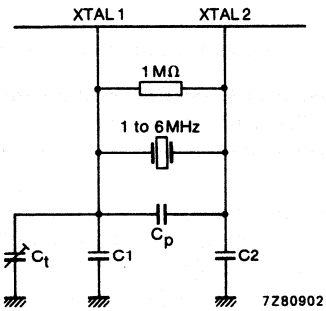
The MAB8422/8442 handles interrupts from three sources as follows:

- $\overline{\text{INT}}$/T0; externally via pin 9
- $\overline{\text{SIOINT}}$; from the internal serial I/O port
- TCNT interrupt; from the internal timer/event counter.

Each interrupt vectors to a separate location in the program memory for its service program. Each source can be individually enabled or disabled. When more than one interrupt occurs simultaneously, their priority will be: (1) external, (2) serial I/O and, (3) timer/event counter. An additional external interrupt can be created using the timer/event counter interrupt.

OSCILLATOR CIRCUITRY (see Fig. 8)

The clock frequency is determined by using the internal oscillator or by connecting an external clock to XTAL1. Where the internal oscillator is used the frequency is set by a crystal, a ceramic resonator or an inductor (each with associated capacitors) between XTAL1 and XTAL2. A machine cycle consists of 10 states, each state being 3 oscillator periods. The MAB8422/8442 has a dynamic logic, and therefore, for adequate refreshing the oscillator frequency must be at least 1 MHz.



1. Crystal - AT-cut
2. Ceramic resonator
   $C_1 = C_2 = 27$ pF
   C_t is optional
   $C_p < 6{,}75$ pF (parasitic capacitance)

Fig. 8(a) Quartz crystal or ceramic resonator mode.

If the frequency has to be trimmed, then a trimmer capacitor C_t should be connected in parallel with the fixed capacitor C_1.

Table 1 shows the LC values for timing generation with the LC oscillator.

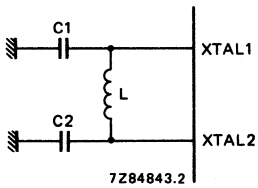
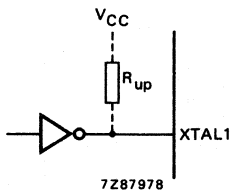


Fig. 8(b) LC pi-network.

Table 1 LC oscillator timing

frequency	C1 = C2	L
3,0 MHz	33 pF	100 μH
4,0 MHz	33 pF	56 μH
4,4 MHz	33 pF	47 μH
5,0 MHz	33 pF	33 μH
6,0 MHz	33 pF	22 μH



Drive XTAL1
Leave XTAL2 open

Driver may be high-speed CMOS or any TTL
t_r, $t_f < 10$ ns

Fig. 9 External drive.

RESET

A positive-going signal on the RESET input:

- sets the program counter to zero,
- selects location 0 of memory bank 0, and register bank 0,
- sets the stack pointer to zero (000); pointing to RAM address 8,
- disables the interrupts (external), timer and serial I/O),
- stops the timer/event counter, then sets it to zero,
- sets the timer prescaler to modulo-32,
- resets the timer flag,
- sets all ports to logic '1' (input mode),
- sets ports P1.0/SDA and P1.1/SCL to the parallel part mode and disables the serial I/O.

Automatic reset at power-up may be obtained by connecting the RESET pin to V_{CC} through a 1 μF capacitor C1, together with a diode to V_{SS} (cathode to RESET pin). This arrangement is satisfactory, if both the voltage (V_{CC}) rise time and the oscillator start-up time do not exceed either 1 or 10 ms respectively.

The power-on reset circuit is shown in Fig. 11; the input characteristics are shown in Fig. 12. At power-on the current drawn by RESET commences to charge the capacitor C1. The difference between this increasing capacitor voltage and V_{CC} is known as V_{RESET}. The charging circuit is designed to hold V_{RESET} above the lower threshold of a schmitt trigger arrangement, long enough to effect a complete reset. The minimum time required is the oscillator start-up time, plus two machine cycles.

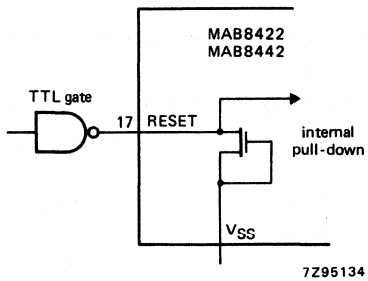


Fig. 10 External reset.

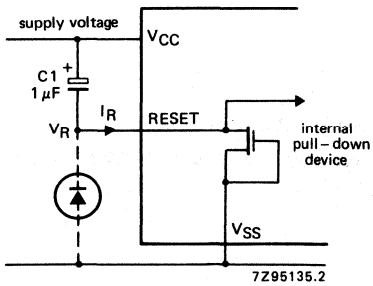


Fig. 11 Power-on reset circuitry.

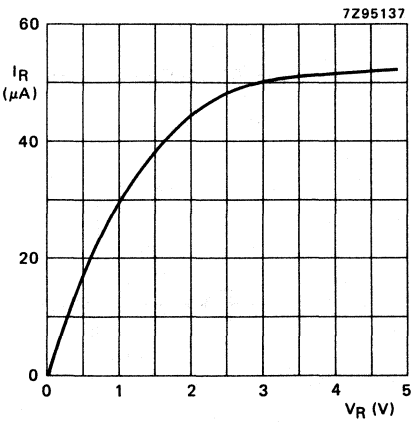


Fig. 12 Power-on reset input characteristics.

INSTRUCTION SET

The instruction set consists of over 80 one and two byte instructions and is based on the MAB8048 instruction set. New instructions include those for serial I/O operation and memory bank selection. Program code efficiency is high because all ROM locations on a 256 byte page require only a single byte address.

Table 2 gives the instruction set of the MAB84X2 family and Table 3 shows the instruction map. The following symbols and abbreviations are used.

symbol	description
A	the accumulator
AC	the auxiliary carry flag
addr	program memory address (11-bits)
Bb	bit designation (b = 0–7)
BS	the bank switch
C	carry flag
CLK	clock signal
CNT	event counter
D	nibble designation (4-bits)
DBF	program memory bank flip-flop
data	number of expression (8-bits)
F0, F1	flags 0 and 1
I	interrupt
$\overline{\text{INT}}$	external interrupt
P	'in-page' operation designation
Pp	port designation (p = 1, 2 or 4–7)
PSW	program status word
Rr	register designation (r = 0, 1 or 0–7)
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 an 1 inputs
#	immediate data prefix
@	indirect address prefix
S	current value of program counter
←	is replaced by
↔	is exchanged with

Table 2 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) −1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1}) \leftarrow A_n$ $(A_0) \leftarrow (C), (C) \leftarrow (A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (C), (C) \leftarrow (A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7}) \leftrightarrow (A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data		
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3}) \leftrightarrow ((R0_{0-3}))$ $(A_{0-3}) \leftrightarrow ((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3) \leftarrow (A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7}) \leftarrow (A), (A) \leftarrow ((PC))$		

Table 2 Instruction set (continued)

FLAGS	CLR C	97	1/1	clear carry bit	(C)←0	2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)	2
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1 r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1	
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1 r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1	
BRANCH	JMP addr	• 4 address	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))	
	DJNZ Rr, addr	E* address	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 r = 0–7 if (Rr) not zero (PC_{0-7})←addr	
	DJNZ @Rr, addr	E0 address	2/2	decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr	
		E1 address			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr	
	JBb addr	▲ 2 address	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr b = 0–7	
	JC addr	F6 address	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr	
	JNC addr	E6 address	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr	
	JZ addr	C6 address	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr	
	JNZ addr	96 address	2/2	jump to addr if A is NOT zero	if A ≠ 0 : (PC_{0-7})←addr	
	JT0 addr	36 address	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr	
	JNT0 addr	26 address	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr	
	JT1 addr	56 address	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr	
	JNT1 addr	46 address	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr	
	JTF addr	16 address	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr	4
	JNTF addr	06 address	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr	

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
SUBROUTINE	CALL addr	▲4 address	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4, 6, 7}$) (SP)←(SP) + 1 (PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) – 1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) – 1 ($PSW_{4, 6, 7}$) + (PC)←((SP))	6

Table 2 Instruction set (continued)

PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 data 99 data 9A data	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 data 89 data 8A data	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
	OUTL PO,A	90	1/2	Output accumulator data to port ϕ	(P0)←(A)	8
SERIAL INPUT/OUTPUT	EN SI	85	1/1	enable serial I/O interrupt		
	DIS SI	95	1/1	disable serial I/O interrupt		
	NOP	00	1/1	no operation		

Notes to Table 2.

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF).
5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 1111 P2.3, P2.2, P2.1, P2.0.
8. Only for software-transfer from the MAB8021.

* : 8, 9, A, B, C, D, E, F
● : 0, 2, 4, 6, 8, A, C, E
▲ : 1, 3, 5, 7, 9, B, D, F

TABLE 3 MAB8422/8442 INSTRUCTION MAP

first hexadecimal character of opcode ↓

second hexadecimal character of opcode →

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP			ADD A, # data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp							
1	INC ∂Rr		JB0 addr	ADDC A, # data	CALL page 0	DIS I	JTF addr	INC A	INC Rr							
2	XCH A, ∂Rr			MOV A, # data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	XCH A,Rr							
3	XCHD A,∂Rr		JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	OUTL Pp,A							
4	ORL A, ∂Rr		MOV A, T	ORL A, # data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr							
5	ANL A, ∂Rr		JB2 addr	ANL A, # data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr							
6	ADD A, ∂Rr		MOV T, A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr							
7	ADDC A, ∂Rr		JB3 addr		CALL page 3			RR A	ADDC A,Rr							
8				RET	JMP page 4	EN SI			ORL Pp,# data							
9	OUTL PO, A		JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,# data							
A	MOV ∂Rr, A			MOVP A, ∂A	JMP page 5	SEL MB2		CPL C	MOV Rr, A							
B	MOV ∂Rr, # data		JB5 addr	JMPP ∂A	CALL page 5	SEL MB3			MOV Rr, # data							
C	DEC ∂Rr				JMP page 6	SEL RB0	JZ addr	MOV A, PSW	DEC Rr							
D	XRL A, ∂Rr		JB6 addr	XRL A, # data	CALL page 6	SEL RB1		MOV PSW, A	XRL A,Rr							
E	DJNZ ∂Rr, addr				JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr							
F	MOV A, ∂Rr		JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A, Rr							

ABSOLUTE MAXIMUM RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Input voltage on any pin with respect to ground (V_{SS})	V_I	−0,5	+7	V
Total power dissipation	P_{tot}	−	1	W
Input/output current for all pins except port 0	I_I, I_O	−	10	mA
Input/output current for port 0	I_I, I_O	−	20	mA
Storage temperature	T_{stg}	−65	+150	°C
Operating temperature				
standard	T_{amb}	0	+70	°C
extended	T_{amb}	−40	+85	°C
automotive	T_{amb}	−40	+110	°C

DC CHARACTERISTICS

V_{CC} = 5 V (± 10%); V_{SS} = 0 V

parameter	conditions	symbol	min.	max.	unit
Supply current					
MAB8422/42	at 0 °C	I_{CC}	−	70	mA
MAF8422/42	at −40 °C	I_{CC}	−	90	mA
MAF84A22/42	at −40 °C	I_{CC}	−	90	mA
Inputs					
Input voltage LOW (except P1.0/SDA and P1.1/SCL)		V_{IL}	−0,5	0,8	V
Input voltage LOW (P1.0/SDA and P1.1/SCL)		V_{IL1}	−0,5	1,5	V
Input voltage HIGH all inputs except XTAL1, P1.0/SDA and P1.1/SCL		V_{IH}	2,0	V_{CC} + 0,5	V
Input voltage HIGH to XTAL1, P1.0/SDA and P1.1/SCL		V_{IH1}	3,0	V_{CC} + 0,5	V
Outputs					
Output voltage LOW (P0 only)	I_{OL} = 10 mA	V_{OL}		1,0	V
Output voltage LOW (P1.0/SDA and P1.1/SCL)	I_{OL} = 5 mA	V_{OL1}		0,45	V
Output voltage LOW (P0 and P2)	I_{OL} = 1,6 mA	V_{OL2}		0,45	V
Output voltage HIGH (all outputs unless open-drain)	I_{OH} = −50 μA	V_{OH}	2,4		V
Output leakage current	$V_{CC} > V_I > V_{SS}$	± I_{OL}		10	μA

AC CHARACTERISTICS

parameter	symbol	min.	max.	unit
Frequency				
MAB/MAF8422/42	f_{XTAL}	1	6	MHz
MAF84A22/42	f_{XTAL}	1	5	MHz
Cycle time				
MAB/MAF8422/42	t_{CY}	5	30	μs
MAF84A22/42	t_{CY}	6	30	μs

T1 ZERO-CROSS CHARACTERISTICS

T_{amb} = 0 to + 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V; C_L = 80 pF

parameter	conditions	symbol	min.	max.	unit
Zero-cross detection input (T1) peak-to-peak	AC coupled, C = 1 μF	$V_{ZX(p-p)}$	1	3	V
Zero-cross accuracy	50 Hz sine wave	A_{ZX}	–	± 135	mV
Zero-cross detection input frequency (T1)		F_{ZX}	0,05	1	kHz

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C552 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The PCB83C552 has the same instruction set as the PCB80C51. Two versions of the derivative exist although the generic term "PCB83C552" is used to refer to both family members:

- PCB83C552: 8 K bytes mask-programmable ROM, 256 bytes RAM
- PCB80C552: ROM-less version of the PCB83C552

This I/O intensive device provides architectural enhancements to function as a controller in the field of automotive electronics, specifically engine management and gear box control.

The PCB83C552 contains a non-volatile 8 K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a fifteen-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I²C-bus), a 'watchdog' timer and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C552 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.

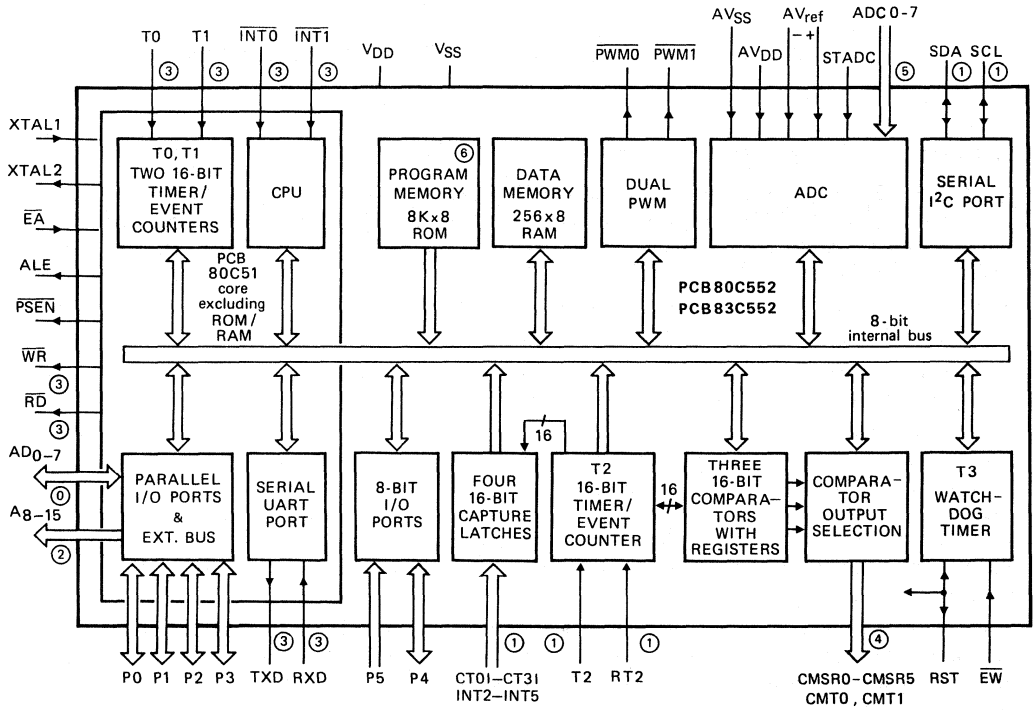
Features

- 80C51 central processing unit
- 8 K x 8 ROM, expandable externally to 64 K bytes
- 256 x 8 RAM, expandable externally to 64 K bytes
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- A 10-bit ADC with 8 multiplexed analogue inputs
- Two 8-bit resolution, Pulse Width Modulated outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analogue inputs
- I²C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART compatible with the standard PCB80C51
- On-chip watchdog timer

- **A version for extended temperature range is in preparation**

PACKAGE OUTLINES

PCB83C552; PCB80C552: 68-lead plastic leaded-chip-carrier (PLCC) (SOT188 pedestal or SOT188AA pocket versions, these are interchangeable).



⓪ alternative function of port 0
① alternative functions of port 1
② alternative function of port 2
③ alternative function of port 3
④ alternative function of port 4
⑤ alternative function of port 5
⑥ not present in PCB80C552

7Z97647.5

POWER SUPPLY
V_{DD} + 5 V MAIN SUPPLY
V_{SS} GROUND

Fig. 1 Block diagram.

DEVELOPMENT DATA

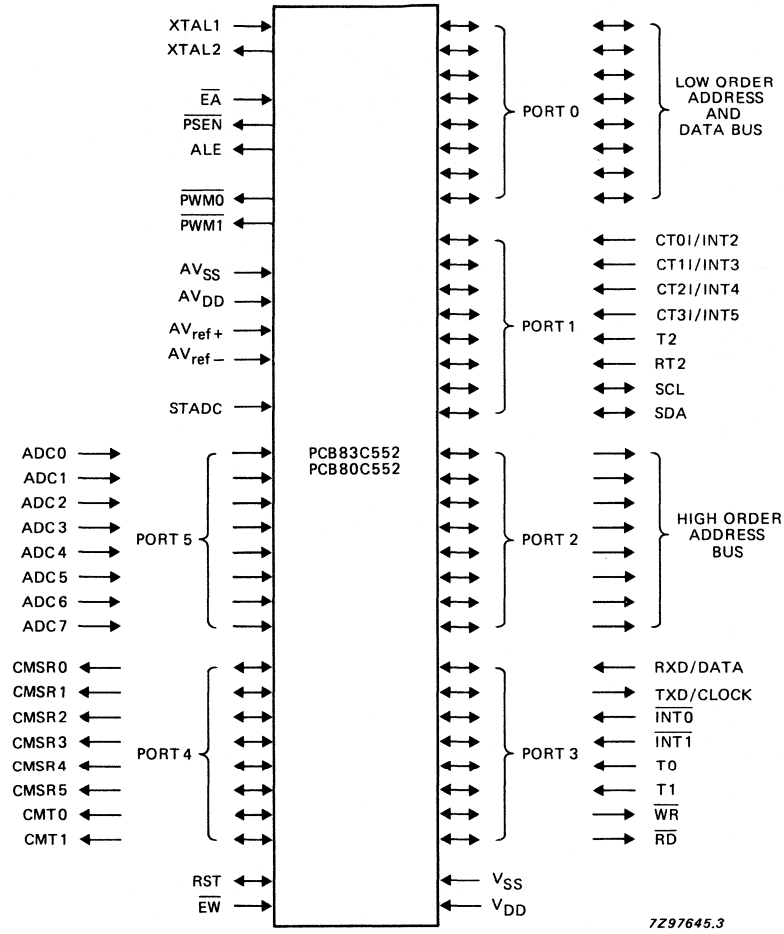


Fig. 2 Functional diagram.

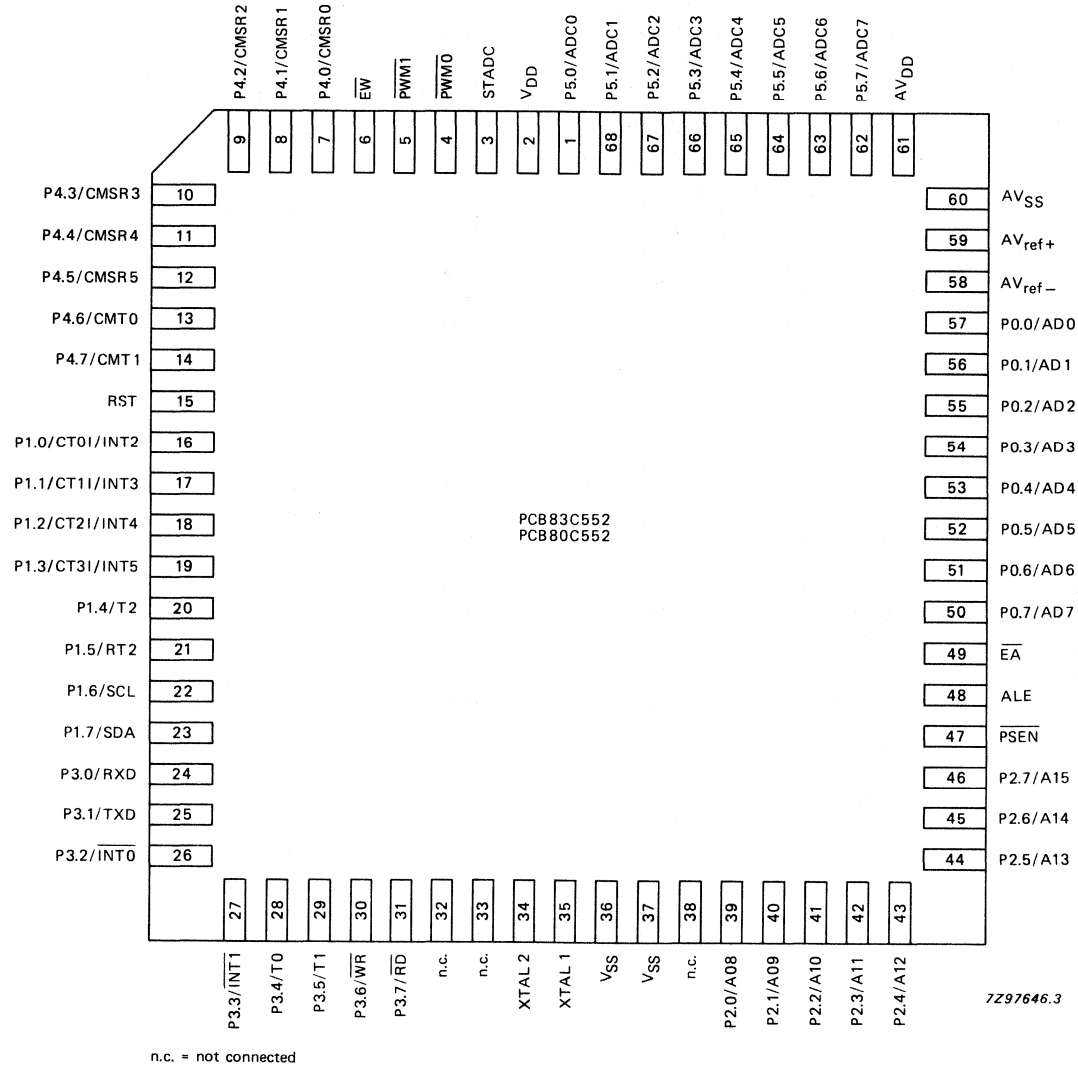


Fig. 3 Pinning diagram for PCB83C552.

DEVELOPMENT DATA

PINNING

2	V_{DD}	**Digital power supply**: + 5 V power supply pin during normal operation, Idle mode and Power-down mode
3	STADC	**Start ADC operation**: Input starting analogue to digital conversion (ADC operation can also be started by software)
4	$\overline{PWM0}$	**Pulse width** modulation output 0
5	$\overline{PWM1}$	**Pulse width** modulation output 1
6	$\overline{EW}$	**Enable watchdog timer**: Enable for T3 watchdog timer and disable Power-down mode
7-14	P4.0-P4.7	**Port 4** 8-bit quasi-bidirectional I/O port

Port pin	Alternative function	
P4.0	CMSR0	Timer T2: compare and set/reset outputs on a match with timer T2
P4.1	CMSR1	
P4.2	CMSR2	
P4.3	CMSR3	
P4.4	CMSR4	
P4.5	CMSR5	
P4.6	CMT0	Timer T2: compare and toggle outputs on a match with timer T2
P4.7	CMT1	

15	RST	**Reset**: Input to reset the PCB83C552. It also provides a reset pulse as output when timer T3 overflows.
16-23	P1.0-P1.7	**Port 1** 8-bit quasi-bidirectional I/O port

Port pin	Alternative function	
P1.0	CT0I/INT2	Capture timer input signals for timer T2 or Interrupts INT2 to INT5
P1.1	CT1I/INT3	
P1.2	CT2I/INT4	
P1.3	CT3I/INT5	
P1.4	T2	: T2 event input
P1.5	RT2	: T2 timer reset signal. Rising edge triggered
P1.6	SCL	: Serial port clock line I^2C-bus
P1.7	SDA	: Serial port data line I^2C-bus

24-31	P3.0-P3.7	**Port 3** 8-bit quasi-bidirectional I/O port

Port pin	Alternative function	
P3.0	RXD	: Serial input port
P3.1	TXD	: Serial output port
P3.2	$\overline{INT0}$	: External interrupt
P3.3	$\overline{INT1}$	: External interrupt
P3.4	T0	: Timer 0 external input
P3.5	T1	: Timer 1 external input
P3.6	$\overline{WR}$	: External data memory write strobe
P3.7	$\overline{RD}$	: External data memory read strobe

32, 33 Not connected

PINNING (continued)

34	XTAL2	**Crystal input 2:** output of the inverting amplifier that forms the oscillator. Left open-circuit when an external oscillator clock is used.
35	XTAL1	**Crystal input 1:** input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external oscillator clock signal when an external oscillator is used.
36, 37	V_{SS}	**Two digital** ground pins
38		Not connected
39-46	P2.0-P2.7	**Port 2** 8-bit quasi-bidirectional I/O port Port pin — Alternative function P2.0-P2.7 — High-order address byte for external memory (A08-A15)
47	$\overline{PSEN}$	**Program store enable:** active LOW read strobe to external program memory
48	ALE	**Address latch enable:** latches the low byte of the address during accesses to external memory. It is activated every six oscillator periods. During an external data memory access one ALE pulse is skipped. ALE can drive up to 8 LSTTL inputs and handles CMOS inputs without an external pull-up.
49	$\overline{EA}$	**External access:** When $\overline{EA}$ is held at TTL level HIGH, the CPU executes out of the internal program ROM provided the program counter is less than 8192. When $\overline{EA}$ is held at TTL LOW level, the CPU executes out of external program memory. $\overline{EA}$ is not allowed to float.
50-57	P0.7-P0.0	**Port 0** 8-bit binary I/O port Port pin — Alternative function P0.7-P0.0 — Multiplexed low-order address and data bus of external memory (AD7-AD0)
58	$AV_{ref}-$	**Low end** of analogue to digital conversion reference resistor
59	$AV_{ref}+$	**High end** of analogue to digital conversion reference resistor
60	AV_{SS}	**Analogue** ground
61	AV_{DD}	**Analogue** power supply
62-68,1	P5.7-P5.0	**Port 5** 8-bit input port Port pin — Alternative function P5.0-P5.7 — Eight input channels to ADC (ADC0-ADC7)

To avoid a 'latch-up' effect at power-on, the voltage on any pin at any time must not be higher or lower than V_{DD} + 0,5 V or V_{SS} − 0,5 V respectively.

FUNCTIONAL DESCRIPTION

General

The PCB83C552 is a stand-alone high-performance microcontroller designed for use in real-time applications such as instrumentation, industrial control and specific automotive control applications.

The device provides in addition to the 80C51 standard functions, a number of dedicated hardware functions for these applications.

The PCB83C552 is a control-oriented CPU with on-chip program and data memory. It can be extended with external program memory up to 64 K bytes. It can also access up to 64 K bytes of external data memory. For systems requiring extra capability, the PCB83C552 can be expanded using standard memories and peripherals.

The PCB83C552 has two software selectable modes of reduced activity for further power reduction – Idle and Power-down. The Idle mode freezes the CPU while allowing the RAM, timers, serial ports and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

Memory organisation

The central processing unit (CPU) manupilates operands in three memory spaces; these are the 64 K-byte external data memory, 256-byte internal data memory and the 64 K-byte internal and external program memory. The internal data memory address space is sub-divided into the 256-byte internal data RAM and 128-byte Special Function Register (SFR) address spaces, as shown in Fig. 4. Figures 5(a) and (b) show the Special Function Register memory map. Internal RAM locations 0-127 are directly and indirectly addressable. Internal RAM locations 128-255 are only indirectly addressable. The special function register locations 128-255 are only directly addressable.

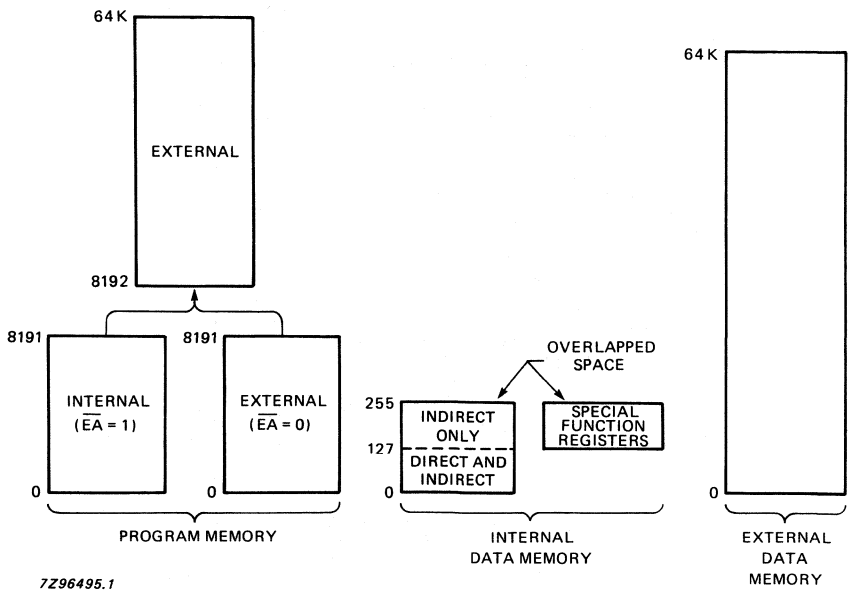
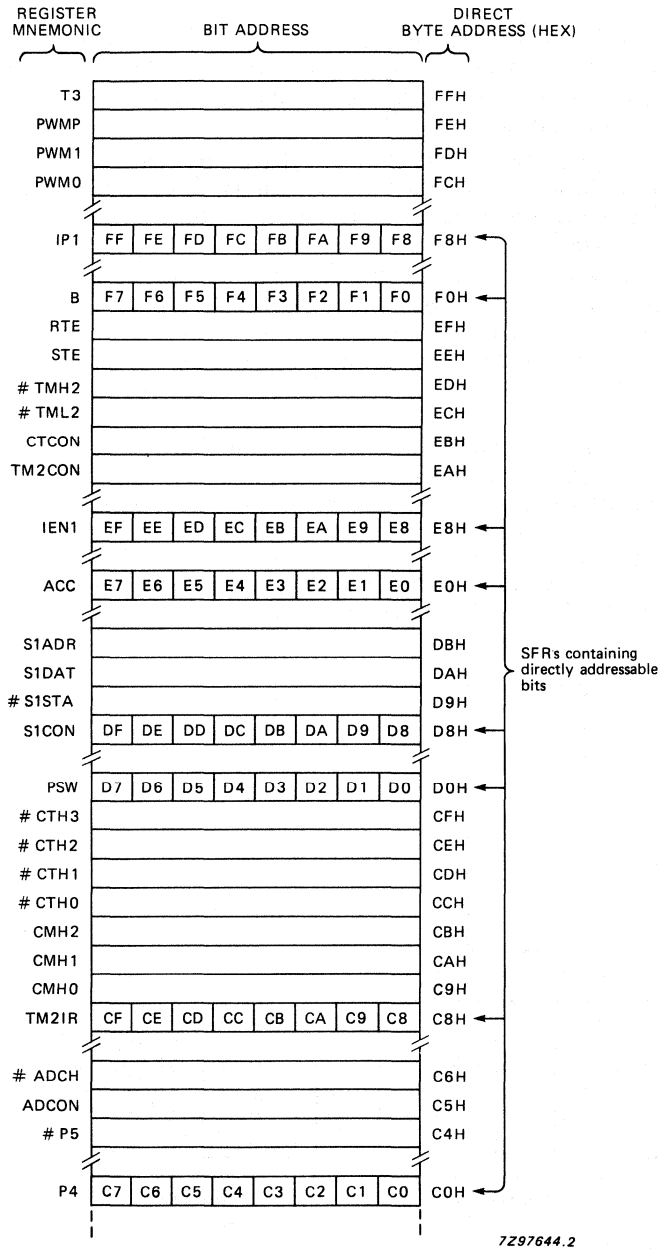


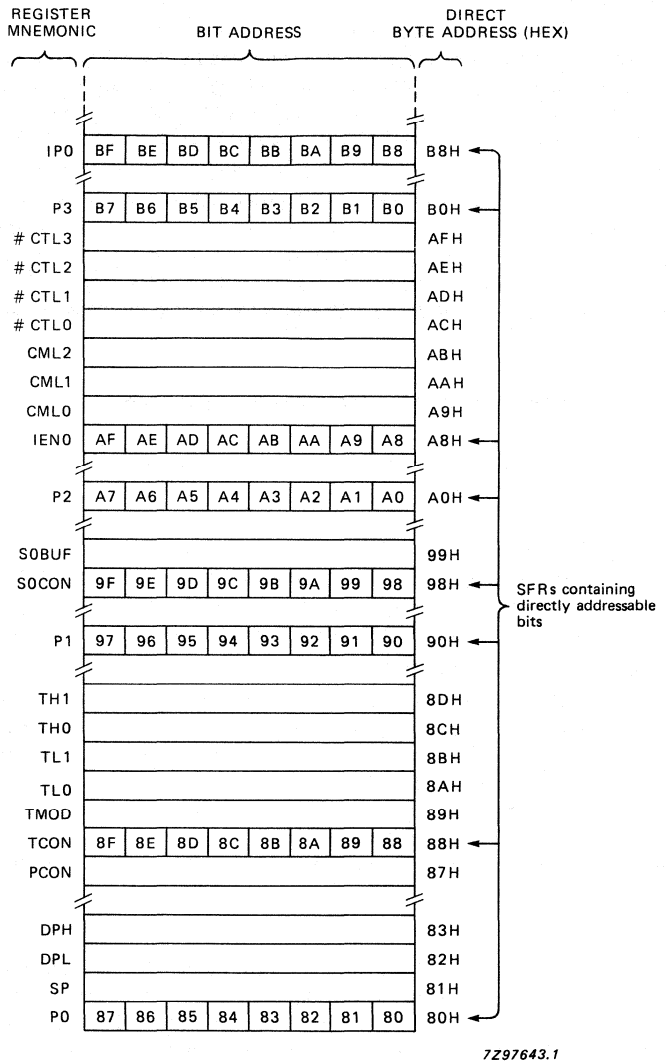
Fig. 4 Memory map.

FUNCTIONAL DESCRIPTION (continued)



# denotes read only registers

Fig. 5(a) Special Function Register memory map (continued in Fig. 5(b)).



# denotes read only registers

Fig. 5(b) Special Function Register memory map (continued from Fig. 5(a)).

FUNCTIONAL DESCRIPTION (continued)

The internal data RAM contains four register banks (each with eight registers), 128 addressable bits, a scratchpad area and the stack. The stack depth is limited by the available internal data RAM and its location is determined by the 8-bit stack pointer. All registers except the program counter and the four 8-register banks reside in the special function register address space. These memory mapped registers include arithmetic registers, pointers, I/O ports, interrupt system registers, ADC and PWM registers, timers and serial port registers. There are 128 addressable bit locations in the SFR address space.

The PCB83C552 contains 256 bytes of internal data RAM and 56 special function registers. It provides a non-paged program memory address space to accommodate relocatable code. Conditional branches are performed relative to the program counter. The register-indirect jump permits branching relative to a 16-bit base register with an offset provided by an 8-bit index register. 16-bit jumps and calls permit branching to any location in the contiguous 64 K program memory address space.

Addressing

The PCB83C552 has five methods for addressing source operands:

- Register
- Direct
- Register-Indirect
- Immediate
- Base-Register plus Index-Register-Indirect

The first three methods can be used for addressing destination operands. Most instructions have a "destination/source" field that specifies the data type, addressing methods and operands involved. For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four 8-register banks through Register, Direct, or Register-Indirect
- 256 bytes of internal data RAM through Direct or Register-Indirect. Bytes 0-127 may be addressed directly/indirectly. Bytes 128-255 share their address locations with the SFR registers and so may only be addressed indirectly as data RAM
- Special function registers through Direct at address locations 128-255
- External data memory through Register-Indirect
- Program memory look-up tables through Base-Register plus Index-Register-Indirect

Instruction set

The PCB83C552 uses the powerful instruction set of the PCB80C51. Additional special function registers are incorporated to control the on-chip peripherals. The instruction set consists of 49 single-byte, 45 two-byte and 17 three-byte instructions. When using a 12 MHz oscillator, 64 instructions execute in 1 μs and 45 instructions execute in 2 μs. Multiply and divide instructions execute in 4 μs.

I/O facilities

The PCB83C552 has six 8-bit ports. Ports 0 - 3 are the same as in the 80C51, with the exception of the additional functions of Port 1. The parallel I/O function of Port 4 is equal to that of Ports 1, 2 and 3. Port 5 has a parallel input port function, but has no function as an output port. Port lines P1.7 and P1.6 may be selected as the SDA and SCL lines of serial port SIO1 (I^2C). Because the I^2C-bus may be active while the device is disconnected from V_{DD}, these pins are provided with open drain drivers. Pins P1.7 and P1.6 do not have pull-up devices when used as ports.

Ports 0, 1, 2, 3, 4 and 5 perform the following alternative functions:

- Port 0: provides the multiplexed low-order address and data bus used for expanding the PCB83C552 with standard memories and peripherals.
- Port 1: Port 1 is used for a number of special functions;
  - 4 capture inputs
  - external counter input
  - external counter reset input
  - SCL and SDA for the I^2C interface

Bits whose alternate function is not used may be used as normal bidirectional I/O pins.

- Port 2: provides the high-order address bus when expanding the PCB83C552 with external program memory and/or external data memory.
- Port 3: pins can be configured individually to provide:
  - external interrupt request inputs
  - counter inputs
  - serial port receiver input and transmitter output
  - control signals to READ and WRITE external data memory

The generation or use of a Port 3 pin as an alternative function is carried out automatically by the PCB83C552 provided the associated Special Function Register bit is set high.

- Port 4: can be configured to provide signals indicating a match between timer counter T2 and its compare registers.
- Port 5: may be used in conjunction with the ADC interface. Unused analogue inputs can be used as digital inputs. As Port 5 lines may be used as inputs to the ADC, these digital inputs have an inherent hysteresis to prevent the input logic from drawing too much current from the power lines when driven by analogue signals. Channel to channel crosstalk should be taken into consideration when both digital and analogue signals are simultaneously input to Port 5 (see DC characteristics).

All ports are bidirectional with the exception of Port 5 which is an input port.

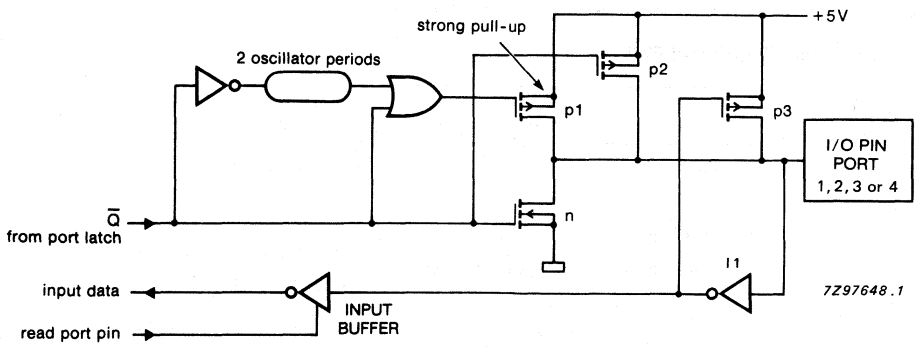


Fig. 6 I/O buffers in the PCB83C552 (Ports 2, 3, 4 and P1.0 to P1.5).

FUNCTIONAL DESCRIPTION (continued)

In addition to the standard 8-bit ports, the I/O facilities of the PCB83C552 also include a number of special I/O lines:

Pulse width modulated outputs

Two pulse width modulated output channels are provided with the PCB83C552. These channels output pulses of programmable length and interval. The repetition frequency is defined by an 8-bit prescaler PWMP which generates the clock for the counter. Both the prescaler and counter are common to both PWM channels. The 8-bit counter counts modulo 255 i.e. from 0 to 254 inclusive. The value of the 8-bit counter is compared to the contents of two registers: PWM0 and PWM1. Provided the contents of either of these registers is greater than the counter value, the output of $\overline{PWM0}$ or $\overline{PMW1}$ is set LOW. If the contents of these registers are equal to, or less than the counter value, the output will be HIGH. The pulse-width-ratio is therefore defined by the contents of the registers PWM0 and PWM1. The pulse-width-ratio is in the range of 0 to 255/255 and may be programmed in increments of 1/255.

The repetition frequency f_{PWM}, at the $\overline{PWMn}$ outputs is given by:

$$f_{PWM} = \frac{f_{osc}}{2 \times (1 + PWMP) \times 255}$$

This gives a repetition frequency range of 92 Hz to 23,5 kHz (f_{osc} = 12 MHz).

By loading the PWM registers with either 00H or FFH, the PWM outputs can be retained at a constant HIGH or LOW level respectively. When loading FFH to the PWM registers, the 8-bit counter will never actually reach this value.

Both $\overline{PWMn}$ output pins are driven by push-pull drivers, and are not shared with any other function.

Prescaler frequency control register PWMP

	7	6	5	4	3	2	1	0
PWMP (FEH)								

MSB LSB

Bit	Function
PWMP.0-7	Prescaler division factor = (PWMP) + 1

Pulse width registers PWM0 and PWM1

	7	6	5	4	3	2	1	0
PWM0 (FCH) PWM1 (FDH)								

MSB LSB

Bit	Function
PWM0.0-7 PWM1.0-7	Low/high ratio of $\overline{PWMn}$ signals $= \frac{(PWMn)}{255 - (PWMn)}$

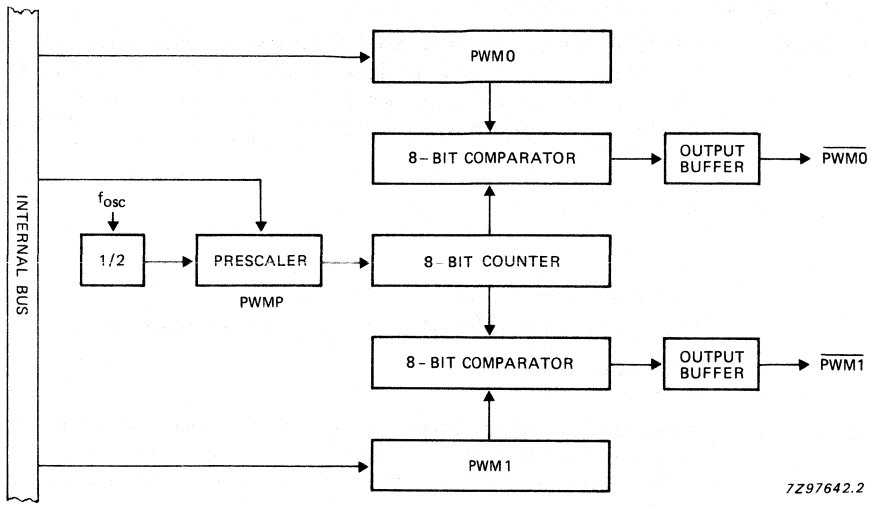


Fig. 7 Functional diagram of pulse width modulated outputs.

DEVELOPMENT DATA

Analogue input pins

The analogue input circuitry consists of an 8-input analogue multiplexer and an ADC with 10-bit resolution. The analogue reference voltage and analogue power supplies are connected via separate input pins. The conversion takes 50 machine cycles i.e. 50 μs at 12 MHz oscillator frequency.

The ADC is controlled using the ADCON control register. Input channels are selected by the analogue multiplexer, care of ADCON register bits 0-2.

ADC control register ADCON

	7	6	5	4	3	2	1	0
ADCON (C5H)	ADC.1	ADC.0	ADEX	ADCI	ADCS	AADR2	AADR1	AADR0

Bit	Symbol	Function
ADCON.7	ADC.1	Bit 1 of ADC converted value
ADCON.6	ADC.0	Bit 0 of ADC converted value
ADCON.5	ADEX	Enable external start of conversion by STADC
		0 = Conversion cannot be started externally by STADC
		1 = Conversion can be started externally by STADC
ADCON.4	ADCI	ADC interrupt flag: this flag is set when an ADC conversion result is ready to be read. An interrupt is invoked if this is enabled. The flag must be cleared by software. It cannot be set by software.

FUNCTIONAL DESCRIPTION (continued)

ADCON.3 ADCS — ADC start and status: setting this bit starts an ADC conversion. It may be set by software or by the external signal STADC. The ADC logic ensures that this signal is HIGH while the ADC is busy. On completion of the conversion, ADCS is reset at the same time the interrupt flag ADCI is set. ADCS can not be reset by software.

ADCI	ADCS	OPERATION
0	0	ADC not busy, a conversion can be started
0	1	ADC busy, start of a new conversion is blocked
1	0	Conversion completed, start of a new conversion is blocked
1	1	Not possible

ADCON.2 AADR2
ADCON.1 AADR1
ADCON.0 AADR0

Analogue input select: this binary coded address selects one of the eight analogue port bits of P5 to be input to the converter. It can only be changed when ADCI and ADCS are both LOW. AADR2 is the most significant bit (100 selects the ADC4 analogue input channel).

The completion of the 10-bit ADC conversion is flagged by ADCI in the ADCON register and the result is stored in special function register ADCH (upper 8 bits) and the 2 LSBs in register ADCON.

An ADC conversion in progress is unaffected by an external or software ADC start. The result of a completed conversion remains unaffected provided ADCI = logic 1. While ADCS = logic 1 or ADCI = logic 1, a new ADC START will be blocked and consequently lost. An ADC conversion already in progress is aborted when the Idle or Power-down mode is entered. The result of a completed conversion (ADCI = logic 1) remains unaffected when entering the Idle mode.

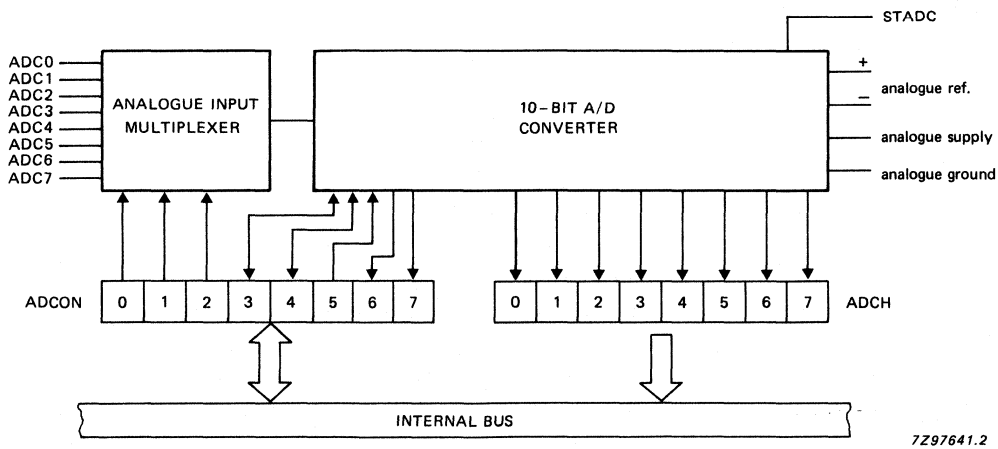


Fig. 8 Functional diagram of analogue input.

Timer/event counters

The PCB83C552 contains three 16-bit timer/event counters: Timer 0, Timer 1 and Timer T2 and one 8-bit timer, T3. Timer 0 and Timer 1 may be programmed to carry out the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests

Timer 0 and Timer 1 can be programmed independently to operate in three modes:

- Mode 0: 8-bit timer or 8-bit counter each with divide-by-32 prescaler
- Mode 1: 16-bit time-interval or event counter
- Mode 2: 8-bit time-interval or event counter with automatic reload upon overflow

Timer 0 can be programmed to operate in an additional mode as follows:

- Mode 3: one 8-bit time-interval or event counter and one 8-bit time-interval counter

When Timer 0 is in Mode 3, Timer 1 can be programmed to operate in Modes 0, 1 or 2 but cannot set an interrupt request flag or generate an interrupt. However the overflow from Timer 1 can be used to pulse the serial port transmission-rate generator.

The frequency handling range of these counters with a 12 MHz crystal is as follows:

- In the timer function, the timer is incremented at a frequency of 1 MHz — a division by 12 of the oscillator frequency
- 0 Hz to an upper limit of 0,5 MHz when programmed for external inputs

Both internal and external inputs can be gated to the counter by a second external source for directly measuring pulse durations.

The counters are started and stopped under software control. Each one sets its interrupt request flag when it overflows from all logic 1s to all logic 0s (or automatic reload value), with the exception of mode 3 as previously described.

Timer T2

Timer T2 is a 16 bit timer/counter which has, coupled to it, capture and compare facilities. The operational diagram is shown in Fig. 9.

The 16 bit timer/counter is clocked via a prescaler with a programmable division factor of 1, 2, 4 or 8. The input of the prescaler is clocked with 1/12 of the oscillator frequency, or with positive edges on the T2 input, or it is switched to the off position. This prescaler is cleared if its division factor or its input source is changed, or if the timer/counter is reset. T2 is readable 'on the fly', but posseses no extra read latches; this means that software precautions have to be taken against misinterpretation in overflow from least to most significant byte during read. T2 is not loadable and is reset by the RST signal or at the positive edge of the input signal RT2, if enabled. In the Idle mode the timer/counter and prescaler are reset and halted.

T2 is connected to four 16-bit capture registers: CT0, CT1, CT2 and CT3. These registers are loaded with the contents of T2 and an interrupt is requested upon receipt of the input signals CT0I, CT1I, CT2I or CT3I. These input signals are shared with Port 1. Using the capture register CTCON, these inputs may capture on a positive edge, a negative edge or on either a positive or negative edge.

FUNCTIONAL DESCRIPTION (continued)

The contents of the compare registers CM0, CM1 and CM2 are continually compared with the counter value of Timer T2. When a match is found an interrupt may be invoked. Using the match signal of CM0, the controller sets bits 0-5 of Port 4, if the corresponding bits of the set enable register STE are logic 1.

Considering a match with CM1, if the corresponding bits of the reset/toggle enable register RTE are logic 1, then the controller will use the match signal to reset bits 0-5 of Port 4. Bits 6 and 7 of Port 4 may be 'toggled' by the signal that indicates a match between Timer T2 and CM2 if the corresponding bits of RTE are logic 1. CM0, CM1 and CM2 are reset by the RST signal.

Port 4 can be read and written by software without affecting the toggle, set and reset signals. At byte overflow of the least significant byte, or at a 16-bit overflow of the timer/counter, an interrupt sharing the same interrupt vector is requested. Either or both of these overflows can be programmed to request an interrupt.

All interupt flags must be reset by software.

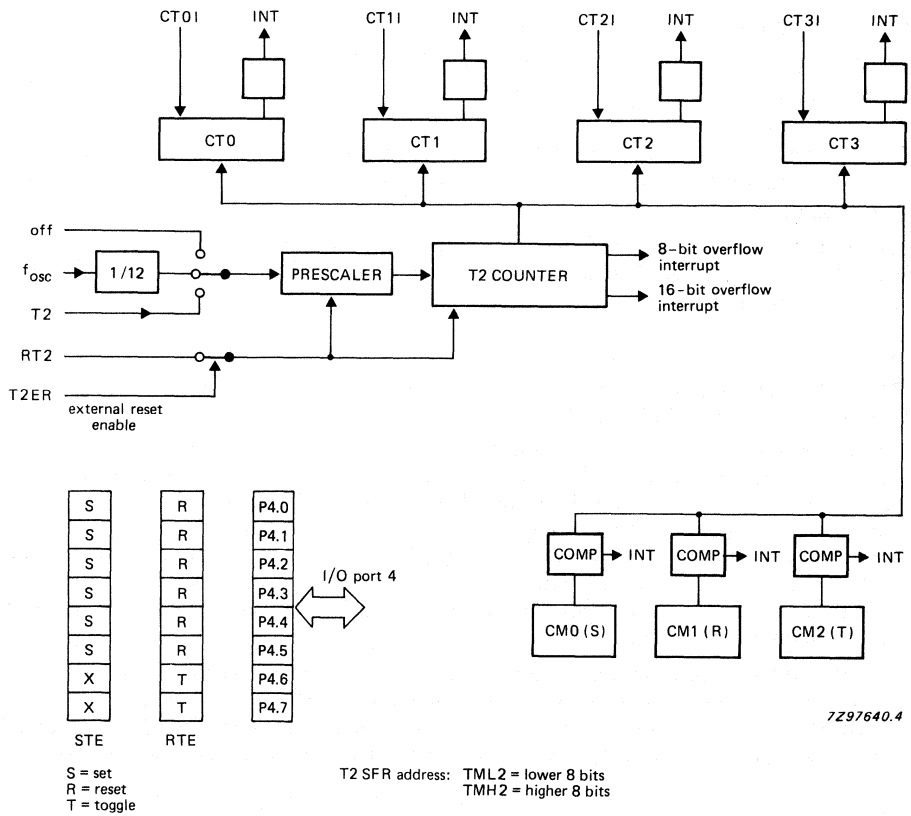


Fig. 9 Block diagram of Timer T2 configuration.

Counter control register TM2CON

	7	6	5	4	3	2	1	0
TM2CON (EAH)	T2IS1	T2IS0	T2ER	T2B0	T2P1	T2P0	T2MS1	T2MS0
	MSB							LSB

Bit	Symbol	Function
TM2CON.7	T2IS1	Timer 2 16 bit overflow interrupt select
TM2CON.6	T2IS0	Timer 2 byte overflow interrupt select
TM2CON.5	T2ER	Timer 2 external reset enable
TM2CON.4	T2B0	Timer 2 byte overflow interrupt flag
TM2CON.3	T2P1	Timer 2 prescaler select
TM2CON.2	T2P0	
TM2CON.1	T2MS1	Timer 2 mode select
TM2CON.0	T2MS0	

T2P1	T2P0	T2 clock
0	0	clock source
0	1	clock source/2
1	0	clock source/4
1	1	clock source/8

T2MS1	T2MS0	Mode Selected
0	0	Timer T2 is halted
0	1	T2 clock source = $f_{osc}/12$
1	0	Test mode; do not use
1	1	T2 clock source = pin T2

Capture control register CTCON

	7	6	5	4	3	2	1	0
CTCON (EBH)	CTN3	CTP3	CTN2	CTP2	CTN1	CTP1	CTN0	CTP0
	MSB							LSB

Bit	Symbol	Capture/Interrupt on:
CTCON.7	CTN3	CT3I negative edge
CTCON.6	CTP3	CT3I positive edge
CTCON.5	CTN2	CT2I negative edge
CTCON.4	CTP2	CT2I positive edge
CTCON.3	CTN1	CT1I negative edge
CTCON.2	CTP1	CT1I positive edge
CTCON.1	CTN0	CT0I negative edge
CTCON.0	CTP0	CT0I positive edge

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Timer interrupt flag register TM21R

	7	6	5	4	3	2	1	0
TM2IR (C8H)	T20V	CMI2	CMI1	CMI0	CTI3	CTI2	CTI1	CTI0
	MSB							LSB

Bit	Symbol	Function
TM2IR.7	T20V	T2 16-bit overflow interrupt flag
TM2IR.6	CMI2	CM2 interrupt flag
TM2IR.5	CMI1	CM1 interrupt flag
TM2IR.4	CMI0	CM0 interrupt flag
TM2IR.3	CTI3/INT5	CT3 interrupt flag
TM2IR.2	CTI2/INT4	CT2 interrupt flag
TM2IR.1	CTI1/INT3	CT1 interrupt flag
TM2IR.0	CTI0/INT2	CT0 interrupt flag

Interrupt enable register IEN1 is used to enable/disable timer 2 interrupts.
Interrupt priority register IP1 is used to determine the timer interrupt priority.

The set enable register STE

	7	6	5	4	3	2	1	0
STE (EEH)	TG4.7	TG4.6	SP45	SP44	SP43	SP42	SP41	SP40
	MSB							LSB

Bit	Symbol	Function
STE.7	TG4.7	
STE.6	TG4.6	
STE.5	SP45	if "1" then P4.5 is set on a match between CM0 and T2
STE.4	SP44	if "1" then P4.4 is set on a match between CM0 and T2
STE.3	SP43	if "1" then P4.3 is set on a match between CM0 and T2
STE.2	SP42	if "1" then P4.2 is set on a match between CM0 and T2
STE.1	SP41	if "1" then P4.1 is set on a match between CM0 and T2
STE.0	SP40	if "1" then P4.0 is set on a match between CM0 and T2

If STE.n is "0" then P4.n is not affected by a match between CM0 and T2

The reset/toggle enable register RTE

	7	6	5	4	3	2	1	0
RTE (EFH)	TP47	TP46	RP45	RP44	RP43	RP42	RP41	RP40
	MSB							LSB

Bit	Symbol	Function
RTE.7	TP47	if "1" then P4.7 toggles on a match between CM2 and T2
RTE.6	TP46	if "1" then P4.6 toggles on a match between CM2 and T2
RTE.5	RP45	if "1" then P4.5 is reset on a match between CM1 and T2
RTE.4	RP44	if "1" then P4.4 is reset on a match between CM1 and T2
RTE.3	RP43	if "1" then P4.3 is reset on a match between CM1 and T2
RTE.2	RP42	if "1" then P4.2 is reset on a match between CM1 and T2
RTE.1	RP41	if "1" then P4.1 is reset on a match between CM1 and T2
RTE.0	RP40	if "1" then P4.0 is reset on a match between CM1 and T2

If RTE.n is "0" then P4.n is not affected by a match between CM1 and T2 or CM2 and T2

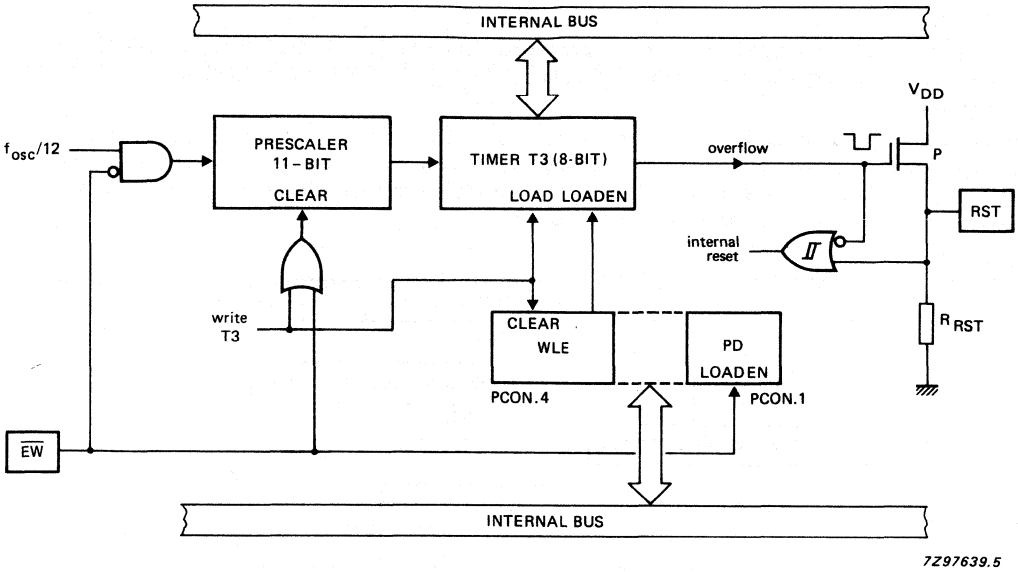


Fig. 10 Functional diagram of T3 watchdog timer.

T3 The watchdog timer (see Fig. 10)

In addition to Timer T2 and the standard timers, a watchdog timer consisting of an 11-bit prescaler and an 8-bit timer are also incorporated.

The timer is incremented every 2 ms, derived from the oscillator frequency of 12 MHz by the following:

$$f_{timer} = \frac{f_{osc}}{12 \times 2048}$$

When a timer overflow occurs, the microcontroller is reset and a reset output pulse is generated at pin RST. To prevent a system reset the timer must be reloaded in time by the application software. If the processor suffers a hardware/software malfunction, the software will fail to reload the timer. This failure will produce a reset upon overflow thus preventing the processor running out of control.

The watchdog timer can only be reloaded if the condition flag WLE = PCON.4 has been previously set by software.

At the moment the counter is loaded the condition flag is automatically cleared.

The time interval between the timer's reloading and occurance of a reset, is dependent upon the reloaded value. This may range from 2 ms to 0,5 s at an oscillator frequency of 12 MHz.

In the Idle state the watchdog timer and reset circuitry remain active.

The watchdog timer is controlled by the watchdog enable pin ($\overline{EW}$). A logic 0 enables the watchdog timer and disables the Power-down mode. A logic 1 disables and resets the watchdog timer and enables the Power-down mode.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Serial I/O (see Fig. 11)

The PCB83C552 is equipped with two independent serial ports. SIO0 is the full duplex UART port and is identical to the serial port of the PCB80C51 (see "SINGLE-CHIP 8-BIT MICROCONTROLLERS" User Manual).

Serial port SIO1 supports the I^2C-bus, the function of which is controlled by the S1CON register. S1STA is the status register whose contents may also be used as a vector to various service routines. S1DAT is the data shift register and S1ADR the slave address register. The least significant bit of S1ADR enables/disables general call address recognition.

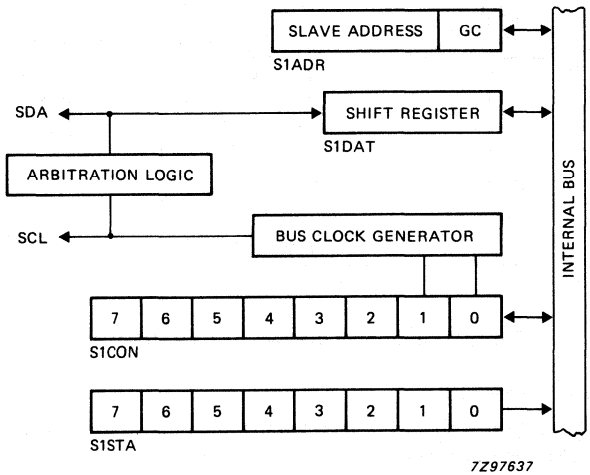


Fig. 11 Block diagram of I^2C serial I/O.

The I^2C serial I/O has complete autonomy in byte handling and operates in 4 modes:

1. Master transmitter
2. Master receiver
3. Slave transmitter
4. Slave receiver

Slave address recognition is performed by on-chip hardware.

The I^2C-bus consists of two lines: a data line (SDA) and a clock line (SCL). These lines also function as the I/O port lines on P1.7 and P1.6. The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware.

Serial control register S1CON

	7	6	5	4	3	2	1	0
S1CON (D8H)	CR2	ENS1	STA	STO	SI	AA	CR1	CR0

Bits CR0, CR1 and CR2 determine the serial clock frequency that is generated in the master mode of operation.

Table 1 Serial clock rates

CR2 (1)	CR1	CR0	bit frequency (kHz) at f_{OSC}:			f_{OSC} divided by
			6 MHz	12 MHz	16 MHz (1)	
0	0	0	23	47	63	256 (1)
0	0	1	27	54	71	224 (1)
0	1	0	31	63	83	192 (1)
0	1	1	37	75	100	160 (1)
1	0	0	6.25	12.5	17	960
1	0	1	50	100	133 (2)	120
1	1	0	100	200 (2)	267 (2)	60
1	1	1	0.25 < 62.5	0.5 < 62.5	0.67 < 56	96 x (256 - reload value Timer 1) (reload value range: 0 - 254 in mode 2)

Notes to Table 1

(1) A maximum frequency of 16 MHz will be implemented in a later version. At present control bit CR2 is not used.

(2) These frequencies exceed the upper limit of 100 kHz of the I^2C-bus specification and cannot be used in an I^2C-bus application.

DEVELOPMENT DATA

AA

Assert acknowledge bit. When this bit is set, an acknowledge is returned after any one of the following conditions:

- Own slave address is received
- General call address is received (S1ADR.0 = logic 1)
- A data byte is received, while the device is programmed to be a master receiver
- A data byte is received, while the device is a selected slave receiver

When this bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own address or general call address is received.

SI

SIO1 interrupt flag. This flag is set, and an interrupt request is generated, after any of the following events occur:

- A START condition is generated in MST mode
- The own slave address has been received during AA = logic 1
- The general call address has been received while S1ADR.0 and AA = logic 1
- A data byte has been received or transmitted in MST mode (even if arbitration is lost)
- A data byte has been received or transmitted as selected slave
- A STOP or START condition is received as selected slave receiver or transmitter

FUNCTIONAL DESCRIPTION (continued)

STO

STOP flag. When in master mode, and this bit is set a STOP condition is generated. A STOP condition detected on the I²C-bus clears this bit. This bit may also be set in slave mode in order to recover from an error condition. Then no STOP condition is generated to the I²C-bus, but the hardware releases the SDA and SCL lines and switches to the not selected slave receiver mode. The STOP flag is cleared by the hardware.

STA

START flag. When this bit is set in slave mode, the hardware checks the I²C-bus and generates a START condition if the bus is free or after the bus becomes free. If the device operates in master mode it will generate a repeated START condition.

ENS1

0 = Serial I/O Disabled and reset. P1.6 and P1.7 I/O port function with open drain

1 = Serial I/O Enabled. Output ports P1.6 and P1.7 must be set to logic 1

Serial status register S1STA (S1STA is a read-only register)

	7	6	5	4	3	2	1	0
S1STA (D9H)	SC4	SC3	SC2	SC1	SC0	0	0	0

S1STA.3 - S1STA.7 hold a status code. S1STA.0 - S1STA.2 are held LOW. The contents of the status register may be used as a vector to a service routine. This optimizes the response time of the software and consequently that of the I²C-bus.

Abbreviations used:

SLA	:	7-bit slave address
R	:	Read bit
W	:	Write bit
ACK	:	Acknowledgement (acknowledge bit = logic 0)
$\overline{\text{ACK}}$	:	Not acknowledgement (acknowledge bit = logic 1)
DATA	:	8-bit data byte to or from I²C-bus
MST	:	Master
SLV	:	Slave
TRX	:	Transmitter
REC	:	Receiver

The following is a list of the status codes:

MST/TRX mode

S1STA value

- 08H — A START condition has been transmitted
- 10H — A repeated START condition has been transmitted
- 18H — SLA and W have been transmitted, ACK has been received
- 20H — SLA and W have been transmitted, $\overline{\text{ACK}}$ received
- 28H — DATA of S1DAT has been transmitted, ACK received
- 30H — DATA of S1DAT has been transmitted, $\overline{\text{ACK}}$ received
- 38H — Arbitration lost in SLA, R/W or DATA

MST/REC mode

S1STA value

38H – Arbitration lost while returning $\overline{ACK}$
40H – SLA and R have been transmitted, ACK received
48H – SLA and R have been transmitted, $\overline{ACK}$ received
50H – DATA has been received, ACK returned
58H – DATA has been received, $\overline{ACK}$ returned

SLV/REC mode

S1STA value

60H – Own SLA and W have been received, ACK returned
68H – Arbitration lost in SLA, R/W as MST. Own SLA and W have been received, ACK returned
70H – General CALL has been received, ACK returned
78H – Arbitration lost in SLA, R/W as MST. General call has been received
80H – Previously addressed with own SLA. DATA byte received, ACK returned
88H – Previously addressed with own SLA. DATA byte received, $\overline{ACK}$ returned
90H – Previously addressed with general call. DATA byte has been received, ACK has been returned
98H – Previously addressed with general call. DATA byte has been received, $\overline{ACK}$ has been returned
A0H – A STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX.

SLV/TRX mode

S1STA value

A8H – Own SLA and R have been received, ACK returned
B0H – Arbitration lost in SLA, R/W as MST. Own SLA and R have been received, ACK returned
B8H – DATA byte has been transmitted, ACK received
C0H – DATA byte has been transmitted, $\overline{ACK}$ received
C8H – Last DATA byte has been transmitted (AA = logic 0), ACK received

Miscellaneous

S1STA value

00H – Bus error during MST mode or selected SLV mode, due to an erroneous START or STOP condition

The data shift register S1DAT

S1DAT (DAH)	7	6	5	4	3	2	1	0

This register contains the serial data to be transmitted or data which has just been received. Bit 7 is transmitted or received first; i.e. data is shifted from right to left.

Address register S1ADR

S1ADR (DBH)	7	6	5	4	3	2	1	0

S1ADR.0, GC : 0 = general call address is not recognized
1 = general call address is recognized

S1ADR.7-1 : own slave address

This 8-bit register may be loaded with the 7-bit slave address to which the controller will respond when programmed as a slave receiver/transmitter. The LSB (GC) is used to determine whether the general call address is recognized.

FUNCTIONAL DESCRIPTION (continued)

Idle and Power-down operation (see Fig. 12)

Idle mode operation permits the interrupt, serial ports and timer blocks to continue to function while the CPU is halted. The following functions are also switched off when the processor enters the Idle mode.

Timer T2	(stopped and reset)
PWM0, PWM1	(reset, output = HIGH)
ADC	(aborted if in progress)

The following functions remain active during Idle mode. These functions may generate an interrupt or reset and thus end the Idle mode.

Timer 0, Timer 1
Timer T3
SIO0, SIO1
External interrupt

The Power-down operation freezes the oscillator. The Power-down mode can only be activated by setting the PD bit in the PCON register. The PD bit can only be set if the EWN input is HIGH.

Idle mode

The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before Idle mode is activated. Once in the Idle mode, the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 2.

There are two ways to terminate the Idle mode:

Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware terminating Idle mode. The interrupt is serviced, and following return from interrupt instruction RETI, the next instruction to be executed will be the one which follows the instruction that wrote a logic 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle mode is with an external hardware reset, or an internal reset caused by an overflow of Timer T3. Since the oscillator is still running, the hardware reset is required to be active for two machine cycles (24 oscillator periods) to complete the reset operation.

Power-down mode

The instruction that sets PCON.1 is the last executed prior to going into the Power-down mode. Once in Power-down mode, the oscillator is stopped. Only the contents of the on-chip RAM are preserved. The Special Function Registers are not saved. A hardware reset is the only way of exiting the Power-down mode.

In the Power-down mode, V_{DD} may be reduced to minimize circuit power consumption. The voltage must not be reduced until the Power-down mode is entered, but must be restored before the hardware reset is applied which will free the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

The status of the external pins during Power-down mode is shown in Table 2. If the Power-down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull-up transistor p1 (see Fig. 6).

Table 2 Status of external pins during Idle and Power-down modes

mode	memory	ALE	$\overline{PSEN}$	Port 0	Port 1	Port 2	Port 3	Port 4	$\overline{PWM0}$/$\overline{PWM1}$
Idle (1)	internal	1	1	port data	port data	port data	port data	port data	HIGH
Idle (1)	external	1	1	floating	port data	address	port data	port data	HIGH
Power-down	internal	0	0	port data	port data	port data	port data	port data	HIGH
Power-down	external	0	0	floating	port data	port data	port data	port data	HIGH

Power control register (PCON)

These special modes are activated by software via the Special Function Register PCON. Its hardware address is 87H. PCON is not bit addressable.

	7	6	5	4	3	2	1	0
PCON (87H)	SMOD	–	–	WLE	GF1	GF0	PD	IDL

Bit	Symbol	Function
PCON.7	SMOD	Double Baud rate bit. When set to logic 1 the baud rate is doubled when the serial port SIO0 is being used in modes 1, 2 or 3
PCON.6	–	(reserved)
PCON.5	–	(reserved)
PCON.4	WLE	Watchdog load enable. This flag must be set by software prior to loading T3 (watchdog timer). It is cleared when T3 is loaded
PCON.3	GF1	General-purpose flag bit
PCON.2	GF0	General-purpose flag bit
PCON.1	PD	Power-down bit. Setting this bit activates Power-down mode. It can only be set if input $\overline{EW}$ is high.
PCON.0	IDL	Idle mode bit. Setting this bit activates the Idle mode

If logic 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (0XX00000).

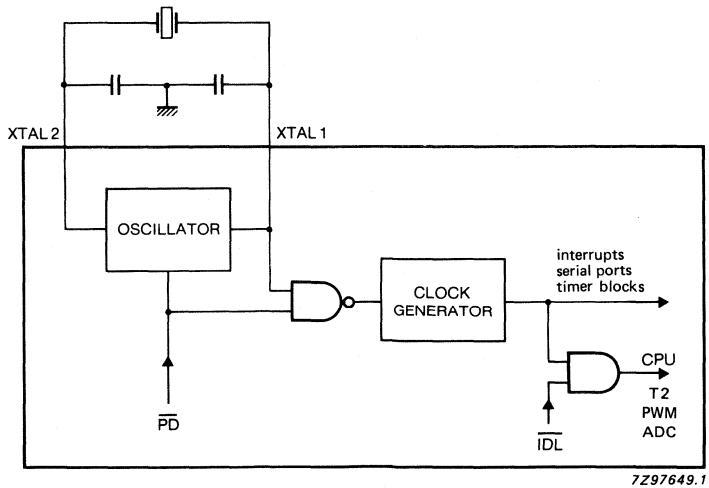


Fig. 12 Internal Idle and Power-down clock configuration.

FUNCTIONAL DESCRIPTION (continued)

Interrupt system (see Fig. 13)

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. Interrupt response latency is from 3 μs to 8 μs when using a 12 MHz crystal. The PCB83C552 acknowledges interrupt requests from fifteen sources as follows:

- $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$: externally via pins 26 and 27 respectively
- INT2 to INT5: externally via pins 16 to 19 respectively. These pins are shared with the four capture inputs of Timer T2.
- Timer 0 and Timer 1: from the two internal counters
- Timer T2 (8 separate interrupts): 4 capture interrupts, 3 compare interrupts and an overflow interrupt
- ADC end-of-conversion interrupt
- I^2C serial I/O port interrupt
- UART serial I/O port interrupt.

Each interrupt vectors to a separate location in program memory for its service program. Each source can be individually enabled or disabled by a corresponding bit in the IE0 or IE1 register, moreover each interrupt may be programmed to a high or low priority level using a corresponding bit in the IP0 or IP1 register. Also all enabled sources can be globally disabled or enabled. Both external interrupts can be programmed to be level-activated or transition-activated, and an active LOW level allows "wire-ORing" of several interrupt sources to the input pin.

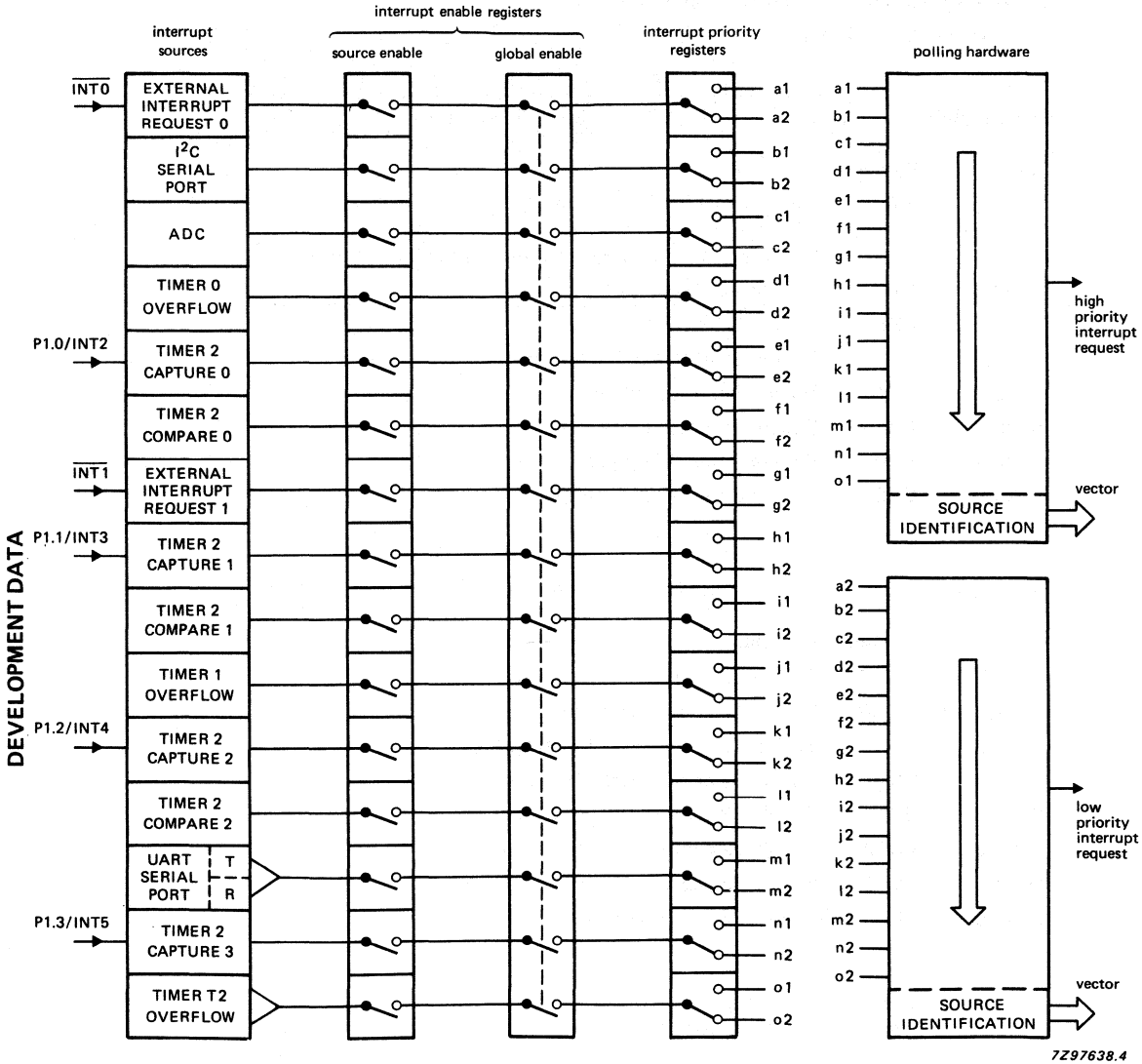


Fig. 13 Interrupt system.

FUNCTIONAL DESCRIPTION (continued)

Interrupt enable registers

	7	6	5	4	3	2	1	0
IEN0 (A8H)	EA	EAD	ES1	ES0	ET1	EX1	ET0	EX0

Bit	Symbol	Function
IEN0.7	EA	General enable/disable control 0 = No interrupt is enabled 1 = Any individually enabled interrupt will be accepted
IEN0.6	EAD	Enable ADC interrupt
IEN0.5	ES1	Enable SIO1 (I^2C) interrupt
IEN0.4	ES0	Enable SIO0 (UART) interrupt
IEN0.3	ET1	Enable Timer 1 interrupt
IEN0.2	EX1	Enable External 1 interrupt
IEN0.1	ET0	Enable Timer 0 interrupt
IEN0.0	EX0	Enable External 0 interrupt

	7	6	5	4	3	2	1	0
IEN1 (E8H)	ET2	ECM2	ECM1	ECM0	ECT3	ECT2	ECT1	ECT0

Bit	Symbol	Function
IEN1.7	ET2	Enable T2 overflow interrupt(s)
IEN1.6	ECM2	Enable T2 comparator 2 interrupt
IEN1.5	ECM1	Enable T2 comparator 1 interrupt
IEN1.4	ECM0	Enable T2 comparator 0 interrupt
IEN1.3	ECT3	Enable T2 capture register 3 interrupt
IEN1.2	ECT2	Enable T2 capture register 2 interrupt
IEN1.1	ECT1	Enable T2 capture register 1 interrupt
IEN1.0	ECT0	Enable T2 capture register 0 interrupt

where 0 = interrupt disabled
and 1 = interrupt enabled

Interrupt priority registers

	7	6	5	4	3	2	1	0
IP0 (B8H)	–	PAD	PS1	PS0	PT1	PX1	PT0	PX0

Bit	Symbol	Function
IP0.7	–	Unused
IP0.6	PAD	ADC interrupt priority level
IP0.5	PS1	SIO1 (I^2C) interrupt priority level
IP0.4	PS0	SIO0 (UART) interrupt priority level
IP0.3	PT1	Timer 1 interrupt priority level
IP0.2	PX1	External interrupt 1 priority level
IP0.1	PT0	Timer 0 interrupt priority level
IP0.0	PX0	External interrupt 0 priority level

	7	6	5	4	3	2	1	0
IP1 (F8H)	PT2	PCM2	PCM1	PCM0	PCT3	PCT2	PCT1	PCT0

Bit	Symbol	Function
IP1.7	PT2	T2 overflow interrupt(s) priority level
IP1.6	PCM2	T2 comparator 2 priority interrupt level
IP1.5	PCM1	T2 comparator 1 priority interrupt level
IP1.4	PCM0	T2 comparator 0 priority interrupt level
IP1.3	PCT3	T2 capture register 3 priority interrupt level
IP1.2	PCT2	T2 capture register 2 priority interrupt level
IP1.1	PCT1	T2 capture register 1 priority interrupt level
IP1.0	PCT0	T2 capture register 0 priority interrupt level

Interrupt priority levels are as follow

0 – low priority
1 – high priority

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Table 3 shows the interrupt vectors. The vector indicates the ROM location where the appropriate interrupt service routine starts.

Table 3 Interrupt vectors

Source		Vector
External 0	X0	0003H
Timer 0 overflow	T0	000BH
External 1	X1	0013H
Timer 1 overflow	T1	001BH
Serial I/O 0 (UART)	S0	0023H
Serial I/O 1 (I^2C)	S1	002BH
T2 capture 0	CT0	0033H
T2 capture 1	CT1	003BH
T2 capture 2	CT2	0043H
T2 capture 3	CT3	004BH
ADC completion	ADC	0053H
T2 compare 0	CM0	005BH
T2 compare 1	CM1	0063H
T2 compare 2	CM2	006BH
T2 overflow	T2	0073H

Interrupt priority

Each interrupt source can be either high priority or low priority. If both priorities are requested simultaneously, the processor will branch to the high priority vector. If there are simultaneous requests from sources of the same priority, then interrupts will be serviced in the following order:

X0, S1, ADC, T0, CT0, CM0, X1, CT1, CM1, T1, CT2, CM2, S0, CT3, T2

A low priority interrupt routine can only be interrupted by a high priority interrupt. A high priority interrupt routine can not be interrupted.

Oscillator circuitry

The oscillator circuitry of the PCB83C552 is a single-stage inverting amplifier in a Pierce oscillator configuration. The circuitry between XTAL 1 and XTAL 2 is basically an inverter biased to the transfer point. Either a crystal or ceramic resonator can be used as the feedback element to complete the oscillator circuitry. Both are operated in parallel resonance. XTAL 1 (pin 35) is the high gain amplifier input, and XTAL 2 (pin 34) is the output (see Fig. 14). To drive the PCB83C552 externally, XTAL 1 is driven from an external source and XTAL 2 left open-circuit (see Fig. 15).

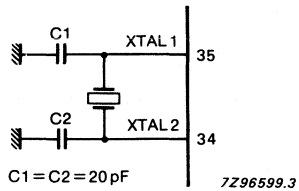


Fig. 14 PCB83C552 oscillator circuit.

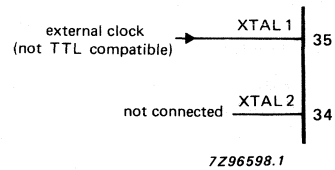


Fig. 15 Driving the PCB83C552 from an external source.

DEVELOPMENT DATA

Reset circuitry (see Fig. 16)

The reset circuitry for the PCB83C552 is connected to the reset pin RST. A Schmitt trigger is used at the input for noise rejection. The output of the Schmitt trigger is sampled by the reset circuitry every machine cycle.

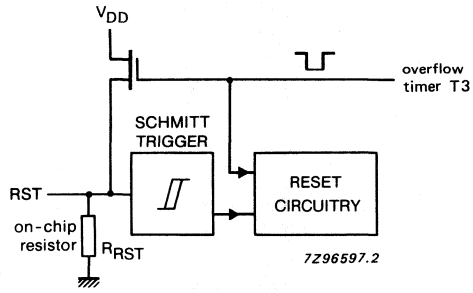


Fig. 16 On-chip reset configuration.

A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods). The CPU responds by executing an internal reset. During reset ALE and $\overline{PSEN}$ output a HIGH level. In order to perform a correct reset, this level must not be affected by external elements.

Also with the PCB83C552, the RST line can be pulled HIGH internally by a pull-up transistor activated by the watchdog timer T3. The length of the output pulse from T3 is 3 machine cycles. A pulse of such short duration is necessary in order to recover from a processor or system fault as fast as possible.

FUNCTIONAL DESCRIPTION (continued)

N.B. It can be seen that the short reset pulse from Timer T3 cannot discharge the power-on reset capacitor (see Fig. 17). Consequently, when the watchdog timer is also used to reset external devices this capacitor arrangement should not be connected to the RST pin, and an extra circuit should be used to perform the power-on reset operation. It should be remembered that a Timer T3 overflow, if enabled, will force a reset condition to the PCB83C552 by an internal connection, whether the output RST is tied LOW or not.

The internal reset is executed during the second cycle in which RST is HIGH and is repeated every cycle until RST goes LOW. It leaves the internal registers as follows:

Register	Content
ACC	0000 0000
ADCON	xx00 0000
ADCH	xxxx xxxx
B	0000 0000
CML0 - CML2	0000 0000
CMH0 - CMH2	0000 0000
CTCON	0000 0000
CTL0 - CTL3	xxxx xxxx
CTH0 - CTH3	xxxx xxxx
DPL	0000 0000
DPH	0000 0000
IEN0	0000 0000
IEN1	0000 0000
IP0	x000 0000
IP1	0000 0000
PCH	0000 0000
PCL	0000 0000
PCON	0xx0 0000
PSW	0000 0000
PWM0	0000 0000
PWM1	0000 0000
PWMP	0000 0000
P0 - P4	1111 1111
P5	xxxx xxxx
RTE	0000 0000
S0BUF	xxxx xxxx
S0CON	0000 0000
S1ADR	0000 0000
S1CON	0000 0000
S1DAT	0000 0000
S1STA	1111 1000
SP	0000 0111
STE	1100 0000
TCON	0000 0000
TH0, TH1	0000 0000
TMH2	0000 0000
TL0, TL1	0000 0000
TML2	0000 0000
TMOD	0000 0000
TM2CON	0000 0000
TM2IR	0000 0000
T3	0000 0000

x = undefined state.

The internal RAM is not affected by reset. When V_{DD} is turned on, the RAM content is indeterminate.

Power-on reset (see Fig. 17)

When V_{DD} is turned on, and provided its rise-time does not exceed 10 ms, an automatic reset can be obtained by connecting the RST pin to V_{DD} via a 2,2 μF capacitor. When the power is switched on, the voltage on the RST pin is equal to V_{DD} minus the capacitor voltage, and decreases from V_{DD} as the capacitor charges through the internal resistor (R_{RST}) to ground. The larger the capacitor, the more slowly V_{RST} decreases. V_{RST} must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles.

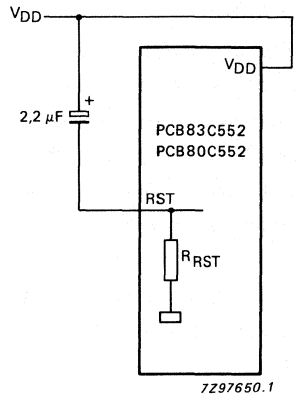


Fig. 17 Power-on reset.

INSTRUCTION SET

Table 4 Instruction set description

mnemonic		description	bytes/ cycles		opcode (hex.)
Arithmetic operations					
ADD	A,Rr	Add register to A	1	1	2*
ADD	A,direct	Add direct byte to A	2	1	25
ADD	A,@Ri	Add indirect RAM to A	1	1	26, 27
ADD	A,#data	Add immediate data to A	2	1	24
ADDC	A,Rr	Add register to A with carry flag	1	1	3*
ADDC	A,direct	Add direct byte to A with carry flag	2	1	35
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A,#data	Add immediate data to A with carry flag	2	1	34
SUBB	A,Rr	Subtract register from A with borrow	1	1	9*
SUBB	A,direct	Subtract direct byte from A with borrow	2	1	95
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A,#data	Subtract immediate data from A with borrow	2	1	94
INC	A	Increment A	1	1	04
INC	Rr	Increment register	1	1	0*
INC	direct	Increment direct byte	2	1	05
INC	@Ri	Increment indirect RAM	1	1	06, 07
DEC	A	Decrement A	1	1	14
DEC	Rr	Decrement register	1	1	1*
DEC	direct	Decrement direct byte	2	1	15
DEC	@Ri	Decrement indirect RAM	1	1	16, 17
INC	DPTR	Increment data pointer	1	2	A3
MUL	AB	Multuply A & B	1	4	A4
DIV	AB	Divide A by B	1	4	84
DA	A	Decimal adjust A	1	1	D4

mnemonic		description	bytes/ cycles		opcode (hex.)
Logic operations					
ANL	A,Rr	AND register to A	1	1	5*
ANL	A,direct	AND direct byte to A	2	1	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	1	54
ANL	direct,A	AND A to direct byte	2	1	52
ANL	direct,#data	AND immediate data to direct byte	3	2	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	1	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	1	44
ORL	direct, A	OR A to direct byte	2	1	42
ORL	direct,#data	OR immediate data to direct byte	3	2	43
XRL	A,Rr	Exclusive-OR register to A	1	1	6*
XRL	A,direct	Exclusive-OR direct byte to A	2	1	65
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	Exclusive-OR immediate data to A	2	1	64
XRL	direct,A	Exclusive-OR A to direct byte	2	1	62
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2	63
CLR	A	Clear A	1	1	E4
CPL	A	Complement A	1	1	F4
RL	A	Rotate A left	1	1	23
RLC	A	Rotate A left through the carry flag	1	1	33
RR	A	Rotate A right	1	1	03
RRC	A	Rotate A right through the carry flag	1	1	13
SWAP	A	Swap nibbles within A	1	1	C4

INSTRUCTION SET (continued)

mnemonic		description	bytes/ cycles		opcode (hex.)
Data transfer					
MOV	A,Rr	Move register to A	1	1	E*
MOV	A,direct**	Move direct byte to A	2	1	E5
MOV	A,@Ri	Move indirect RAM to A	1	1	E6, E7
MOV	A,#data	Move immediate data to A	2	1	74
MOV	Rr,A	Move A to register	1	1	F*
MOV	Rr,direct	Move direct byte to register	2	2	A*
MOV	Rr,#data	Move immediate data to register	2	1	7*
MOV	direct,A	Move A to direct byte	2	1	F5
MOV	direct,Rr	Move register to direct byte	2	2	8*
MOV	direct,direct	Move direct byte to direct byte	3	2	85
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	Move immediate data to direct byte	3	2	75
MOV	@Ri,A	Move A to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1	76, 77
MOV	DPTR,#data16	Load data pointer with a 16-bit constant	3	2	90
MOVC	A,@A+DPTR	Move code byte relative to DPTR to A	1	2	93
MOVC	A,@A+PC	Move code byte relative to PC to A	1	2	83
MOVX	A,@Ri	Move external RAM (8-bit address) to A	1	2	E2, E3
MOVX	A,@DPTR	Move external RAM (16-bit address) to A	1	2	E0
MOVX	@Ri,A	Move A to external RAM (8-bit address)	1	2	F2, F3
MOVX	@DPTR,A	Move A to external RAM (16-bit address)	1	2	F0
PUSH	direct	Push direct byte onto stack	2	2	C0
POP	direct	Pop direct byte from stack	2	2	D0
XCH	A,Rr	Exchange register with A	1	1	C*
XCH	A,direct	Exchange direct byte with A	2	1	C5
XCH	A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD	A,@Ri	Exchange LOW-order nibble indirect RAM with A	1	1	D6, D7

** MOV A,ACC is not a valid instruction.

mnemonic		description	bytes/ cycles		opcode (hex.)
Boolean variable manipulation					
CLR	C	Clear carry flag	1	1	C3
CLR	bit	Clear direct bit	2	1	C2
SETB	C	Set carry flag	1	1	D3
SETB	bit	Set direct bit	2	1	D2
CPL	C	Complement carry flag	1	1	B3
CPL	bit	Complement direct bit	2	1	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C,bit	OR direct bit to carry flag	2	2	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C,bit	Move direct bit to carry flag	2	1	A2
MOV	bit,C	Move carry flag to direct bit	2	2	92
Program and machine control					
ACALL	addr11	Absolute subroutine call	2	2	●1addr
LCALL	addr16	Long subroutine call	3	2	12
RET		Return from subroutine	1	2	22
RETI		Return from interrupt	1	2	32
AJMP	addr11	Absolute jump	2	2	▲1addr
LJMP	addr16	Long jump	3	2	02
SJMP	rel	Short jump (relative address)	2	2	80
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2	73
JZ	rel	Jump if A is zero	2	2	60
JNZ	rel	Jump if A is not zero	2	2	70
JC	rel	Jump if carry flag is set	2	2	40
JNC	rel	Jump if carry flag is not set	2	2	50
JB	bit,rel	Jump if direct bit is set	3	2	20
JNB	bit,rel	Jump if direct bit is not set	3	2	30
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2	10
CJNE	A,direct,rel	Compare direct to A and jump if not equal	3	2	B5
CJNE	A,#data,rel	Compare immediate to A and jump if not equal	3	2	B4
CJNE	Rr,#data,rel	Compare immediate to reg. and jump if not equal	3	2	B*
CJNE	@Ri,#data,rel	Compare immediate to ind. and jump if not equal	3	2	B6, B7
DJNZ	Rr,rel	Decrement register and jump if not zero	2	2	D*
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2	D5
NOP		No operation	1	1	00

DEVELOPMENT DATA

Notes to Table 4

Data addressing modes

Rr	Working register R0-R7.
direct	128 internal RAM locations and any special function register (SFR).
@Ri	Indirect internal RAM location addressed by register R0 or R1 of the actual register bank.
#data	8-bit constant included in instruction.
#data16	16-bit constant included as bytes 2 and 3 of instruction.
bit	direct addressed bit in internal RAM or SFR.
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 K-byte program memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 K-byte page of program memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is −128 to + 127 bytes relative to first byte of the following instruction.

Hexadecimal opcode cross-reference to Table 4

* : 8, 9, A, B, C, D, E, F.
● : 11, 31, 51, 71, 91, B1, D1, F1.
▲ : 01, 21, 41, 61, 81, A1, C1, E1.

Table 5 Instruction map

first hexadecimal character of opcode ↓ — second hexadecimal character of opcode →

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC dir	INC @Ri 0	1	INC Rr 0	1	2	3	4	5	6	7
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC dir	DEC @Ri 0	1	DEC Rr 0	1	2	3	4	5	6	7
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,dir	ADD A,@Ri 0	1	ADD A,Rr 0	1	2	3	4	5	6	7
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,dir	ADDC A,@Ri 0	1	ADDC A,Rr 0	1	2	3	4	5	6	7
4	JC rel	AJMP addr11	ORL dir,A	ORL dir,#data	ORL A,#data	ORL A,dir	ORL A,@Ri 0	1	ORL A,Rr 0	1	2	3	4	5	6	7
5	JNC rel	ACALL addr11	ANL dir,A	ANL dir,#data	ANL A,#data	ANL A,dir	ANL A,@Ri 0	1	ANL A,Rr 0	1	2	3	4	5	6	7
6	JZ rel	AJMP addr11	XRL dir,A	XRL dir,#data	XRL A,#data	XRL A,dir	XRL A,@Ri 0	1	XRL A,Rr 0	1	2	3	4	5	6	7
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV dir,#data	MOV @Ri,#data 0	1	MOV Rr,#data 0	1	2	3	4	5	6	7
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV dir,dir	MOV dir,@Ri 0	1	MOV dir,Rr 0	1	2	3	4	5	6	7
9	MOV DPTR, #data 16	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,dir	SUBB A,@Ri 0	1	SUBB A,Rr 0	1	2	3	4	5	6	7
A	ORL C,/bit	AJMP addr11	MOV C,bit	INC DPTR	MUL AB		MOV @Ri,dir 0	1	MOV Rr,dir 0	1	2	3	4	5	6	7
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A, #data, rel	CJNE A,dir,rel	CJNE @Ri,#data, rel 0	1	CJNE Rr,#data, rel 0	1	2	3	4	5	6	7
C	PUSH dir	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,dir	XCH A,@Ri 0	1	XCH A,Rr 0	1	2	3	4	5	6	7
D	POP dir	ACALL addr11	SETB bit	SETB C	DA A	DJNZ dir,rel	XCHD A,@Ri 0	1	DJNZ Rr, rel 0	1	2	3	4	5	6	7
E	MOVX A,@DPTR	AJMP addr11	MOVX A,@Ri 0	1	CLR A	MOV A,dir *	MOV A,@Ri 0	1	MOV A,Rr 0	1	2	3	4	5	6	7
F	MOVX @DPTR,A	ACALL addr11	MOVX @Ri,A 0	1	CPL A	MOV dir,A	MOV @Ri,A 0	1	MOV Rr,A 0	1	2	3	4	5	6	7

* MOV A,ACC is not a valid instruction.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Input voltage on any pin with respect to ground (V_{SS})	V_I	−0.5	+ 6.5	V
Input, output current	I_I, I_O	–	5.0	mA
Input, output current on any single pin	I_I, I_O	–	10.0	mA
Total power dissipation	P_{tot}	–	1.0	W
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range				
PCB83C552	T_{amb}	0	+ 70	°C
PCF83C552	T_{amb}	−40	+ 85	°C
PCA83C552	T_{amb}	−40	+ 125	°C

* Value to be fixed.

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 5 V (± 10%); V_{SS} = 0 V; T_{amb} = 0 to 70 °C (PCB83C552); −40 to + 85 °C (PCF83C552); −40 to + 125 °C (PCA83C552).

parameter	conditions	symbol	min.	max.	unit
Supply voltage	T_{amb} = 0 to + 70 °C	V_{DD}	4.0	6.0	V
	T_{amb} = −40 to + 80 °C	V_{DD}	4.0	6.0	V
	T_{amb} = −40 to + 125 °C	V_{DD}	4.5	5.5	V
Supply current operating	(note 1) f_{CLK} = 12 MHz; V_{DD} = 6.0 V	I_{DD}	–	34	mA
	f_{CLK} = 12 MHz; V_{DD} = 6.0 V	I_{DD}	–	30	mA
	(note 2) f_{CLK} = 12 MHz; V_{DD} = 5 V + 20%	I_{DD}	–	8	mA
	f_{CLK} = 12 MHz; V_{DD} = 5 V + 10%	I_{DD}	–	7	mA
Power-down current	2 V < V_{PD} < V_{DD} max.; (note 3)				
	T_{amb} = −40 to + 85 °C	I_{PD}	–	50	μA
	T_{amb} = −40 to + 125 °C	I_{PD}	–	100	μA
Inputs					
LOW level input voltage (except $\overline{EA}$, P1.6/SCL, P1.7/SDA)		V_{IL}	−0.5	$0.2V_{DD}$−0.1	V
LOW level input voltage ($\overline{EA}$)		V_{IL1}	−0.5	$0.2V_{DD}$−0.3	V
HIGH level input voltage (except RST, XTAL1, P1.6/SCL, P1.7/SDA)		V_{IH}	$0.2V_{DD}$+0.9	V_{DD}+0.5	V
LOW level input voltage (P1.6/SCL, P1.7/SDA)		V_{IL2}	−0.5	$0.3V_{DD}$	V
HIGH level input voltage (RST and XTAL1)		V_{IH1}	$0.7V_{DD}$	V_{DD}+0.5	V
HIGH level input voltage (P1.6/SCL, P1.7/SDA)		V_{IH2}	$0.7V_{DD}$	6.0	V
Input current logic 0 (Ports 1, 2, 3 and 4; except P1.6/SDA, P1.7/SCL)	V_I = 0.45 V	$-I_{IL}$	–	50	μA
Input current logic 1 to 0 transition (Ports 1, 2, 3 and 4; except P1.6/SCL, P1.7/SDA)	V_I = 2.0 V	$-I_{TL}$	–	650	μA

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	max.	unit
Input leakage current (Port 0, Port 5, $\overline{EA}$, STADC, $\overline{EW}$)	0,45 V < V_I < V_{DD}	$\pm I_{LI1}$	–	10	μA
Input leakage current (P1.6/SCL, P1.7/SDA)	0 V < V_I < 6.0 V 0 V < V_I < 6.0 V	$\pm I_{LI2}$	–	10	μA
Outputs					
LOW level output voltage (Ports 1, 2, 3 and 4; except P1.6/SCL, P1.7/SDA)	(note 10) I_{OL} = 1.6 mA	V_{OL}	–	0.45	V
LOW level output voltage (Port 0, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$)	(note 10) I_{OL} = 3.2 mA	V_{OL1}	–	0.45	V
LOW level output voltage (P1.6/SCL, P1.7/SDA)	I_{OL} = 3.0 mA	V_{OL2}	–	0.40	V
HIGH level output voltage (Ports 1, 2, 3 and 4; except P1.6/SCL, P1.7/SDA)	V_{DD} = 5 V + 10% $-I_{OH}$ = 60 μA $-I_{OH}$ = 25 μA $-I_{OH}$ = 10 μA	V_{OH} V_{OH} V_{OH}	2.4 0.75V_{DD} 0.9V_{DD}	– – –	V V V
HIGH level output voltage (Port 0 in external bus mode, ALE, $\overline{PSEN}$, $\overline{PWM0}$, $\overline{PWM1}$)	(note 11) V_{DD} = 5 V + 10% $-I_{OH}$ = 400 μA $-I_{OH}$ = 150 μA $-I_{OH}$ = 40 μA	V_{OH1} V_{OH1} V_{OH1}	2.4 0.75V_{DD} 0.9V_{DD}	– – –	V V V
HIGH level output voltage (RST)	$-I_{OH}$ = 400 μA $-I_{OH}$ = 120 μA	V_{OH2} V_{OH2}	2.4 0.8V_{DD}	– –	V V
RST pull-down resistor		R_{RST}	50	150	kΩ
Capacitance of I/O buffer	Test freq. = 1 MHz T_{amb} = 25 °C	$C_{I/O}$	–	10	pF

DEVELOPMENT DATA

DC CHARACTERISTICS

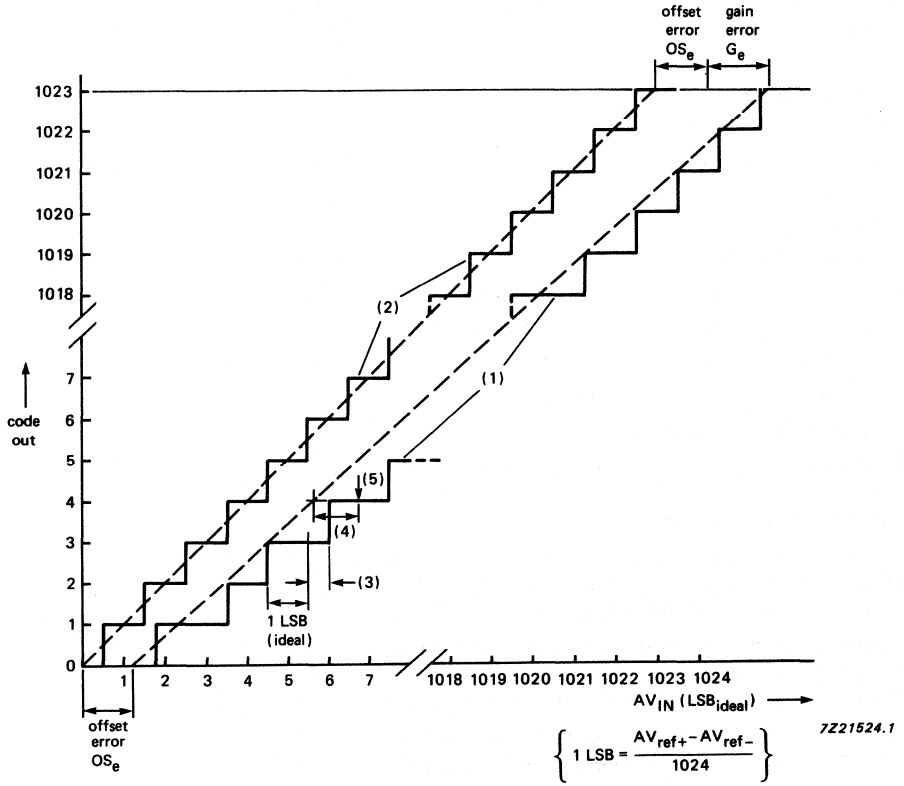
parameter	conditions	symbol	min.	max.	unit
Analogue inputs	(note 10)				
Analogue supply voltage	$AV_{DD} = V_{DD} \pm 0.2$ V	AV_{DD}	4.0	6.0	V
Analogue supply current operating	Port 5 = 0 to AV_{DD}	AI_{DD}	–	1.2	mA
Idle mode	$T_{amb} = -40$ to + 85 °C	AI_{ID}	–	50	μA
	$T_{amb} = -40$ to + 125 °C	AI_{ID}	–	100	μA
Power-down	$2\ V < AV_{PD} < A_{VDD}$ max				
	$T_{amb} = -40$ to + 85 °C	AI_{PD}	–	50	μA
	$T_{amb} = -40$ to + 125 °C	AI_{PD}	–	100	μA
Analogue input voltage		AV_{IN}	$AV_{SS}-0.2$	$AV_{DD}+0.2$	V
Reference voltage		AV_{REF-}	$AV_{SS}-0.2$	–	V
		AV_{REF+}	–	$AV_{DD}+0.2$	V
Resistance between AV_{REF+} and AV_{REF-}		R_{REF}	10	50	kΩ
Analogue input capacitance		C_{IA}	–	15	pF
Sampling time		t_{ADS}	–	$8t_{CY}$	μs
Conversion time (including sample time)		t_{ADC}	–	$50t_{CY}$	μs
Differential non-linearity	(note 4 and 5)	DL_e	–	$-1 < DL_e < 2$	LSB
Integral non-linearity	(note 4 and 6)	IL_e	–	± 2	LSB
Offset error	(note 9)	OS_e	–	± 2	mV
Gain error	(note 7)	G_e	–	± 0.4	%
Channel to channel matching		M_{ctc}	–	± 1	LSB
Crosstalk	0 to 100 kHz (note 8)	C_t	–	–60	dB

Notes to the DC characteristics

1. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10$ ns; $V_{IL} = V_{SS} + 0.5$ V; $V_{IH} = V_{DD} - 0.5$ V; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = $\overline{EW}$ = V_{DD}; STADC = V_{SS}.
2. The Idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10$ ns; $V_{IL} = V_{SS} + 0.5$ V; $V_{IH} = V_{DD} - 0.5$ V; XTAL2 not connected; $\overline{EA}$ = Port 0 = $\overline{EW}$ = V_{DD}; RST = STADC = V_{SS}.
3. The power-down current is measured with all output pins disconnected; XTAL2 not connected; $\overline{EA}$ = Port 0 = $\overline{EW}$ = V_{DD}; RST = STADC = V_{SS}.
4. $AV_{REF+} = 5.12$ V; $AV_{REF-} = 0$ V; $AV_{DD} = 5.0$ V.
5. DLe: The differential non-linearity is the difference between the actual step width and the ideal step width.
6. ILe: The integral non-linearity is the peak difference between the actual and the ideal quantization levels after appropriate adjustment of gain and offset error.
7. The gain error is the relative difference in per cent between the straight line fitting the actual transfer curve (after removing gain error), and the straight line which fits the ideal transfer curve. Gain error is constant at every point on the transfer curve.
8. This should be considered when both analogue and digital signals are input simultaneously.

Notes to the DC characteristics (continued)

9. OSe: The offset error is the absolute difference between the straight line which fits the actual transfer curve (after removing gain error), and a straight line which fits the ideal transfer curve. For an uncalibrated A/D converter, the offset error is constant at every point of the actual transfer curve.
10. Capacitive loading on Port 0 and Port 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1 and Port 3. This noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make a 1-to-0 transition during bus operations. In the most adverse condition (capacitive loading > 100 pF) the noise pulse on ALE may exceed 0.8 V. In this event it may be necessary to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger STROBE input.
11. When the address bits are stabilizing, capacitive loading on Port 0 and Port 2 may cause the HIGH level output voltage on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{DD} specification.
12. The ADC is monotonic; there are no missing codes.



(1) Actual step curve.
(2) Ideal step curve.
(3) Differential non-linearity.
(4) Integral non-linearity.
(5) Centre of step.

Fig.18 ADC conversion characteristic.

After alignment of the offset and gain errors the integral non-linearity is equal to the absolute error.

DEVELOPMENT DATA

AC CHARACTERISTICS

V_{DD} = 5 V ± 20% (PCB83C552), V_{SS} = 0 V, $t_{CK\ min} = 1/f_{max}$ (maximum operating frequency)
V_{DD} = 5 V ± 20% (PCF83C552), V_{SS} = 0 V, $t_{CK\ min} = 1/f_{max}$ (maximum operating frequency)
V_{DD} = 5 V ± 10% (PCA83C552), V_{SS} = 0 V, $t_{CK\ min} = 1/f_{max}$ (maximum operating frequency)
T_{amb} = 0 to + 70 °C, $t_{CK\ min}$ = 83 ns (PCB83C552, see note 1)
T_{amb} = −40 to + 85 °C, $t_{CK\ min}$ = 83 ns (PCF83C552, see note 1)
T_{amb} = −40 to + 125 °C, $t_{CK\ min}$ = 83 ns (PCA83C552, see note 1)
C_L = 100 pF for Port 0, ALE and $\overline{PSEN}$; C_L = 80 pF for all other outputs unless otherwise specified.
(See waveforms Figs 21, 22 and 23).

parameter	symbol	10 MHz		12 MHz		variable clock		unit
		min.	max.	min.	max.	min.	max.	
Program memory								
ALE pulse duration	t_{LL}	160	–	127	–	$2t_{CK}-40$	–	ns
Address set-up time to ALE	t_{AL}	45	–	28	–	$t_{CK}-55$	–	ns
Address hold time after ALE	t_{LA}	65	–	48	–	$t_{CK}-35$	–	ns
Time from ALE to valid instruction input	t_{LIV}	–	300	–	233	–	$4t_{CK}-100$	ns
Time from ALE to control pulse $\overline{PSEN}$	t_{LC}	60	–	43	–	$t_{CK}-40$	–	ns
Control pulse duration $\overline{PSEN}$	t_{CC}	255	–	205	–	$3t_{CK}-45$	–	ns
Time from $\overline{PSEN}$ to valid instruction input	t_{CIV}	–	195	–	145	–	$3t_{CK}-105$	ns
Input instruction hold time after $\overline{PSEN}$	t_{CI}	0	–	0	–	0	–	ns
Input instruction float delay after $\overline{PSEN}$	t_{CIF}	–	75	–	59	–	$t_{CK}-25$	ns
Address to valid instruction input	t_{AIV}	–	395	–	312	–	$5t_{CK}-105$	ns
Address float delay after $\overline{PSEN}$	t_{AFC}	–	10	–	10	–	10	ns

AC CHARACTERISTICS (continued)

parameter	symbol	10 MHz		12 MHz		variable clock		unit
		min.	max.	min.	max.	min.	max.	
External data memory								
RD pulse duration	t_{RR}	500	–	400	–	$6t_{CK}-100$	–	ns
WR pulse duration	t_{WW}	500	–	400	–	$6t_{CK}-100$	–	ns
Address set up time to ALE	t_{AL}	65	–	48	–	$t_{CK}-40$	–	ns
Address hold time after ALE	t_{LA}	–	–	48	–	$t_{CK}-35$	–	ns
RD to valid data input	t_{RD}	–	355	–	252	–	$5t_{CK}-165$	ns
Data hold time after $\overline{RD}$	t_{DR}	0	–	0	–	0	–	ns
Data float delay after $\overline{RD}$	t_{DFR}	–	130	–	97	–	$2t_{CK}-70$	ns
Time from ALE to valid data input	t_{LD}	–	650	–	517	–	$8t_{CK}-150$	ns
Address to valid data input	t_{AD}	–	735	–	585	–	$9t_{CK}-165$	ns
Time from ALE to $\overline{RD}$ or $\overline{WR}$	t_{LW}	250	350	200	300	$3t_{CK}-50$	$3t_{CK}+50$	ns
Time from address to $\overline{RD}$ or $\overline{WR}$	t_{AW}	270	–	203	–	$4t_{CK}-130$	–	ns
Time from $\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	t_{WHLH}	60	140	43	123	$t_{CK}-40$	$t_{CK}+40$	ns
Data valid to $\overline{WR}$ transition	t_{DWX}	40	–	23	–	$t_{CK}-60$	–	ns
Data set-up time before $\overline{WR}$	t_{DW}	550	–	433	–	$7t_{CK}-150$	–	ns
Data hold time after $\overline{WR}$	t_{WD}	50	–	33	–	$t_{CK}-50$	–	ns
Address float delay after $\overline{RD}$	t_{AFR}	–	0	–	0	–	0	ns

Note to AC characteristics

The maximum and minimum operating frequency for all versions is 12 MHz and 1.2 MHz respectively.

Where:

$1/t_{CK}$ = 1.2 to 12 MHz (see Fig.20 and Table 6).

$t_{CY} = 12\ t_{CK}$ (see Fig.21 and DC Characteristics).

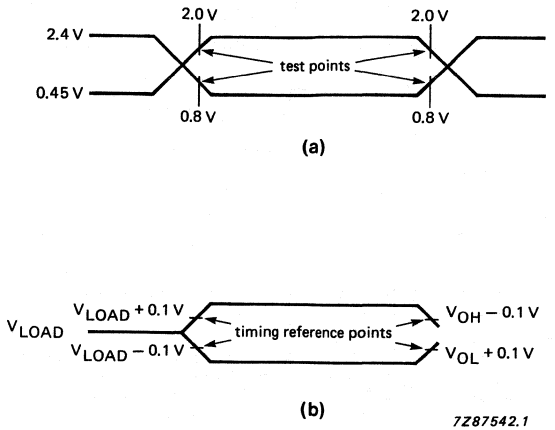


Fig. 19 AC testing input, output waveform (a) and float waveform (b).

DEVELOPMENT DATA

AC testing inputs are driven at 2,4 V for a logic 1 and 0,45 V for a logic 0. Timing measurements are taken at 2,0 V for a logic 1 and 0,8 V for logic 0. The float state is defined as the point at which a Port 0 pin sinks 3,2 mA or sources 400 μA at the voltage test levels.

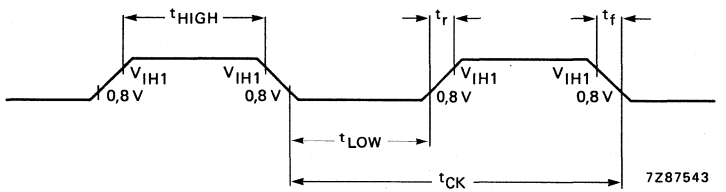


Fig. 20 External clock drive XTAL 1 (see Table 6).

Table 6 External clock drive XTAL 1 (see Fig. 20).

parameter	symbol	variable clock (f = 1,2 to 12 MHz)		unit
		min.	max.	
oscillator clock period	t_{CK}	83,3	833.3	ns
HIGH time	t_{HIGH}	20	t_{CK}-t_{LOW}	ns
LOW time	t_{LOW}	20	t_{CK}-t_{HIGH}	ns
rise time	t_r	–	20	ns
fall time	t_f	–	20	ns
cycle time	t_{CY}1	1	10	μs

1. $t_{CY} = 12t_{CK}$.

AC CHARACTERISTICS (continued)

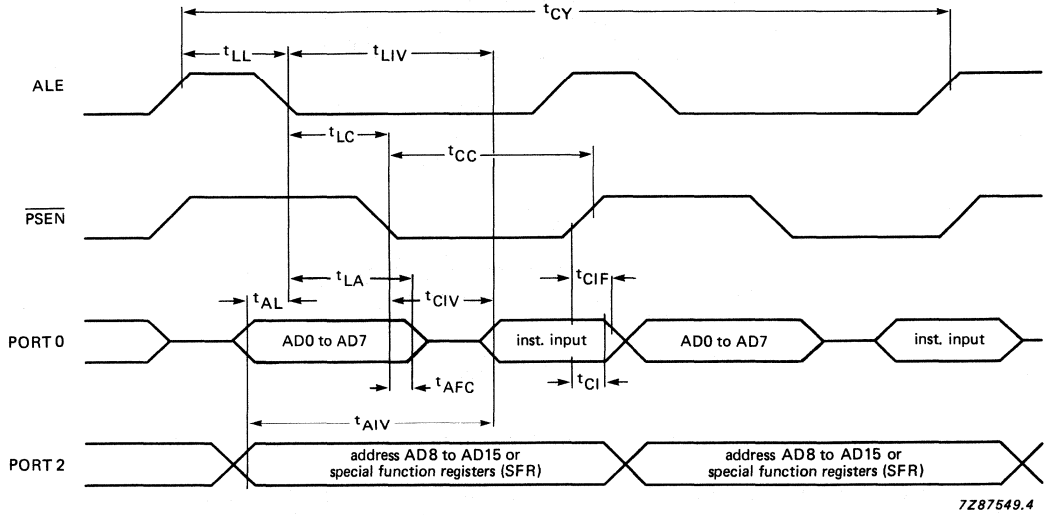


Fig. 21 Read from program memory.

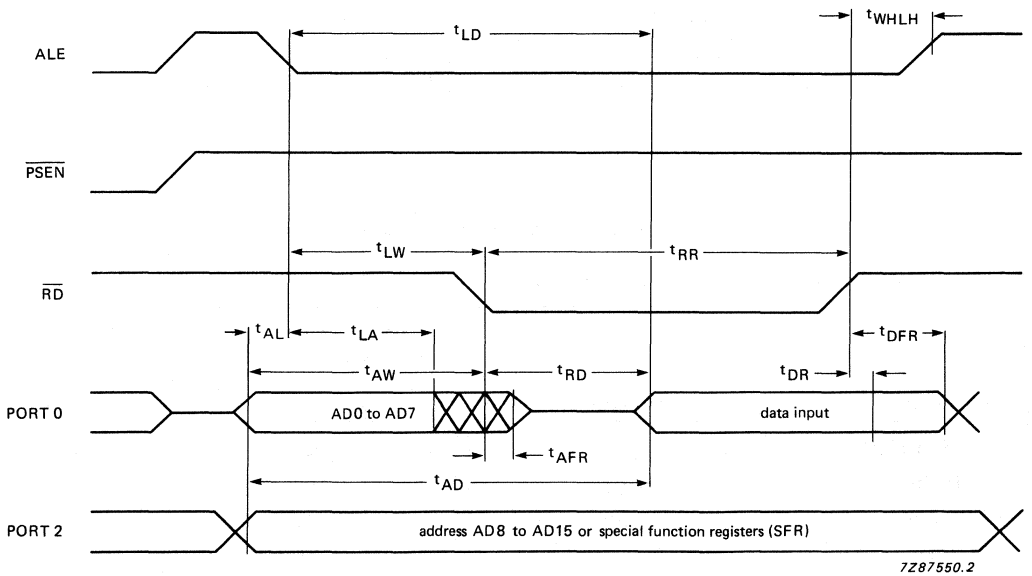


Fig. 22 Read from data memory.

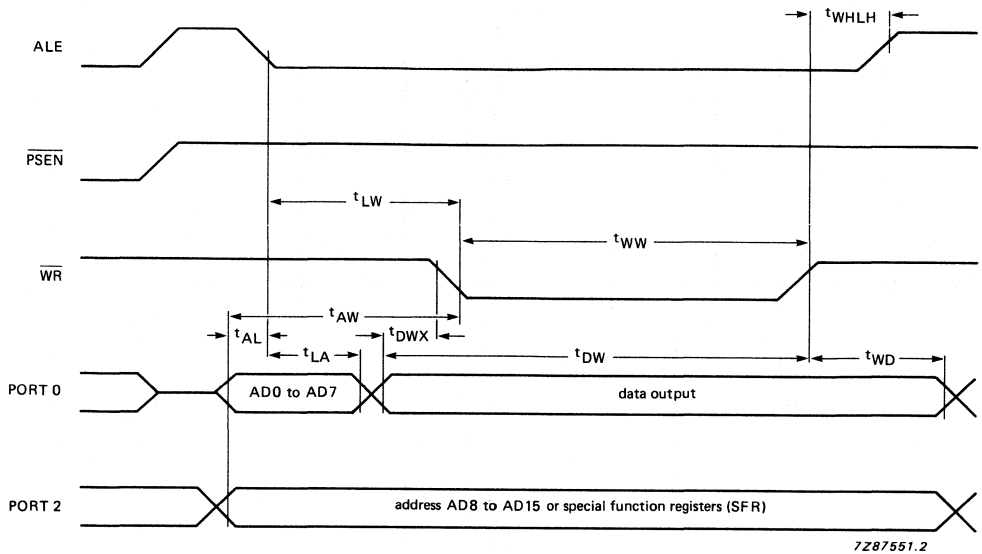


Fig. 23 Write to data memory.

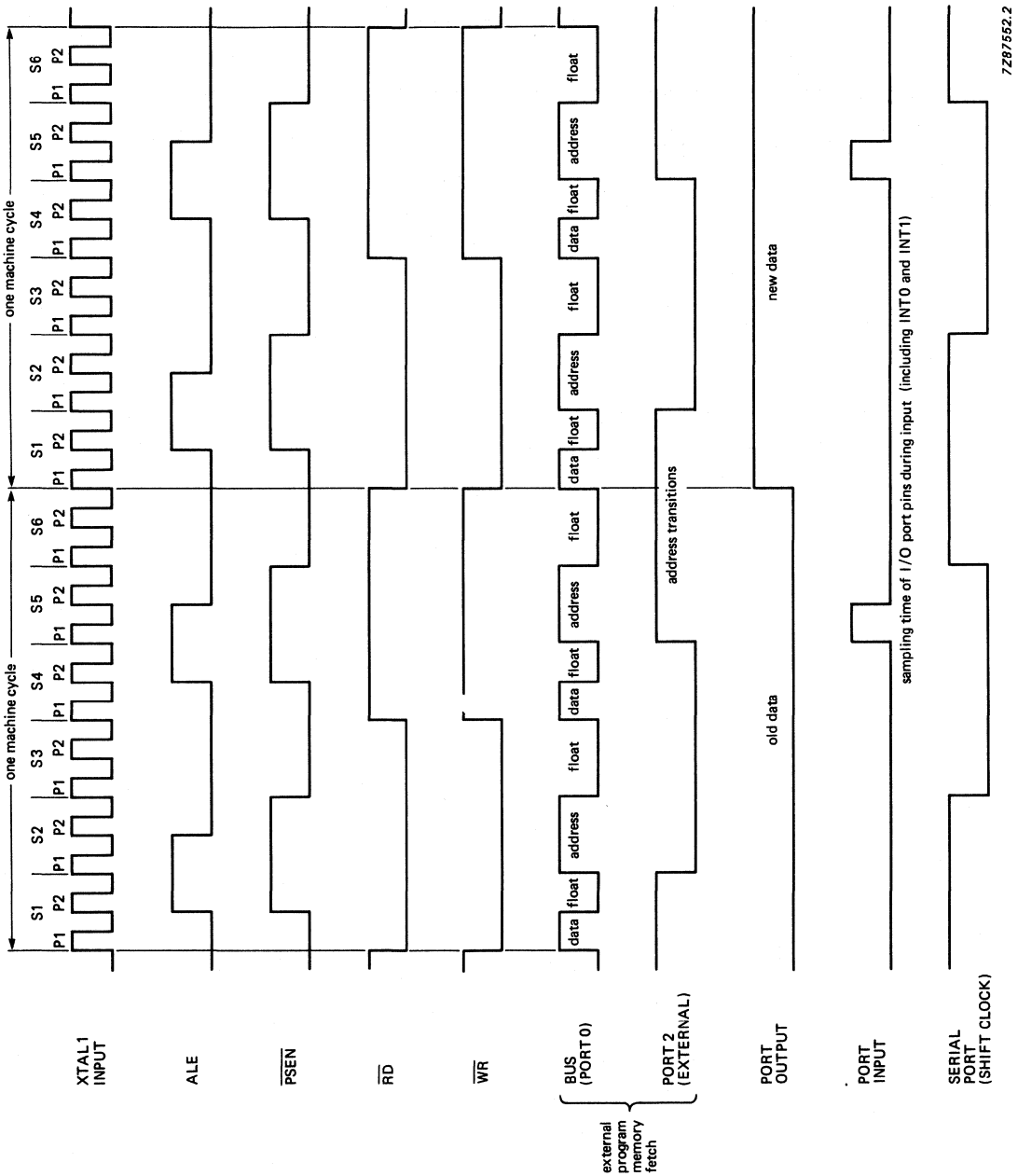


Fig. 24 Instruction cycle timing.

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C652 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The PCB83C652 has the same instruction set as the PCB80C51. Two versions of the derivative exist although the generic term "PCB83C652" is used to refer to both family members:

- PCB83C652: 8 K bytes mask-programmable ROM, 256 bytes RAM
- PCB80C652: ROM-less version of the PCB83C652

This device provides architectural enhancements that make it applicable in a variety of applications in general control systems.

The PCB83C652 contains a non-volatile 8 K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C652 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.

Features

- 80C51 central processing unit
- 8 K x 8 ROM, expandable externally to 64 K bytes
- 256 x 8 RAM, expandable externally to 64 K bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART facilities
  Three temperature ranges available
  0 to + 70 °C; PCB83C652 versions
  −40 to + 85 °C; PCF83C652 versions
  −40 to + 125 °C; PCA83C652 versions
- Extended frequency range: 1.2 MHz to 12 MHz

PACKAGE OUTLINES

PCA/PCB/PCF83C652P; PCA/PCB/PCF80C652P: 40-lead DIL; plastic (SOT129).
PCA/PCB/PCF83C652WP; PCA/PCB/PCF80C652WP: 44-lead plastic leaded-chip-carrier (PLCC) (SOT187 pedestal or SOT187AA pocket versions, these are interchangeable).
PCA/PCB/PCF83C652H; PCA/PCB/PCF80C652H: 44-lead quad flat-pack (QFP). This is in preparation.

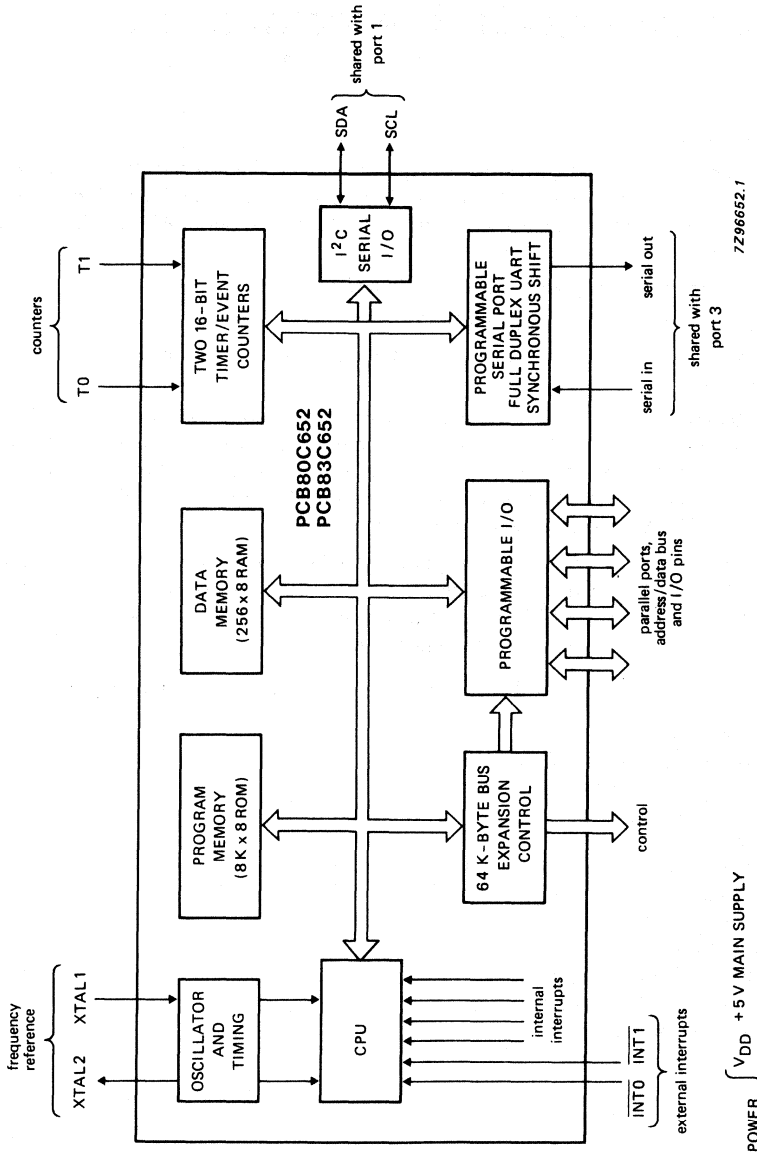


Fig. 1 Block diagram.

DEVELOPMENT DATA

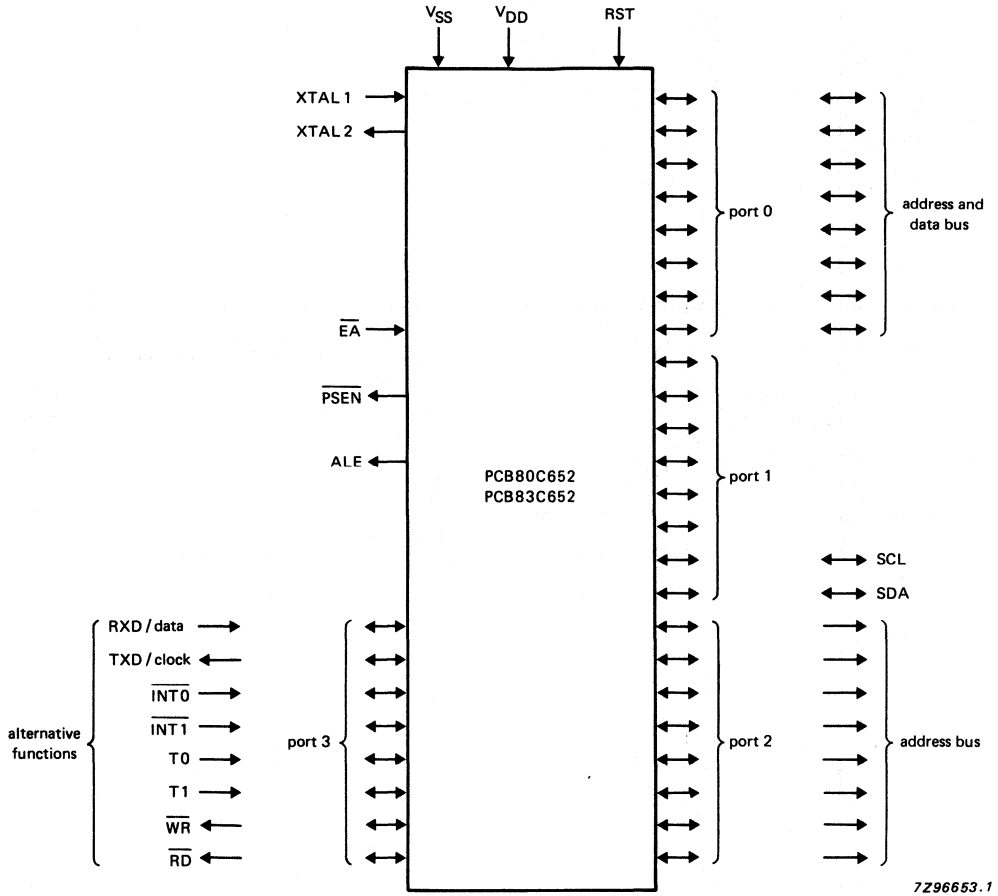


Fig. 2 Functional diagram.

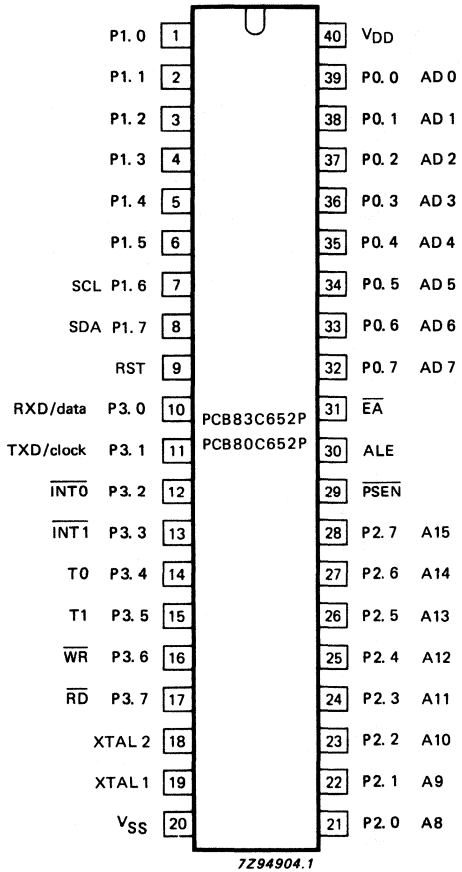


Fig. 3a Pinning diagram for 40-lead DIL package (SOT129).

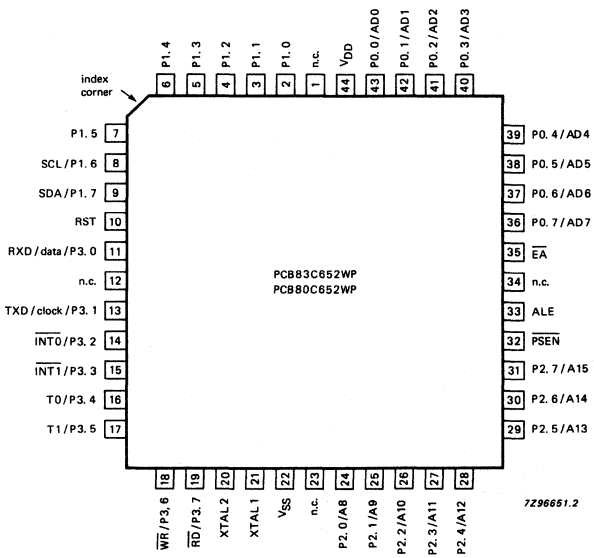


Fig. 3b Pinning diagram for 44-lead PLCC package (SOT187).

PINNING (PCB83C652P, PCB80C652P)

1-8	P1.0-P1.7	**Port 1:** 8-bit quasi-bidirectional I/O port. Port 1 can sink/source one TTL (= 4 LSTTL) input. It can drive CMOS inputs without external pull-ups, except P1.6 and P1.7 which have open drain outputs. Port pin — Alternative function P1.6 — SCL: I^2C-bus serial port clock line P1.7 — SDA: I^2C-bus serial port data line
9	RST	**RESET:** a high level on this pin for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to V_{DD}.

10-17	P3.0-P3.7	**Port 3:** 8-bit quasi-bidirectional I/O port with internal pull-ups. It also serves the following alternative functions:

Port pin	Alternative function
P3.0	RXD/data: serial port receiver data input (asynchronous) or data input/output (synchronous)
P3.1	TXD/clock: serial port transmitter data output (asynchronous) or clock output (synchronous)
P3.2	$\overline{INT0}$: external interrupt 0 or gate control input for timer/event counter 0
P3.3	$\overline{INT1}$: external interrupt 1 or gate control input for timer/event counter 1
P3.4	T0: external input for timer/event counter 0
P3.5	T1: external input for timer/event counter 1
P3.6	$\overline{WR}$: external data memory write strobe
P3.7	$\overline{RD}$: external data memory read strobe

The generation or use of a Port 3 pin as an alternative function is carried out automatically by the PCB83C652 provided the associated Special Function Register bit is set high. Port 3 can sink/source one TTL (= 4 LSTTL) input. It can drive CMOS inputs without external pull-ups.

18	XTAL 2	**Crystal input 2:** output of the inverting amplifier that forms the oscillator. Left open-circuit when an external oscillator clock is used (see Figs 10 and 11).
19	XTAL 1	**Crystal input 1:** input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external oscillator clock signal when an external oscillator is used (see Figs 10 and 11).
20	V_{SS}	**Ground:** circuit ground potential.
21-28	P2.0-P2.7	**Port 2:** 8-bit quasi-bidirectional I/O port with internal pull-ups. During access to external memories (RAM/ROM) that use 16-bit addresses (MOVX @DPTR) Port 2 emits the high order address byte. When external RAM is accessed with an 8-bit address (MOVX @Ri) Port 2 emits the contents of the P2 special function register. Port 2 can sink/source one TTL (= 4 LSTTL) input. It can drive CMOS inputs without external pull-ups.
29	$\overline{PSEN}$	**Program Store Enable output:** read strobe to the external program memory via Port 0 and 2. It is activated twice each machine cycle during fetches from external program memory. When executing out of external program memory two activations of $\overline{PSEN}$ are skipped during each access to external data memory. $\overline{PSEN}$ is not activated (remains HIGH) during no fetches from external program memory. $\overline{PSEN}$ can sink/source 8 LSTTL inputs. It can drive CMOS inputs without an external pull-up.
30	ALE	**Address Latch Enable output:** latches the low byte of the address during accesses to external memory in normal operation. It is activated every six oscillator periods except during an external data memory access. ALE can sink/source 8 LSTTL inputs. It can drive CMOS inputs without an external pull-up.

DEVELOPMENT DATA

PINNING (continued)

31	$\overline{EA}$	**External Access input:** When $\overline{EA}$ is held at a TTL high level the CPU executes out of the internal program ROM provided the program counter is less than 8192. When $\overline{EA}$ is held at a TTL low level, the CPU executes out of external program memory via Port 0 and Port 2. $\overline{EA}$ is not allowed to float.
32-39	P0.7-P0.0	**Port 0:** 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus during accesses to external memory (during these accesses it activates internal pull-ups). Port 0 can sink/source eight LSTTL inputs.
40	V_{DD}	**Power supply:** + 5 V power supply pin during normal operation, Idle mode and Power-down mode.

To avoid a 'latch-up' effect at power-on, the voltage on any pin at any time must not be higher or lower than V_{DD} + 0,5 V or V_{SS} − 0,5 V respectively.

FUNCTIONAL DESCRIPTION

General

The PCB83C652 is a stand-alone high-performance microcontroller designed for use in real-time applications such as instrumentation and industrial control.

The device provides, in addition to the 80C51 standard functions, a serial I^2C-bus interface. As well as the parallel bus, functions may also be expanded using the I^2C-bus utilizing the complete line of the I^2C clips family.

The PCB83C652 is a control-oriented CPU with on-chip program and data memory. It can be extended with external program memory up to 64 K bytes. It can also access up to 64 K bytes of external data memory. For systems requiring extra capability, the PCB83C652 can be expanded using standard memories and peripherals.

The PCB83C652 has two software selectable modes of reduced activity for further power reduction – Idle and Power-down. The Idle mode freezes the CPU while allowing the RAM, timers, serial ports and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

Memory organization

The central processing unit (CPU) manipulates operands in three memory spaces; these are the 64 K-byte external data memory, 256-byte internal data memory and the 64 K-byte internal and external program memory. The internal data memory address space is sub-divided into the 256-byte internal data RAM and 128-byte Special Function Register (SFR) address spaces, as shown in Fig. 4. Figure 5 shows the Special Function Registers memory map. Internal RAM locations 0-127 are directly and indirectly addressable. Internal RAM locations 128-255 are only indirectly addressable. The special function register locations 128-255 are only directly addressable.

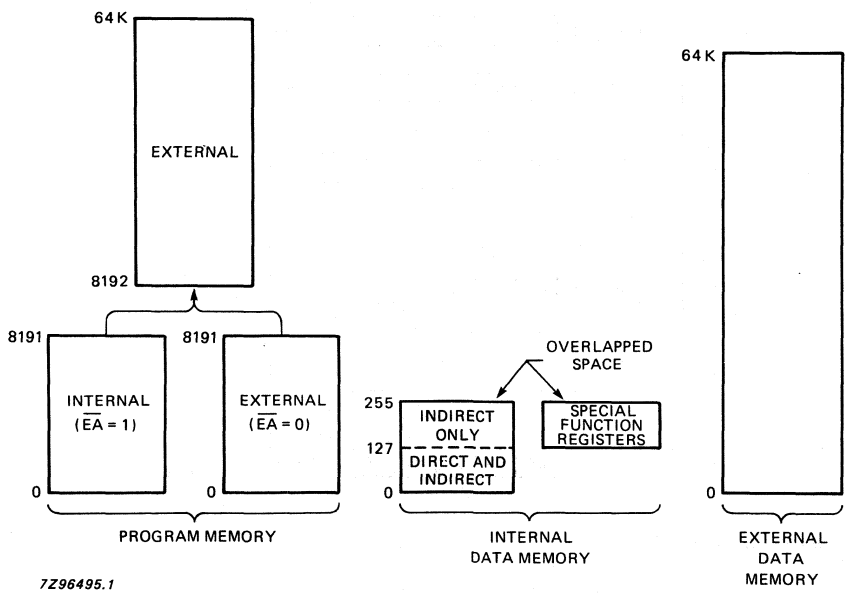
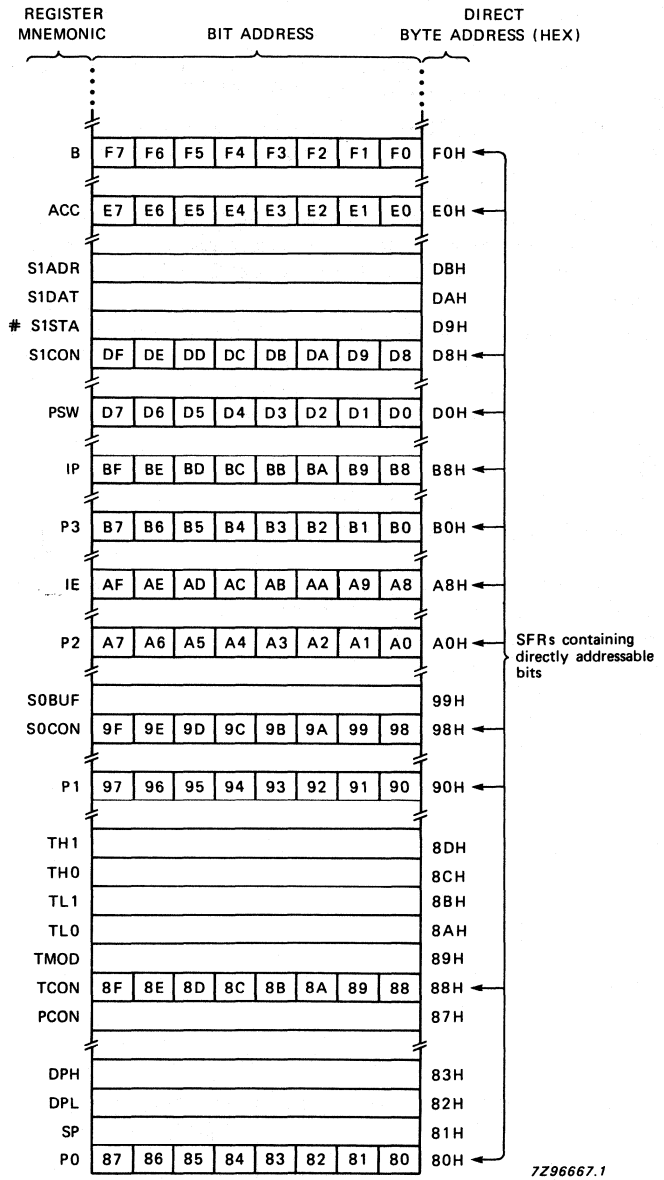


Fig. 4 Memory map.



S1STA is a read-only register.

Fig. 5 Special function registers memory map.

FUNCTIONAL DESCRIPTION (continued)

The internal data RAM contains four register banks (each with eight registers), 128 addressable bits, a scratchpad area and the stack. The stack depth is limited by the available internal data RAM and its location is determined by the 8-bit stack pointer. All registers except the program counter and the four 8-register banks reside in the special function register address space. These memory mapped registers include arithmetic registers, pointers, I/O ports, interrupt system registers, timers and serial port registers. There are 128 addressable bit locations in the SFR address space.

The PCB83C652 contains 256 bytes of internal data RAM and 25 special function registers. It provides a non-paged program memory address space to accommodate relocatable code. Conditional branches are performed relative to the program counter. The register-indirect jump permits branching relative to a 16-bit base register with an offset provided by an 8-bit index register. 16-bit jumps and calls permit branching to any location in the contiguous 64 K program memory address space.

Addressing

The PCB83C652 has five methods for addressing source operands:

- Register
- Direct
- Register-Indirect
- Immediate
- Base-Register plus Index-Register-Indirect

The first three methods can be used for addressing destination operands. Most instructions have a "destination/source" field that specifies the data type, addressing methods and operands involved. For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four 8-register banks through Register, Direct, or Register-Indirect.
- 256 bytes of internal data RAM through Direct or Register-Indirect. Bytes 0-127 may be addressed directly/indirectly. Bytes 128-255 share their address locations with the SFR registers and so may only be addressed indirectly as data RAM.
- Special function registers through Direct at address locations 128-255.
- External data memory through Register-Indirect.
- Program memory look-up tables through Base-Register plus Index-Register-Indirect.

The PCB83C652 is classified as an 8-bit device since the internal ROM, RAM, Special Function Registers (SFR), Arithmetic Logic Unit (ALU) and external data bus are each 8-bits wide. It performs operations on bit, nibble, byte and double-byte data types.

Facilities are available for byte transfer, logic and integer arithmetic operations. Data transfer, logic and conditional branch operations can be performed directly on Boolean variables to provide excellent bit handling.

Instruction set

The PCB83C652 uses the powerful instruction set of the PCB80C51. Additional special function registers are incorporated to control the on-chip peripherals. The instruction set consists of 49 single-byte, 45 two-byte and 17 three-byte instructions. When using a 12 MHz oscillator, 64 instructions execute in 1 μs and 45 instructions execute in 2 μs. Multiply and divide instructions execute in 4 μs.

FUNCTIONAL DESCRIPTION (continued)

I/O facilities

The PCB83C652 has four 8-bit ports. Ports 0-3 are the same as in the 80C51, with the exception of the additional functions of Port 1. Port lines P1.7 and P1.6 may be selected as the SDA and SCL lines of serial port SIO1 (I^2C). Because the I^2C-bus may be active while the device is disconnected from V_{DD}, these pins are provided with open drain drivers.

N.B. Therefore pins P1.7 and P1.6 do not have pull-up devices when used as ports.

Ports 0, 1, 2 and 3 perform the following alternative functions:

- Port 0: provides the multiplexed low-order address and data bus used for expanding the PCB83C652 with standard memories and peripherals.
- Port 1: Port 1 is partly used for the I^2C-bus functions;
  - SCL and SDA for the I^2C interface, P1.6 and P1.7 respectively.

Bits whose alternate function is not used may be used as normal bidirectional I/O pins.

- Port 2: provides the high-order address bus when expanding the PCB83C652 with external program memory and/or external data memory.
- Port 3: pins can be configured individually to provide:
  - external interrupt request inputs
  - counter inputs
  - serial port receiver input and transmitter output
  - control signals to READ and WRITE external data memory

The generation or use of a Port 3 pin as an alternative function is carried out automatically by the PCB83C652 provided the associated Special Function Register bit is set high.

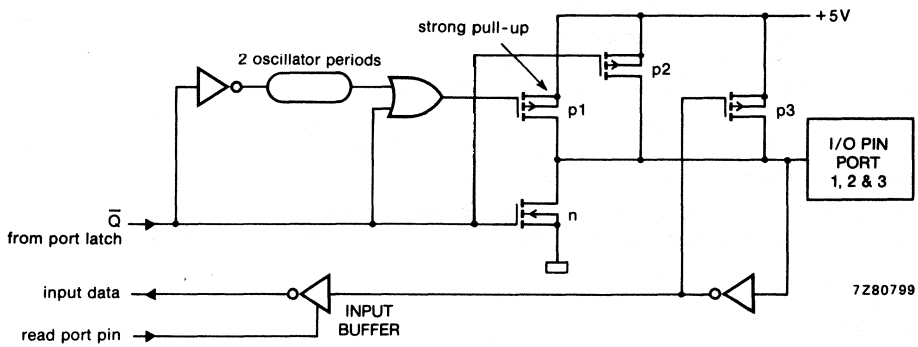


Fig. 6 I/O buffers in the PCB83C652 (Ports 2, 3, and P1.0 to P1.5).

Timer/event counters

The PCB83C652 contains two 16-bit timer/event counters: Timer 0 and Timer 1. Timer 0 and Timer 1 may be programmed to carry out the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests.

Timer 0 and Timer 1 can be programmed independently to operate in three modes:

- Mode 0: 8-bit timer or 8-bit counter each with divide-by-32 prescaler
- Mode 1: 16-bit time-interval or event counter
- Mode 2: 8-bit time-interval or event counter with automatic reload upon overflow.

Timer 0 can be programmed to operate in an additional mode as follows:

- Mode 3: one 8-bit time-interval or event counter and one 8-bit time-interval counter.

When Timer 0 is in Mode 3, Timer 1 can be programmed to operate in Modes 0, 1 or 2 but cannot set an interrupt request flag or generate an interrupt. However the overflow from Timer 1 can be used to pulse the serial port transmission-rate generator.

The frequency handling range of these counters with a 12 MHz crystal is as follows:

- In the timer function, the timer is incremented at a frequency of 1 MHz — a division by 12 of the oscillator frequency
- 0 Hz to an upper limit of 0,5 MHz when programmed for external inputs.

Both internal and external inputs can be gated to the counter by a second external source for directly measuring pulse durations.

The counters are started and stopped under software control. Each one sets its interrupt request flag when it overflows from all logic 1s to all logic 0s (or automatic reload value), with the exception of mode 3 as previously described.

Serial I/O (see Fig. 7)

The PCB83C652 is equipped with two independent serial ports. SIO0 is the full duplex UART port and is identical to the serial port of the PCB80C51.

Serial port SIO1 supports the I^2C-bus, the function of which is controlled by the S1CON register. S1STA is the status register whose contents may also be used as a vector to various service routines. S1DAT is the data shift register and S1ADR the slave address register. The least significant bit of S1ADR enables/disables general call address recognition.

FUNCTIONAL DESCRIPTION (continued)

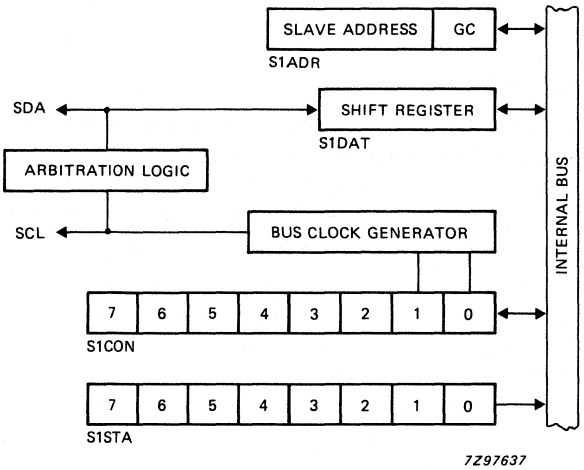


Fig. 7 Block diagram of I^2C serial I/O.

The I^2C serial I/O has complete autonomy in byte handling and operates in 4 modes:

1. Master transmitter
2. Master receiver
3. Slave transmitter
4. Slave receiver

Slave address recognition is performed by on-chip hardware.

The I^2C-bus consists of two lines: a data line (SDA) and a clock line (SCL). These lines also function as the I/O port lines on P1.7 and P1.6. The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware.

Serial control register S1CON

	7	6	5	4	3	2	1	0
S1CON(D8H)	X	ENS1	STA	STO	SI	AA	CR1	CR0

Bits CR1 and CR0 determine the clock frequency that is generated in the master mode of operation. Table 1 displays the clock rate when using a 12 MHz crystal.

Table 1 Clock rate when using a 12 MHz crystal

CR1 / CR0	bit frequency	f_{osc} divided by
0 0	12,5 kHz	960
0 1	100 kHz	120
1 0	200 kHz	60 ($f_{osc} < 6$ MHz meeting I^2C)
1 1	62,5–0,5 kHz	96 x (256–reload value Timer 1) (reload value range: 0-254 in mode 2)

AA

Assert acknowledge bit. When this bit is set, an acknowledge is returned after any one of the following conditions:

- Own slave address is received
- General call address is received (S1ADR.0 = logic 1)
- A data byte is received, while the device is programmed to be a master receiver
- A data byte is received, while the device is a selected slave receiver.

When this bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own address or general call address is received.

SI

SIO1 interrupt flag. This flag is set, and an interrupt request is generated, after any of the following events occur:

- A START condition is generated in MST mode
- The own slave address has been received during AA = logic 1
- The general call address has been received while S1ADR.0 and AA = logic 1
- A data byte has been received or transmitted in MST mode (even if arbitration is lost)
- A data byte has been received or transmitted as selected slave
- A STOP or START condition is received as selected slave receiver or transmitter.

STO

STOP flag. When in master mode,and this bit is set a STOP condition is generated. A STOP condition detected on the I^2C-bus clears this bit. This bit may also be set in slave mode in order to recover from an error condition. Then no STOP condition is generated to the I^2C-bus, but the hardware releases the SDA and SCL lines and switches to the not selected slave receiver mode. The STOP flag is cleared by the hardware.

STA

START flag. When this bit is set, the hardware checks the I^2C-bus and generates a START condition if the bus is free. If the device is already programmed as either master/transmitter or master/receiver, it will generate a repeated START condition.

ENS1

0 = Serial I/O Disabled and reset. Output ports P1.6 and P1.7 function with open drain

1 = Serial I/O Enabled. Output ports P1.6 and P1.7 must be set to logic 1.

FUNCTIONAL DESCRIPTION (continued)

Serial status register S1STA (S1STA is a read-only register)

	7	6	5	4	3	2	1	0
S1STA(D9H)	SC4	SC3	SC2	SC1	SC0	0	0	0

S1STA.3 - S1STA.7 hold a status code. S1STA.0 - S1STA.2 are held LOW. The contents of the status register may be used as a vector to a service routine. This optimizes the response time of the software and consequently that of the I^2C-bus.

Abbreviations used:

SLA : 7-bit slave address
R : Read bit
W : Write bit
ACK : Acknowledgement (acknowledge bit = logic 0)
$\overline{\text{ACK}}$: Not acknowledgement (acknowledge bit = logic 1)
DATA : 8-bit data byte to or from I^2C-bus
MST : Master
SLV : Slave
TRX : Transmitter
REC : Receiver

The following is a list of the status codes:

MST/TRX mode

S1STA value

08H - A START condition has been transmitted
10H - A repeated START condition has been transmitted
18H - SLA and W have been transmitted, ACK has been received
20H - SLA and W have been transmitted, $\overline{\text{ACK}}$ received
28H - DATA of S1DAT has been transmitted, ACK received
30H - DATA of S1DAT has been transmitted, $\overline{\text{ACK}}$ received
38H - Arbitration lost in SLA, R/W or DATA

MST/REC mode

S1STA value

38H - Arbitration lost while returning $\overline{\text{ACK}}$
40H - SLA and R have been transmitted, ACK received
48H - SLA and R have been transmitted, $\overline{\text{ACK}}$ received
50H - DATA has been received, ACK returned
58H - DATA has been received, $\overline{\text{ACK}}$ returned

SLV/REC mode

S1STA value

- 60H - Own SLA and W have been received, ACK returned
- 68H - Arbitration lost in SLA, R/W as MST. Own SLA and W have been received, ACK returned
- 70H - General CALL has been received, ACK returned
- 78H - Arbitration lost in SLA, R/W as MST. General call has been received
- 80H - Previously addressed with own SLA. DATA byte received, $\overline{\text{ACK}}$ returned
- 88H - Previously addressed with own SLA. DATA byte received, $\overline{\text{ACK}}$ returned
- 90H - Previously addressed with general call. DATA byte has been received, ACK has been returned
- 98H - Previously addressed with general call. DATA byte has been received, $\overline{\text{ACK}}$ has been returned
- A0H - A STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX.

SLV/TRX mode

S1STA value

- A8H - Own SLA and R have been received, ACK returned
- B0H - Arbitration lost in SLA, R/W as MST. Own SLA and R have been received, ACK returned
- B8H - DATA byte has been transmitted, $\overline{\text{ACK}}$ received
- C0H - DATA byte has been transmitted, $\overline{\text{ACK}}$ received
- C8H - Last DATA byte has been transmitted (AA = logic 0), ACK received.

Miscellaneous

S1STA value

- 00H - Bus error during MST mode or selected SLV mode, due to an erroneous START or STOP condition

The data shift register S1DAT

S1DAT(DAH)	7	6	5	4	3	2	1	0

This register contains the serial data to be transmitted or data which has just been received. Bit 7 is transmitted or received first; i.e. data is shifted from right to left.

Address register S1ADR

S1ADR (DBH)	7	6	5	4	3	2	1	0

S1ADR.0, GC : 0 = general call address is not recognized
1 = general call address is recognized

S1ADR.7-1 : own slave address

This 8-bit register may be loaded with the 7-bit slave address to which the controller will respond when programmed as a slave receiver/transmitter. The LSB (GC) is used to determine whether the general call address is recognized.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Idle and Power-down operation (see Fig. 8)

Idle mode operation permits the interrupt, serial ports and timer blocks to continue to function while the CPU is halted.

The following functions remain active during Idle mode. These functions may generate an interrupt or reset and thus end the Idle mode:

Timer 0, Timer 1
SIO0, SIO1
External interrupt

The Power-down operation freezes the oscillator. The Power-down mode can only be activated by setting the PD bit in the PCON register.

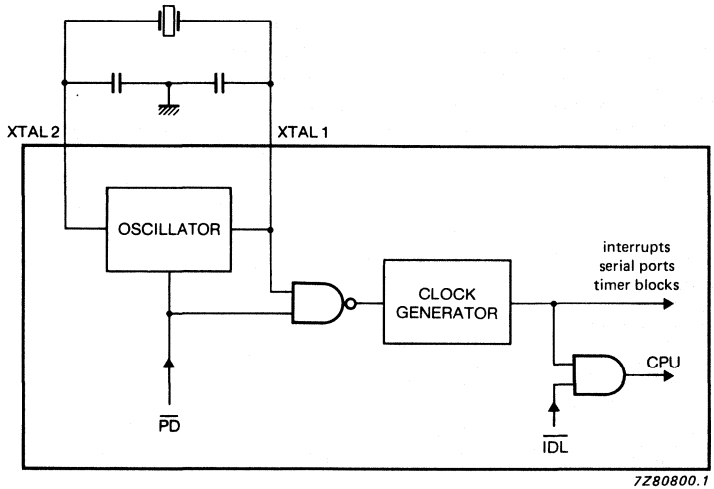


Fig. 8 Internal Idle and Power-down clock configuration.

Power control register

These special modes are activated by software via the Special Function Register PCON. Its hardware address is 87H. PCON is not bit addressable.

	7	6	5	4	3	2	1	0
PCON(87H)	SMOD	–	–	–	GF1	GF0	PD	IDL

Bit	Symbol	Function
PCON.7	SMOD	Double Baud rate bit. When set to logic 1 the baud rate is doubled when the serial port SIO0 is being used in modes 1, 2 or 3
PCON.6	–	(reserved)
PCON.5	–	(reserved)
PCON.4	–	(reserved)
PCON.3	GF1	General-purpose flag bit
PCON.2	GF0	General-purpose flag bit
PCON.1	PD	Power-down bit. Setting this bit activates Power-down mode
PCON.0	IDL	Idle mode bit. Setting this bit activates the Idle mode.

If logic 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is 0XXX0000.

Idle mode

The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before Idle mode is activated. Once in the Idle mode, the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 2.

There are two ways to terminate the Idle mode:

Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware terminating Idle mode. The interrupt is serviced, and following return from interrupt instruction RETI, the next instruction to be executed will be the one which follows the instruction that wrote a logic 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an interrupt, the service routine can examine the status of the flags bits.

The second way of terminating the Idle mode is with an external hardware reset. Since the oscillator is still running, the hardware reset is required to be active for two machine cycles (24 oscillator periods) to complete the reset operation.

Power-down mode

The instruction that sets PCON.1 is the last executed prior to going into the Power-down mode. Once in Power-down mode, the oscillator is stopped. Only the contents of the on-chip RAM are preserved. The Special Function Registers are not saved. A hardware reset is the only way of exiting the Power-down mode.

In the Power-down mode, V_{DD} may be reduced to minimize circuit power consumption. The voltage must not be reduced until the Power-down mode is entered, but must be restored before the hardware reset is applied which will free the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

The status of the external pins during Power-down mode is shown in Table 2. If the Power-down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull-up transistor p1 (see Fig. 6).

FUNCTIONAL DESCRIPTION (continued)

Table 2 Status of the external pins during Idle and Power-down modes.

mode	memory	ALE	$\overline{PSEN}$	Port 0	Port 1	Port 2	Port 3
Idle	internal	1	1	port data	port data	port data	port data
Idle	external	1	1	floating	port data	address	port data
Power-down	internal	0	0	port data	port data	port data	port data
Power-down	external	0	0	floating	port data	port data	port data

Note: Ports 1.7 and 1.6 if selected, function as SDA and SCL respectively in the Idle mode.

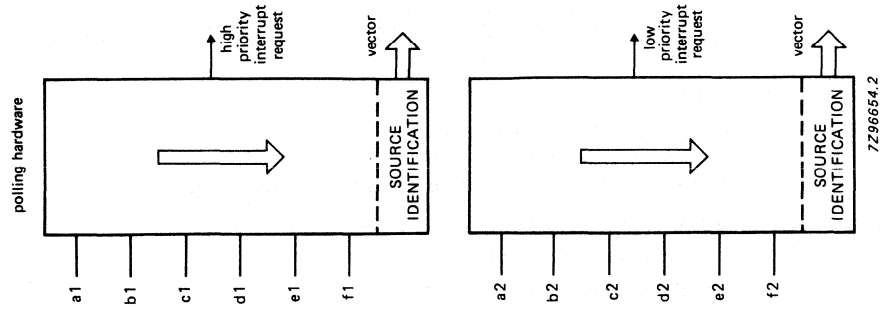
Interrupt system (see Fig. 9)

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. Interrupt response latency is from 3 μs to 8 μs when using a 12 MHz crystal. The PCB83C652 acknowledges interrupt requests from six sources as follows:

- $\overline{INT0}$ and $\overline{INT1}$: two external interrupts
- Timer 0 and Timer 1: two internal counters
- I^2C serial I/O interrupt
- UART serial I/O port interrupt

Each interrupt vectors to a separate location in program memory for its service program. Each source can be individually enabled or disabled by a corresponding bit in the IE register, moreover each interrupt may be programmed to a high or low priority level using a corresponding bit in the IP register. Also all enabled sources can be globally disabled or enabled. Both external interrupts can be programmed to be level-activated or transition-activated; an active LOW level allows "wire-ORing" of several interrupt sources to the input pin.

DEVELOPMENT DATA



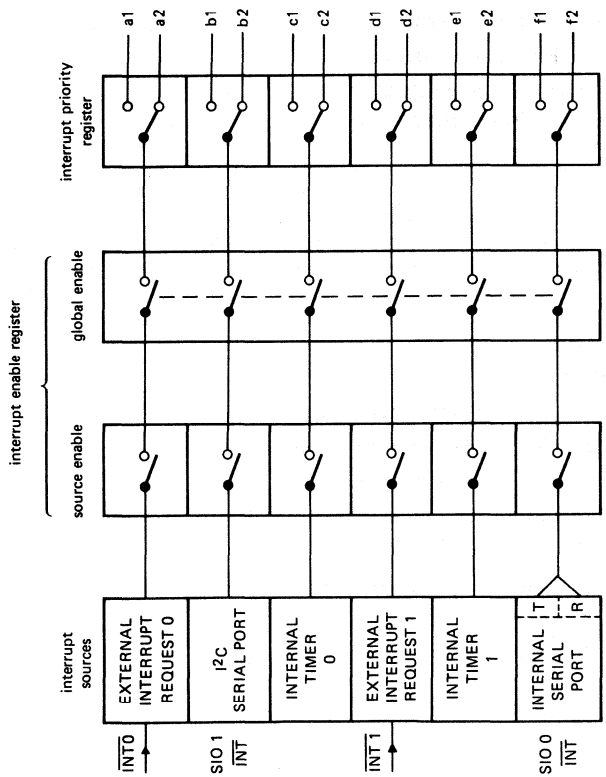


Fig. 9 Interrupt system.

FUNCTIONAL DESCRIPTION (continued)

Interrupt enable register

	7	6	5	4	3	2	1	0
IE(A8H)	EA	–	ES1	ES0	ET1	EX1	ET0	EX0

Bit	Symbol	Function
IE.7	EA	General enable/disable control 0 = No interrupt is enabled 1 = Any individually enabled interrupt will be accepted
IE.6	–	Unused
IE.5	ES1	Enable SIO1 (I^2C) interrupt
IE.4	ES0	Enable SIO0 (UART) interrupt
IE.3	ET1	Enable Timer 1 interrupt
IE.2	EX1	Enable External 1 interrupt
IE.1	ET0	Enable Timer 0 interrupt
IE.0	EX0	Enable External 0 interrupt
		where 0 = interrupt disabled and 1 = interrupt enabled

Interrupt priority register

	7	6	5	4	3	2	1	0
IP(B8H)	–	–	PS1	PS0	PT1	PX1	PT0	PX0

Bit	Symbol	Function
IP.7	–	Unused
IP.6	–	Unused
IP.5	PS1	SIO1 (I^2C) interrupt priority level
IP.4	PS0	SIO0 (UART) interrupt priority level
IP.3	PT1	Timer 1 interrupt priority level
IP.2	PX1	External interrupt 1 priority level
IP.1	PT0	Timer 0 interrupt priority level
IP.0	PX0	External interrupt 0 priority level

Interrupt priority levels are as follows: 0 = low priority
1 = high priority

Table 3 shows the interrupt vectors. The vector indicates the ROM location where the appropriate interrupt service routine starts.

Table 3 Interrupt vectors

source		vector
External 0	X0	0003H
Timer 0 overflow	T0	000BH
External 1	X1	0013H
Timer 1 overflow	T1	001BH
Serial I/O 0 (UART)	S0	0023H
Serial I/O 1 (I^2C)	S1	002BH

Interrupt priority

Each interrupt source can be either high priority or low priority. If both priorities are requested simultaneously, the processor will branch to the high priority vector. If there are simultaneous requests from sources of the same priority, then interrupts will be serviced in the following order:

X0, S1, T0, X1, T1, S0

A low priority interrupt routine can only be interrupted by a high priority interrupt. A high priority interrupt routine can not be interrupted.

Oscillator circuitry

The oscillator circuitry of the PCB83C652 is a single-stage inverting amplifier in a Pierce oscillator configuration. The circuitry between XTAL 1 and XTAL 2 is basically an inverter biased to the transfer point. Either a crystal or ceramic resonator can be used as the feedback element to complete the oscillator circuitry. Both are operated in parallel resonance. XTAL 1 is the high gain amplifier input, and XTAL 2 is the output (see Fig. 10). To drive the PCB83C652 externally, XTAL 1 is driven from an external source and XTAL 2 left open-circuit (see Fig. 11).

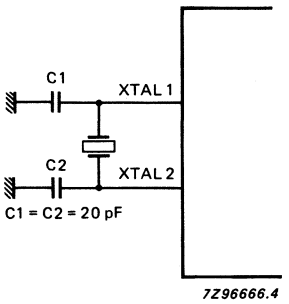


Fig. 10 PCB83C652 oscillator circuit.

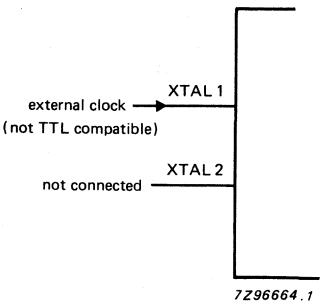


Fig. 11 Driving the PCB83C652 from an external source.

FUNCTIONAL DESCRIPTION (continued)

Reset circuitry (see Fig. 12)

The reset circuitry for the PCB83C652 is connected to the reset pin RST. A Schmitt trigger is used at the input for noise rejection. The output of the Schmitt trigger is sampled by the reset circuitry every machine cycle.

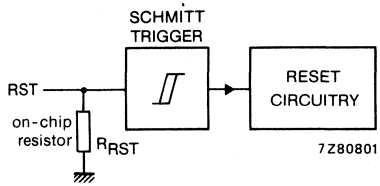


Fig. 12 On-chip reset configuration.

A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods). The CPU responds by executing an internal reset. During reset ALE and $\overline{PSEN}$ output a HIGH level. In order to perform a correct reset, this level must not be affected by external elements.

The internal reset is executed during the second cycle in which RST is HIGH and is repeated every cycle until RST goes LOW. It leaves the internal registers as follows:

Register	Content
ACC	0000 0000
B	0000 0000
DPL	0000 0000
DPH	0000 0000
IE	0x00 0000
IP	xx00 0000
PCH	0000 0000
PCL	0000 0000
PCON	0xxx 0000
PSW	0000 0000
P0 to P3	1111 1111
S0BUF	xxxx xxxx
S0CON	0000 0000
S1ADR	0000 0000
S1CON	x000 0000
S1DAT	0000 0000
S1STA	1111 1000
SP	0000 0111
TCON	0000 0000
TH0, TH1	0000 0000
TL0, TL1	0000 0000
TMOD	0000 0000

The internal RAM is not affected by reset. When V_{DD} is turned on, the RAM content is indeterminate.

Power-on reset (see Fig. 13)

When V_{DD} is turned on an automatic reset can be obtained by connecting the RST pin to V_{DD} via a 2,2 μF capacitor. When the power is switched on, the voltage on the RST pin is equal to V_{DD} minus the capacitor voltage, and decreases from V_{DD} as the capacitor charges through the internal resistor (R_{RST}) to ground. The larger the capacitor, the more slowly V_{RST} decreases. V_{RST} must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles.

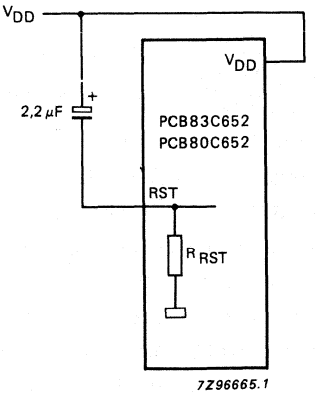


Fig. 13 Power-on reset.

INSTRUCTION SET

Table 4 Instruction set description

mnemonic		description	bytes/ cycles		opcode (hex.)
Arithmetic operations					
ADD	A,Rr	Add register to A	1	1	2*
ADD	A,direct	Add direct byte to A	2	1	25
ADD	A,@Ri	Add indirect RAM to A	1	1	26, 27
ADD	A,#data	Add immediate data to A	2	1	24
ADDC	A,Rr	Add register to A with carry flag	1	1	3*
ADDC	A,direct	Add direct byte to A with carry flag	2	1	35
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A,#data	Add immediate data to A with carry flag	2	1	34
SUBB	A,Rr	Subtract register from A with borrow	1	1	9*
SUBB	A,direct	Subtract direct byte from A with borrow	2	1	95
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A,#data	Subtract immediate data from A with borrow	2	1	94
INC	A	Increment A	1	1	04
INC	Rr	Increment register	1	1	0*
INC	direct	Increment direct byte	2	1	05
INC	@Ri	Increment indirect RAM	1	1	06, 07
DEC	A	Decrement A	1	1	14
DEC	Rr	Decrement register	1	1	1*
DEC	direct	Decrement direct byte	2	1	15
DEC	@Ri	Decrement indirect RAM	1	1	16, 17
INC	DPTR	Increment data pointer	1	2	A3
MUL	AB	Multiply A & B	1	4	A4
DIV	AB	Divide A by B	1	4	84
DA	A	Decimal adjust A	1	1	D4

mnemonic		description	bytes/ cycles		opcode (hex.)
Logic operations					
ANL	A,Rr	AND register to A	1	1	5*
ANL	A,direct	AND direct byte to A	2	1	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	1	54
ANL	direct,A	AND A to direct byte	2	1	52
ANL	direct,#data	AND immediate data to direct byte	3	2	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	1	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	1	44
ORL	direct,A	OR A to direct byte	2	1	42
ORL	direct,#data	OR immediate data to direct byte	3	2	43
XRL	A,Rr	Exclusive-OR register to A	1	1	6*
XRL	A,direct	Exclusive-OR direct byte to A	2	1	65
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	Exclusive-OR immediate data to A	2	1	64
XRL	direct,A	Exclusive-OR A to direct byte	2	1	62
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2	63
CLR	A	Clear A	1	1	E4
CPL	A	Complement A	1	1	F4
RL	A	Rotate A left	1	1	23
RLC	A	Rotate A left through the carry flag	1	1	33
RR	A	Rotate A right	1	1	03
RRC	A	Rotate A right through the carry flag	1	1	13
SWAP	A	Swap nibbles within A	1	1	C4

INSTRUCTION SET (continued)

Table 4 (continued)

mnemonic	description	bytes/ cycles		opcode (hex.)
Data transfer				
MOV A,Rr	Move register to A	1	1	E*
MOV A,direct **	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect RAM to A	1	1	E6, E7
MOV A,#data	Move immediate data to A	2	1	74
MOV Rr,A	Move A to register	1	1	F*
MOV Rr,direct	Move direct byte to register	2	2	A*
MOV Rr,#data	Move immediate data to register	2	1	7*
MOV direct,A	Move A to direct byte	2	1	F5
MOV direct,Rr	Move register to direct byte	2	2	8*
MOV direct,direct	Move direct byte to direct byte	3	2	85
MOV direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV direct,#data	Move immediate data to direct byte	3	2	75
MOV @Ri,A	Move A to indirect RAM	1	1	F6, F7
MOV @Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV @Ri,#data	Move immediate data to indirect RAM	2	1	76, 77
MOV DPTR,#data 16	Load data pointer with a 16-bit constant	3	2	90
MOVC A,@A+DPTR	Move code byte relative to DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative to PC to A	1	2	83
MOVX A,@Ri	Move external RAM (8-bit address) to A	1	2	E2, E3
MOVX A,@DPTR	Move external RAM (16-bit address) to A	1	2	E0
MOVX @Ri,A	Move A to external RAM (8-bit address)	1	2	F2, F3
MOVX @DPTR,A	Move A to external RAM (16-bit address)	1	2	F0
PUSH direct	Push direct byte onto stack	2	2	C0
POP direct	Pop direct byte from stack	2	2	D0
XCH A,Rr	Exchange register with A	1	1	C*
XCH A,direct	Exchange direct byte with A	2	1	C5
XCH A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD A,@Ri	Exchange LOW-order nibble indirect RAM with A	1	1	D6, D7

** MOV A,ACC is not a valid instruction.

mnemonic		description	bytes/ cycles		opcode (hex.)
Boolean variable manipulation					
CLR	C	Clear carry flag	1	1	C3
CLR	bit	Clear direct bit	2	1	C2
SETB	C	Set carry flag	1	1	D3
SETB	bit	Set direct bit	2	1	D2
CPL	C	Complement carry flag	1	1	B3
CPL	bit	Complement direct bit	2	1	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C,bit	OR direct bit to carry flag	2	2	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C,bit	Move direct bit to carry flag	2	1	A2
MOV	bit,C	Move carry flag to direct bit	2	2	92
Program and machine control					
ACALL	addr11	Absolute subroutine call	2	2	●1addr
LCALL	addr16	Long subroutine call	3	2	12
RET		Return from subroutine	1	2	22
RETI		Return from interrupt	1	2	32
AJMP	addr11	Absolute jump	2	2	▲1addr
LJMP	addr16	Long jump	3	2	02
SJMP	rel	Short jump (relative address)	2	2	80
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2	73
JZ	rel	Jump if A is zero	2	2	60
JNZ	rel	Jump if A is not zero	2	2	70
JC	rel	Jump if carry flag is set	2	2	40
JNC	rel	Jump if carry flag is not set	2	2	50
JB	bit,rel	Jump if direct bit is set	3	2	20
JNB	bit,rel	Jump if direct bit is not set	3	2	30
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2	10
CJNE	A,direct,rel	Compare direct to A and jump if not equal	3	2	B5
CJNE	A,#data,rel	Compare immediate to A and jump if not equal	3	2	B4
CJNE	Rr,#data,rel	Compare immed. to reg. and jump if not equal	3	2	B*
CJNE	@Ri,#data,rel	Compare immed. to ind. and jump if not equal	3	2	B6, B7
DJNZ	Rr,rel	Decrement register and jump if not zero	2	2	D*
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2	D5
NOP		No operation	1	1	00

Notes to Table 4

Data addressing modes

Rr	Working register R0-R7.
direct	128 internal RAM locations and any special function register (SFR).
@Ri	Indirect internal RAM location addressed by register R0 or R1 of the actual register bank.
#data	8-bit constant included in instruction.
#data16	16-bit constant included as bytes 2 and 3 of instruction.
bit	direct addressed bit in internal RAM or SFR.
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 K-byte program memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 K-byte page of program memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is −128 to + 127 bytes relative to first byte of the following instruction.

Hexadecimal opcode cross-reference to Table 4

* : 8, 9, A, B, C, D, E, F.
● : 11, 31, 51, 71, 91, B1, D1, F1.
▲ : 01, 21, 41, 61, 81, A1, C1, E1.

Table 5 Instruction map

first hexadecimal chacter of opcode ↓ — second hexadecimal character of opcode →

	0	1	2	3	4	5	6 | 7	8 | 9 | A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC dir	INC @Ri 0 | 1	INC Rr 0 | 1 | 2	3	4	5	6	7
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC dir	DEC @Ri 0 | 1	DEC Rr 0 | 1 | 2	3	4	5	6	7
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,dir	ADD A,@Ri 0 | 1	ADD A,Rr 0 | 1 | 2	3	4	5	6	7
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,dir	ADDC A,@Ri 0 | 1	ADDC A,Rr 0 | 1 | 2	3	4	5	6	7
4	JC rel	AJMP addr11	ORL dir,A	ORL dir,#data	ORL A,#data	ORL A,dir	ORL A,@Ri 0 | 1	ORL A,Rr 0 | 1 | 2	3	4	5	6	7
5	JNC rel	ACALL addr11	ANL dir,A	ANL dir,#data	ANL A,#data	ANL A,dir	ANL A,@Ri 0 | 1	ANL A,Rr 0 | 1 | 2	3	4	5	6	7
6	JZ rel	AJMP addr11	XRL dir,A	XRL dir,#data	XRL A,#data	XRL A,dir	XRL A,@Ri 0 | 1	XRL A,Rr 0 | 1 | 2	3	4	5	6	7
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV dir,#data	MOV @Ri,#data 0 | 1	MOV Rr,#data 0 | 1 | 2	3	4	5	6	7
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV dir,dir	MOV dir,@Ri 0 | 1	MOV dir,Rr 0 | 1 | 2	3	4	5	6	7
9	MOV DPTR, #data	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,dir	SUBB A,@Ri 0 | 1	SUBB A,Rr 0 | 1 | 2	3	4	5	6	7
A	ORL C,/bit	AJMP addr11	MOV C,bit	INC DPTR	MUL AB		MOV @Ri,dir 0 | 1	MOV Rr,dir 0 | 1 | 2	3	4	5	6	7
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A, #data,rel	CJNE A,dir,rel	CJNE @Ri,#data,rel 0 | 1	CJNE Rr,#data,rel 0 | 1 | 2	3	4	5	6	7
C	PUSH dir	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,dir	XCH A,@Ri 0 | 1	XCH A,Rr 0 | 1 | 2	3	4	5	6	7
D	POP dir	ACALL addr11	SETB bit	SETB C	DA A	DJNZ dir,rel	XCHD A,@Ri 0 | 1	DJNZ Rr,rel 0 | 1 | 2	3	4	5	6	7
E	MOVX A,@DPTR	AJMP addr11	MOVX A,@Ri 0 | 1		CLR A	MOV * A,dir	MOV A,@Ri 0 | 1	MOV A,Rr 0 | 1 | 2	3	4	5	6	7
F	MOVX @DPTR,A	ACALL addr11	MOVX @Ri,A 0 | 1		CPL A	MOV dir,A	MOV @Ri,A 0 | 1	MOV Rr,A 0 | 1 | 2	3	4	5	6	7

* MOV A,ACC is not a valid instruction.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Input voltage on any pin with respect to ground (V_{SS})	V_I	−0,5	+ 6,5	V
Input, output current on any single pin	I_I, I_O	−	± 5	mA
Input, output current on any two pins	I_I, I_O	−	± 10	mA
Total power dissipation	P_{tot}	−	1	W
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range				
PCB83C652 versions	T_{amb}	0	+ 70	°C
PCF83C652 versions	T_{amb}	−40	+ 85	°C
PCA83C652 versions	T_{amb}	−40	+ 125	°C

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 5 V (± 10%); V_{SS} = 0 V; T_{amb} = 0 to 70 °C (PCB83C652); −40 to 85 °C (PCF83C652); −40 to 125 °C (PCA83C652). All voltages with respect to V_{SS} unless otherwise specified.

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_{DD}	4.5	5.5	V
Supply current					
operating	(notes 1 and 2)	I_{DD}	–	24	mA
	(notes 1 and 3)	I_{DD}	–	27	mA
idle mode	(notes 2 and 4)	I_{ID}	–	5.0	mA
	(notes 3 and 4)	I_{ID}	–	6.0	mA
Power-down current	(notes 2, 5 and 6)	I_{PD}	–	50	μA
	(notes 3, 5 and 6)	I_{PD}	–	120	μA
Inputs					
LOW level input voltage (except $\overline{EA}$, P1.6/SCL, P1.7/SDA)		V_{IL}	−0.5	$0.2V_{DD}-0.1$	V
LOW level input voltage ($\overline{EA}$)		V_{IL1}	−0.5	$0.2V_{DD}-0.3$	V
LOW level input voltage (P1.6/SCL, P1.7/SDA)*		V_{IL2}	−0.5	1.5	V
HIGH level input voltage (except RST, XTAL 1, P1.6/SCL, P1.7/SDA)		V_{IH}	$0.2V_{DD}+0.9$	$V_{DD}+0.5$	V
HIGH level input voltage (RST and XTAL 1)		V_{IH1}	$0.7V_{DD}$	$V_{DD}+0.5$	V
HIGH level input voltage (P1.6/SCL, P1.7/SDA)*		V_{IH2}	3.0	6	V
Input current logic 0 (Ports 1, 2 and 3 except P1.6/SCL, P1.7/SDA)	V_I = 0.45 V	$-I_{IL}$	–	50	μA
Input current logic 1 to 0 transition (Ports 1, 2, 3 except P1.6/SCL, P1.7/SDA)	V_I = 2.0 V	$-I_{TL}$	–	650	μA
Input leakage current (Port 0, $\overline{EA}$)	$0.45\ V < V_I < V_{DD}$	$\pm I_{LI1}$	–	10	μA
Input leakage current (P1.6/SCL, P1.7/SDA)	$0\ V < V_I < 6\ V$; $0\ V < V_{DD} < 5.5\ V$	$\pm I_{LI2}$	–	10	μA

* The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I^2C specification, so an input voltage below 1.5 V will be recognized as a logic 0 while an input voltage above 3.0 V will be recognized as a logic 1.

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	max.	unit
Outputs					
LOW level output voltage (Ports 1, 2, 3 except P1.6/SCL, P1.7/SDA)*	I_{OL} = 1.6 mA	V_{OL}	–	0.45	V
LOW level output voltage (Port 0, ALE, $\overline{PSEN}$)*	I_{OL} = 3.2 mA	V_{OL1}	–	0.45	V
LOW level output voltage (P1.6/SCL, P1.7/SDA)	I_{OL} = 3.0 mA	V_{OL2}	–	0.40	V
HIGH level output voltage (Ports 1, 2, 3)	$-I_{OH}$ = 60 μA	V_{OH}	2.4	–	V
	$-I_{OH}$ = 25 μA	V_{OH}	$0.75V_{DD}$	–	V
	$-I_{OH}$ = 10 μA	V_{OH}	$0.9V_{DD}$	–	V
HIGH level output voltage (Port 0 in external bus mode, ALE, $\overline{PSEN}$)**	$-I_{OH}$ = 400 μA	V_{OH1}	2.4	–	V
	$-I_{OH}$ = 150 μA	V_{OH1}	$0.75V_{DD}$	–	V
	$-I_{OH}$ = 40 μA	V_{OH1}	$0.9V_{DD}$	–	V
RST pull-down resistor		R_{RST}	50	150	kΩ
I/O pin capacitance	test freq. = 1 MHz; T_{amb} = 25 °C	$C_{I/O}$	–	10	pF

Notes to the DC characteristics

1. The operating supply current is measured with all output pins disconnected; XTAL 1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$ + 0.5 V; $V_{IH} = V_{DD}$ −0.5 V; XTAL 2 not connected; $\overline{EA}$ = RST = Port 0 = P1.6 = P1.7 = V_{DD}; f_{CLK} = 12 MHz.
2. This is a preliminary value and applies to PCB83C652 (0 to 70 °C) and PCF83C652 (−40 to 85 °C).
3. This is a preliminary value and applies to PCA83C652 (−40 to 125 °C).
4. The idle mode supply current is measured with all output pins disconnected; XTAL 1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$ + 0.5 V; $V_{IH} = V_{DD}$ −0.5 V; XTAL 2 not connected; $\overline{EA}$ = Port 0 = P1.6 = P1.7 = V_{DD}; RST = V_{SS}; f_{CLK} = 12 MHz.
5. The power-down current is measured with all output pins disconnected; XTAL 2 not connected; $\overline{EA}$ = Port 0 = P1.6 = P1.7 = V_{DD}; RST = V_{SS}.
6. 2 V $\leqslant V_{PD} \leqslant V_{DD}$ max..

* Capacitive loading on Port 0 and Port 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1 and Port 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make a 1-to-0 transition during Bus operations. In the most adverse condition (capacitive loading > 100 pF) the noise pulse on ALE line may exceed 0.8 V. In this event it may be required to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger STROBE input.

** Capacitive loading on Port 0 and Port 2 may cause the HIGH level output voltage on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{DD} specification when the address bits are stabilizing.

AC CHARACTERISTICS

V_{DD} = 5 V (± 10%); V_{SS} = 0 V; T_{amb} = 0 to 70 °C (PCB83C652); −40 to 85 °C (PCF83C652); −40 to 125 °C (PCA83C652). C_L = 100 pF (Port 0, ALE and $\overline{PSEN}$); C_L = 80 pF (all other outputs); unless otherwise specified (see waveforms Figs 16, 17 and 18).

parameter	symbol	10 MHz		12 MHz		variable clock		unit
		min.	max.	min.	max.	min.	max.	
Program memory								
ALE pulse duration	t_{LL}	160	–	127	–	$2t_{CK}-40$	–	ns
Address set-up time to ALE	t_{AL}	45	–	28	–	$t_{CK}-55$	–	ns
Address hold time after ALE	t_{LA}	65	–	48	–	$t_{CK}-35$	–	ns
Time from ALE to valid instruction input	t_{LIV}	–	300	–	233	–	$4t_{CK}-100$	ns
Time from ALE to control pulse $\overline{PSEN}$	t_{LC}	60	–	43	–	$t_{CK}-40$	–	ns
Control pulse duration $\overline{PSEN}$	t_{CC}	255	–	205	–	$3t_{CK}-45$	–	ns
Time from $\overline{PSEN}$ to valid instruction input	t_{CIV}	–	195	–	145	–	$3t_{CK}-105$	ns
Input instruction hold time after $\overline{PSEN}$	t_{CI}	0	–	0	–	0	–	ns
Input instruction float delay after $\overline{PSEN}$	t_{CIF}	–	75	–	59	–	$t_{CK}-25$	ns
Address to valid instruction input	t_{AIV}	–	395	–	312	–	$5t_{CK}-105$	ns
Address float delay after $\overline{PSEN}$	t_{AFC}	–	10	–	10	–	10	ns

AC CHARACTERISTICS (continued)

parameter	symbol	10 MHz		12 MHz		variable clock		unit
		min.	max.	min.	max.	min.	max.	
External data memory								
$\overline{RD}$ pulse duration	t_{RR}	500	–	400	–	$6t_{CK}-100$	–	ns
$\overline{WR}$ pulse duration	t_{WW}	500	–	400	–	$6t_{CK}-100$	–	ns
Address set-up time to ALE	t_{AL}	45	–	28	–	$t_{CK}-55$	–	ns
Address hold time after ALE	t_{LA}	65	–	48	–	$t_{CK}-35$	–	ns
$\overline{RD}$ to valid data input	t_{RD}	–	335	–	252	–	$5t_{CK}-165$	ns
Data hold time after $\overline{RD}$	t_{DR}	0	–	0	–	0	–	ns
Data float delay after $\overline{RD}$	t_{DFR}	–	130	–	97	–	$2t_{CK}-70$	ns
Time from ALE to valid data input	t_{LD}	–	650	–	517	–	$8t_{CK}-150$	ns
Address to valid data input	t_{AD}	–	735	–	585	–	$9t_{CK}-165$	ns
Time from ALE to $\overline{RD}$ or $\overline{WR}$	t_{LW}	250	350	200	300	$3t_{CK}-50$	$3t_{CK}+50$	ns
Time from address to $\overline{RD}$ or $\overline{WR}$	t_{AW}	270	–	203	–	$4t_{CK}-130$	–	ns
Time from $\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	t_{WHLH}	60	140	43	123	$t_{CK}-40$	$t_{CK}+40$	ns
Data valid to $\overline{WR}$ transition	t_{DWX}	40	–	23	–	$t_{CK}-60$	–	ns
Data set-up time before $\overline{WR}$	t_{DW}	550	–	433	–	$7t_{CK}-150$	–	ns
Data hold time after $\overline{WR}$	t_{WD}	50	–	33	–	$t_{CK}-50$	–	ns
Address float delay after $\overline{RD}$	t_{AFR}	–	0	–	0	–	0	ns

Where:

$1/t_{CK}$ = 1,2 to 12 MHz (see Fig. 15 and Table 6)

t_{CY} = 12 t_{CK} (see Fig. 16 and DC characteristics)

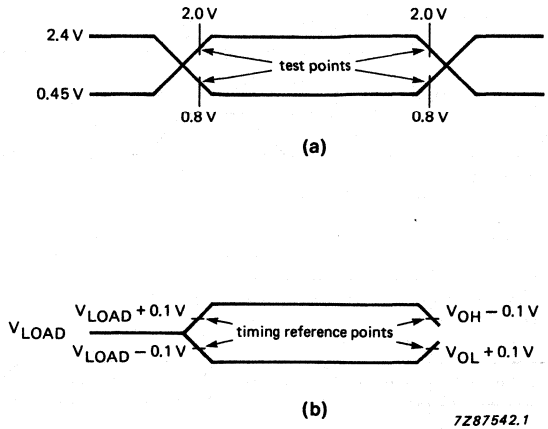


Fig. 14 AC testing input, output waveform (a) and float waveform (b).

AC testing inputs are driven at 2.4 V for a logic 1 and 0.45 V for a logic 0. Timing measurements are taken at 2.0 V for a logic 1 and 0.8 V for logic 0. The float state is defined as the point at which a Port 0 pin sinks 3.2 mA or sources 400 μA at the voltage test levels.

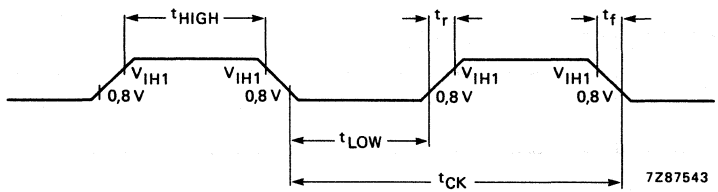


Fig. 15 External clock drive XTAL 1 (see Table 6).

Table 6 External clock drive XTAL 1 (see Fig. 15)

parameter	symbol	variable clock (f = 1.2 to 12 MHz)		unit
		min.	max.	
oscillator clock period	t_{CK}	83	833	ns
HIGH time	t_{HIGH}	20	$t_{CK}-t_{LOW}$	ns
LOW time	t_{LOW}	20	$t_{CK}-t_{HIGH}$	ns
rise time	t_r	–	20	ns
fall time	t_f	–	20	ns
cycle time	$t_{CY} = 12\ t_{CK}$	1	10	μs

AC CHARACTERISTICS (continued)

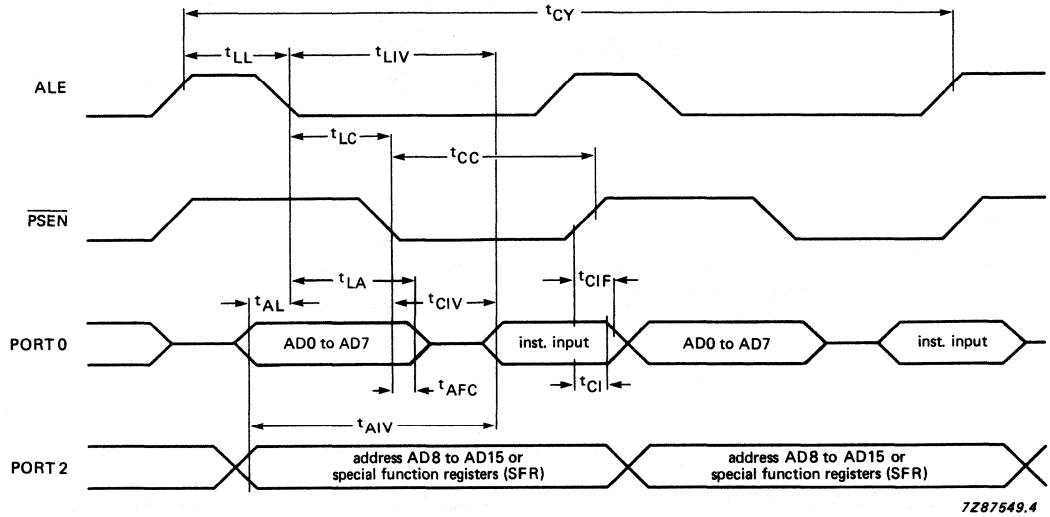


Fig. 16 Read from program memory.

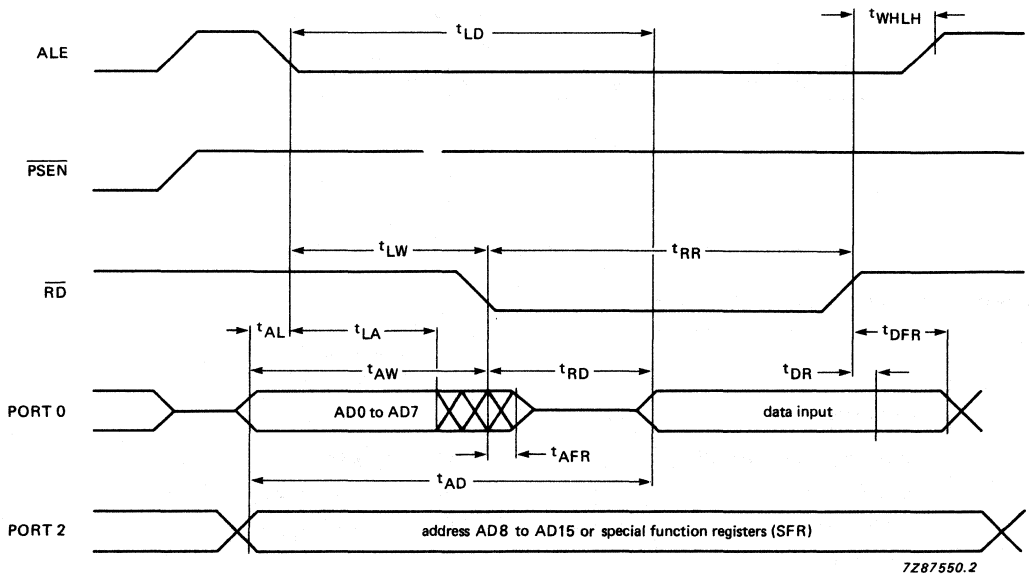


Fig. 17 Read from data memory.

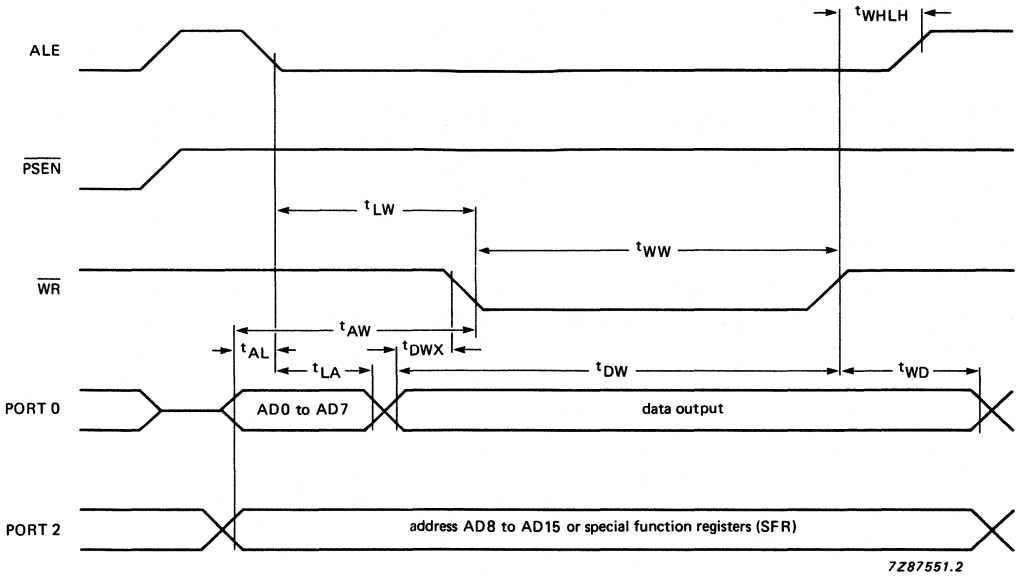


Fig. 18 Write to data memory.

DEVELOPMENT DATA

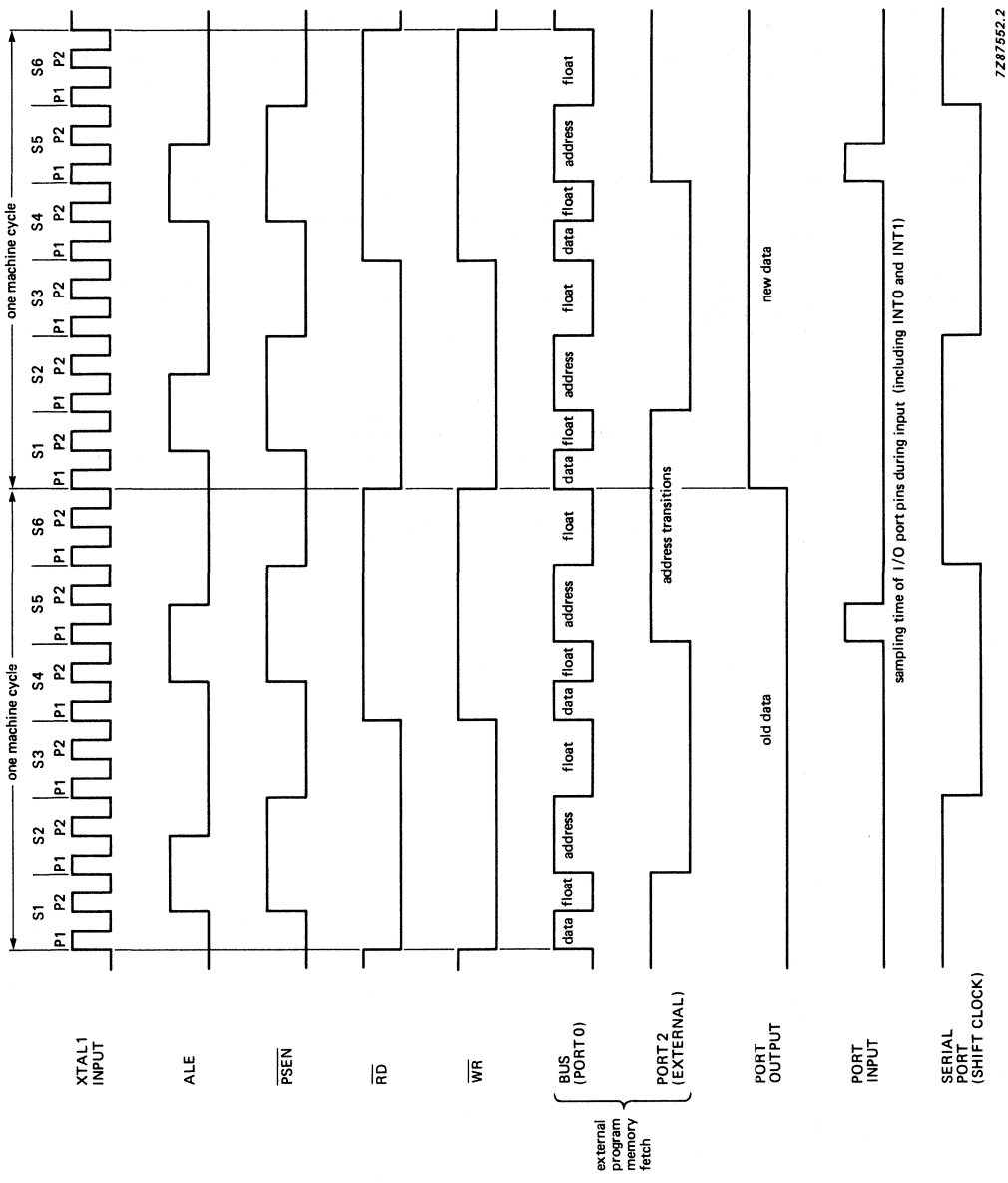


Fig. 19 Instruction cycle timing.

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C654 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The PCB83C654 has the same instruction set as the PCB80C51. The ROM-less PCB80C652 should be used for development purposes.

This device provides architectural enhancements that make it applicable in a variety of applications in general control systems.

The PCB83C654 contains a non-volatile 16 K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C654 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.

Features

- 80C51 central processing unit
- 16 K x 8 ROM, expandable externally to 64 K bytes
- 256 x 8 RAM, expandable externally to 64 K bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART facilities

- **A version for extended temperature range is in preparation**

PACKAGE OUTLINES

PCB83C654P : 40-lead DIL; plastic (SOT129).
PCB83C654WP: 44-lead plastic leaded chip-carrier (PLCC); (SOT187 pedestal or SOT187AA pocket version depending on source, versions are interchangeable).
PCB83C654H : 44-lead quad flat-pack; plastic (SOT205A) in preparation.

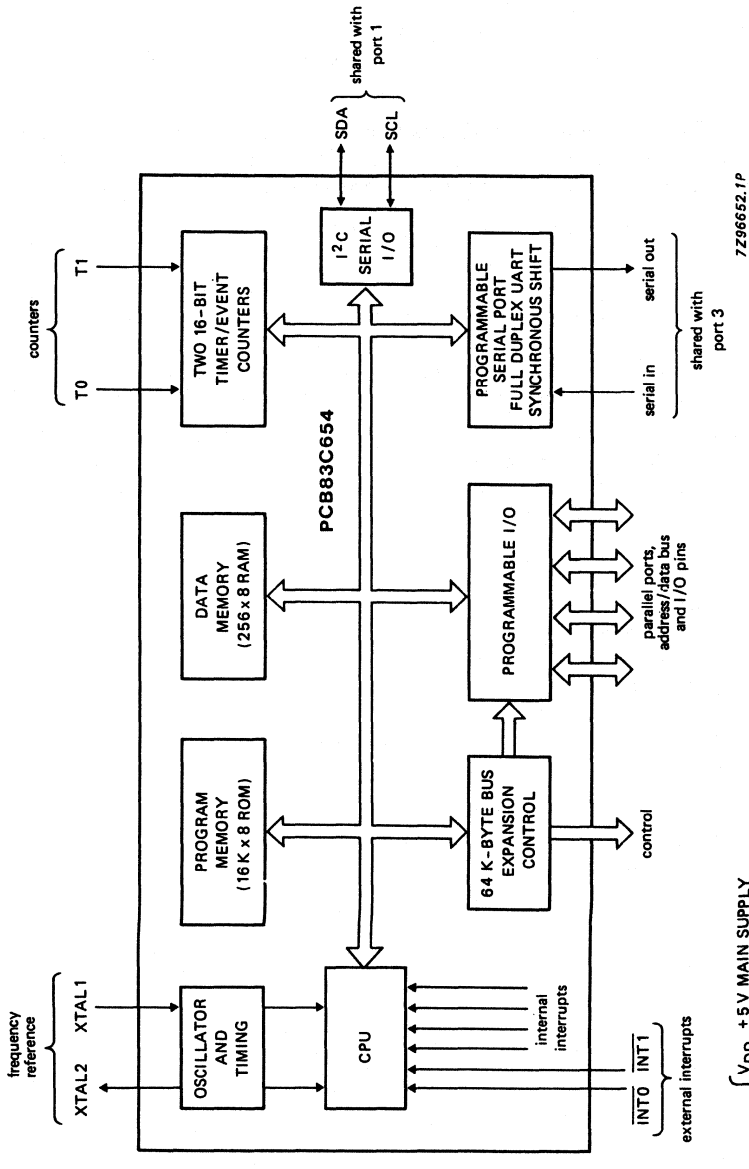


Fig. 1 Block diagram.

DEVELOPMENT DATA

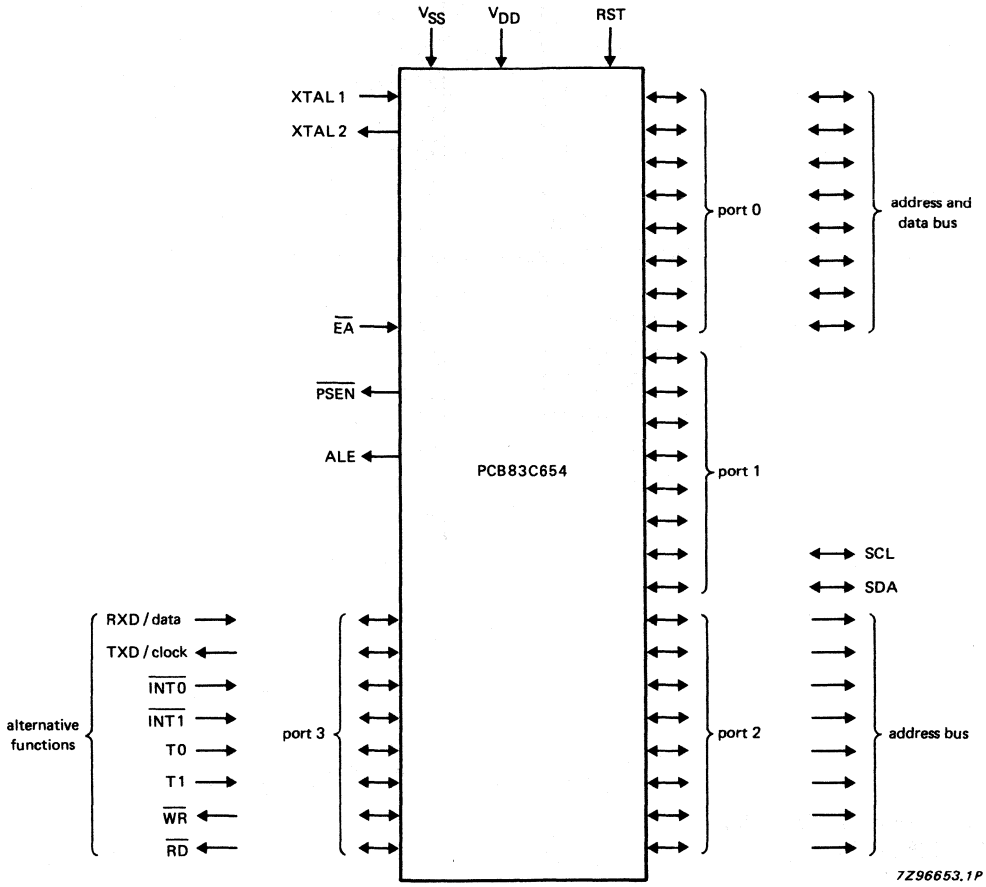


Fig. 2 Functional diagram.

Fig. 3a Pinning diagram for PCB83C654P.

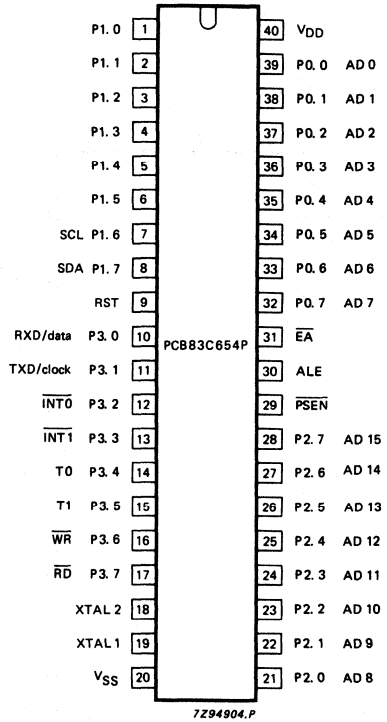
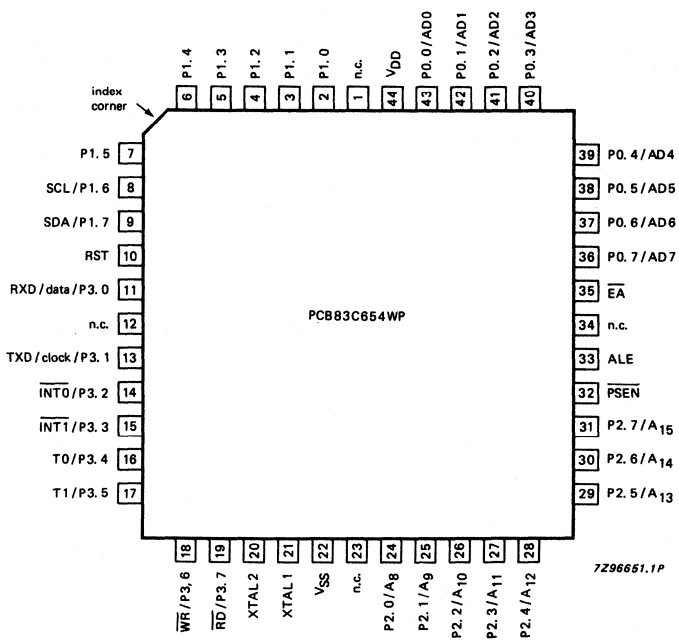


Fig. 3b Pinning diagram for PCB83C654WP.



PINNING (PCB83C654P, PCB80C654P)

1-8	P1.0-P1.7	**Port 1:** 8-bit quasi-bidirectional I/O port. Port 1 can sink/source one TTL (= 4 LSTTL) input. It can drive CMOS inputs without external pull-ups, except P1.6 and P1.7 which have open drain outputs.

Port pin	Alternative function
P1.6	SCL: I^2C-bus serial port clock line
P1.7	SDA: I^2C-bus serial port data line

9	RST	**RESET:** a high level on this pin for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to V_{DD}.
10-17	P3.0-P3.7	**Port 3:** 8-bit quasi-bidirectional I/O port with internal pull-ups. It also serves the following alternative functions:

Port pin	Alternative function
P3.0	RXD/data: serial port receiver data input (asynchronous) or data input/output (synchronous)
P3.1	TXD/clock: serial port transmitter data output (asynchronous) or clock output (synchronous)
P3.2	$\overline{INT0}$: external interrupt 0 or gate control input for timer/event counter 0
P3.3	$\overline{INT1}$: external interrupt 1 or gate control input for timer/event counter 1
P3.4	T0: external input for timer/event counter 0
P3.5	T1: external input for timer/event counter 1
P3.6	$\overline{WR}$: external data memory write strobe
P3.7	$\overline{RD}$: external data memory read strobe

The generation or use of a Port 3 pin as an alternative function is carried out automatically by the PCB83C654 provided the associated Special Function Register bit is set high. Port 3 can sink/source one TTL (= 4 LSTTL) input. It can drive CMOS inputs without external pull-ups.

18	XTAL 2	**Crystal input 2:** output of the inverting amplifier that forms the oscillator. Left open-circuit when an external oscillator clock is used (see Figs 10 and 11).
19	XTAL 1	**Crystal input 1:** input to the inverting amplifier that forms the oscillator, and input to the internal clock generator. Receives the external oscillator clock signal when an external oscillator is used (see Figs 10 and 11).
20	V_{SS}	**Ground:** circuit ground potential.
21-28	P2.0-P2.7	**Port 2:** 8-bit quasi-bidirectional I/O port with internal pull-ups. During access to external memories (RAM/ROM) that use 16-bit addresses (MOVX @DPTR) Port 2 emits the high order address byte. When external RAM is accessed with an 8-bit address (MOVX @Ri) Port 2 emits the contents of the P2 special function register. Port 2 can sink/source one TTL (= 4 LSTTL) input. It can drive CMOS inputs without external pull-ups.
29	$\overline{PSEN}$	**Program Store Enable output:** read strobe to the external program memory via port 0 and 2. It is activated twice each machine cycle during fetches from external program memory. When executing out of external program memory two activations of $\overline{PSEN}$ are skipped during each access to external data memory. $\overline{PSEN}$ is not activated (remains HIGH) during no fetches from external program memory. $\overline{PSEN}$ can sink/source 8 LSTTL inputs. It can drive CMOS inputs without an external pull-up.
30	ALE	**Address Latch Enable output:** latches the low byte of the address during accesses to external memory in normal operation. It is activated every six oscillator periods except during an external data memory access. ALE can sink/source 8 LSTTL inputs. It can drive CMOS inputs without an external pull-up.

PINNING (continued)

31	$\overline{EA}$	**External Access input:** When $\overline{EA}$ is held at a TTL high level the CPU executes out of the internal program ROM provided the program counter is less than 8192. When $\overline{EA}$ is held at a TTL low level, the CPU executes out of external program memory via port 0 and port 2. $\overline{EA}$ is not allowed to float.
32-39	P0.7-P0.0	**Port 0:** 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus during accesses to external memory (during these accesses it activates internal pull-ups). Port 0 can sink/source eight LSTTL inputs.
40	V_{DD}	**Power supply:** + 5 V power supply pin during normal operation, Idle mode and Power-down mode.

To avoid a 'latch-up' effect at power-on, the voltage on any pin at any time must not be higher or lower than V_{DD} + 0,5 V or V_{SS} − 0,5 V respectively.

FUNCTIONAL DESCRIPTION

General

The PCB83C654 is a stand-alone high-performance microcontroller designed for use in real-time applications such as instrumentation and industrial control.

The device provides, in addition to the 80C51 standard functions, a serial I^2C-bus interface. As well as the parallel bus, functions may also be expanded using the I^2C-bus utilizing the complete line of the I^2C clips family.

The PCB83C654 is a control-oriented CPU with on-chip program and data memory. It can be extended with external program memory up to 64 K bytes. It can also access up to 64 K bytes of external data memory. For systems requiring extra capability, the PCB83C654 can be expanded using standard memories and peripherals.

The PCB83C654 has two software selectable modes of reduced activity for further power reduction – Idle and Power-down. The Idle mode freezes the CPU while allowing the RAM, timers, serial ports and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator causing all other chip functions to be inoperative.

Memory organization

The central processing unit (CPU) manipulates operands in three memory spaces; these are the 64 K-byte external data memory, 256-byte internal data memory and the 64 K-byte internal and external program memory. The internal data memory address space is sub-divided into the 256-byte internal data RAM and 128-byte Special Function Register (SFR) address spaces, as shown in Fig. 4. Figure 5 shows the Special Function Register memory map. Internal RAM locations 0-127 are directly and indirectly addressable. Internal RAM locations 128-255 are only indirectly addressable. The special function register locations 128-255 are only directly addressable.

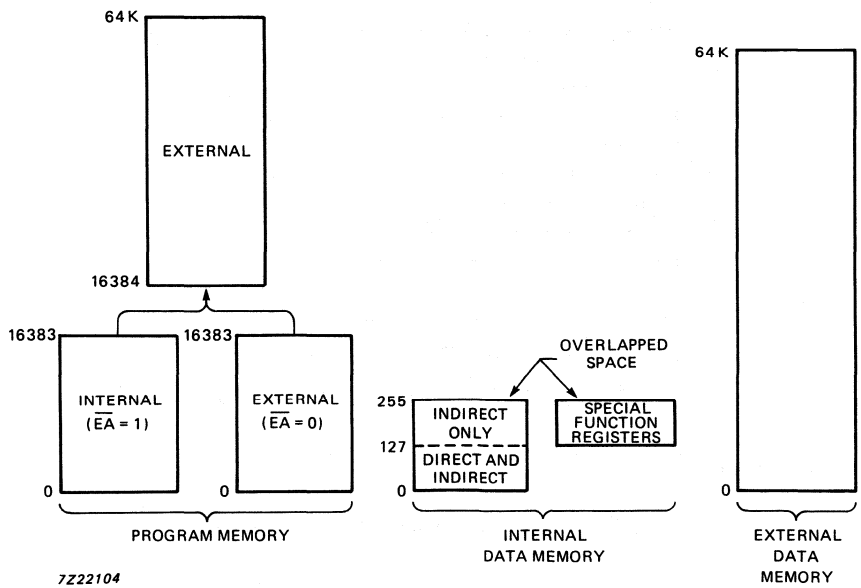
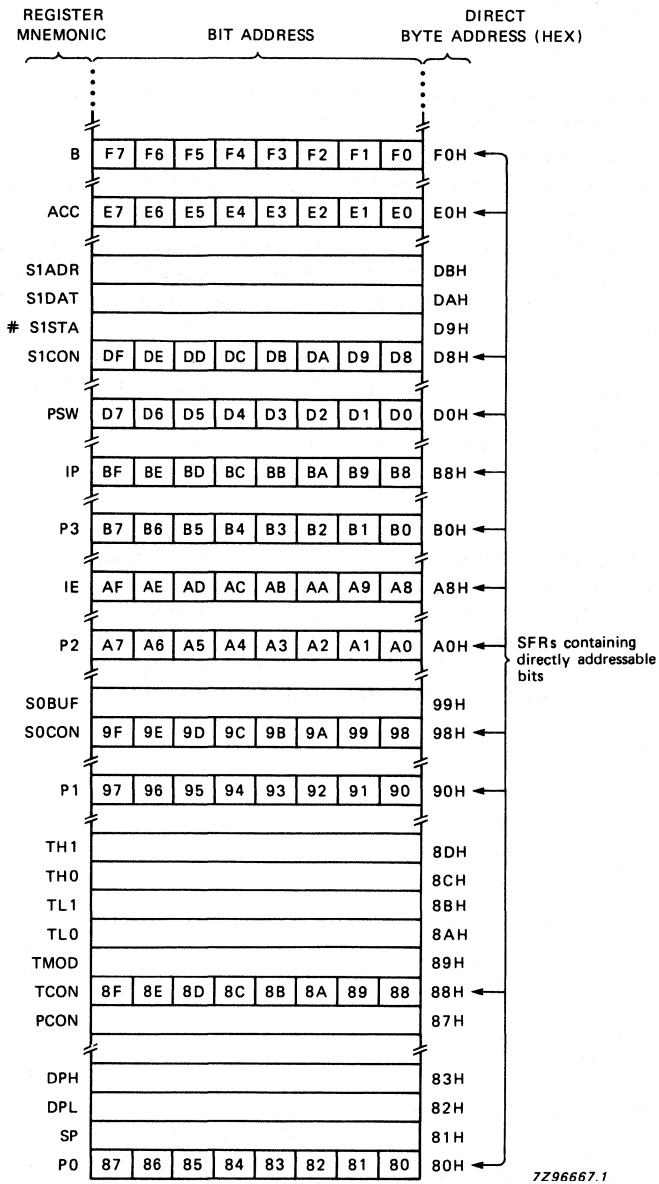


Fig. 4 Memory map.



S1STA is a read-only register.

Fig. 5 Special function registers memory map.

FUNCTIONAL DESCRIPTION (continued)

The internal data RAM contains four register banks (each with eight registers), 128 addressable bits, a scratchpad area and the stack. The stack depth is limited by the available internal data RAM and its location is determined by the 8-bit stack pointer. All registers except the program counter and the four 8-register banks reside in the special function register address space. These memory mapped registers include arithmetic registers, pointers, I/O ports, interrupt system registers, timers and serial port registers. There are 128 addressable bit locations in the SFR address space.

The PCB83C654 contains 256 bytes of internal data RAM and 25 special function registers. It provides a non-paged program memory address space to accommodate relocatable code. Conditional branches are performed relative to the program counter. The register-indirect jump permits branching relative to a 16-bit base register with an offset provided by an 8-bit index register. 16-bit jumps and calls permit branching to any location in the contiguous 64 K program memory address space.

Addressing

The PCB83C654 has five methods for addressing source operands:

- Register
- Direct
- Register-Indirect
- Immediate
- Base-Register plus Index-Register-Indirect

The first three methods can be used for addressing destination operands. Most instructions have a "destination/source" field that specifies the data type, addressing methods and operands involved. For operations other than MOVs, the destination operand is also a source operand.

Access to memory addressing is as follows:

- Registers in one of the four 8-register banks through Register, Direct, or Register-Indirect.
- 256 bytes of internal data RAM through Direct or Register-Indirect. Bytes 0-127 may be addressed directly/indirectly. Bytes 128-255 share their address locations with the SFR registers and so may only be addressed indirectly as data RAM.
- Special function registers through Direct at address locations 128-255.
- External data memory through Register-Indirect.
- Program memory look-up tables through Base-Register plus Index-Register-Indirect.

The PCB83C654 is classified as an 8-bit device since the internal ROM, RAM, Special Function Registers (SFR), Arithmetic Logic Unit (ALU) and external data bus are each 8-bits wide. It performs operations on bit, nibble, byte and double-byte data types.

Facilities are available for byte transfer, logic and integer arithmetic operations. Data transfer, logic and conditional branch operations can be performed directly on Boolean variables to provide excellent bit handling.

Instruction set

The PCB83C654 uses the powerful instruction set of the PCB80C51. Additional special function registers are incorporated to control the on-chip peripherals. The instruction set consists of 49 single-byte, 45 two-byte and 17 three-byte instructions. When using a 12 MHz oscillator, 64 instructions execute in 1 μs and 45 instructions execute in 2 μs. Multiply and divide instructions execute in 4 μs.

FUNCTIONAL DESCRIPTION (continued)

I/O facilities

The PCB83C654 has four 8-bit ports. Ports 0-3 are the same as in the 80C51, with the exception of the additional functions of port 1. Port lines P1.7 and P1.6 may be selected as the SDA and SCL lines of serial port SIO1 (I^2C). Because the I^2C bus may be active while the device is disconnected from V_{DD}, these pins are provided with open drain drivers.

N.B. Therefore pins P1.7 and P1.6 do not have pull-up devices when used as ports.

Ports 0, 1, 2 and 3 perform the following alternative functions:

- Port 0: provides the multiplexed low-order address and data bus used for expanding the PCB83C654 with standard memories and peripherals.
- Port 1: Port 1 is partly used for the I^2C bus functions;
  - SCL and SDA for the I^2C interface, P1.6 and P1.7 respectively.

Pins whose alternate function is not used may be used as normal bidirectional I/O pins.

- Port 2: provides the high-order address bus when expanding the PCB83C654 with external program memory and/or external data memory.
- Port 3: pins can be configured individually to provide:
  - external interrupt request inputs
  - counter inputs
  - serial port receiver input and transmitter output
  - control signals to READ and WRITE external data memory

A Port 3 pin automatically assumes its alternative function when the associated Special Function Register bit is set high.

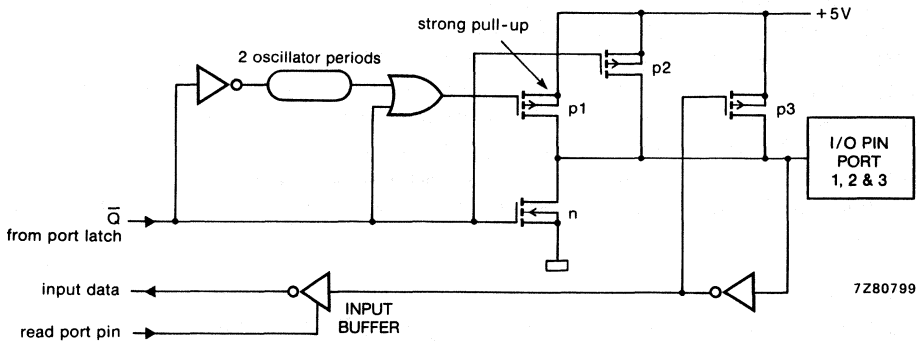


Fig. 6 I/O buffers in the PCB83C654 (Ports 2, 3, and P1.0 to P1.5).

Timer/event counters

The PCB83C654 contains two 16-bit timer/event counters: Timer 0 and Timer 1. Timer 0 and Timer 1 may be programmed to carry out the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests.

Timer 0 and Timer 1 can be programmed independently to operate in three modes:

- Mode 0: 8-bit timer or 8-bit counter each with divide by 32 prescaler
- Mode 1: 16-bit time-interval or event counter
- Mode 2: 8-bit time-interval or event counter with automatic reload upon overflow.

Timer 0 can be programmed to operate in an additional mode as follows:

- Mode 3: one 8-bit time-interval or event counter and one 8-bit time-interval counter.

When Timer 0 is in Mode 3, Timer 1 can be programmed to operate in Modes 0, 1 or 2 but cannot set an interrupt request flag or generate an interrupt. However the overflow from Timer 1 can be used to pulse the serial port transmission-rate generator.

The frequency handling range of these counters with a 12 MHz crystal is as follows:

- In the timer function, the timer is incremented at a frequency of 1 MHz – a division by 12 of the oscillator frequency
- 0 Hz to an upper limit of 0,5 MHz when programmed for external inputs.

Both internal and external inputs can be gated to the counter by a second external source for directly measuring pulse durations.

The counters are started and stopped under software control. Each one sets its interrupt request flag when it overflows from all logic 1s to all logic 0s (or automatic reload value), with the exception of mode 3 as previously described.

Serial I/O (see Fig. 7)

The PCB83C654 is equipped with two independent serial ports. SIO0 is the full duplex UART port and is identical to the serial port of the PCB80C51.

Serial port SIO1 supports the I^2C-bus, the function of which is controlled by the S1CON register. S1STA is the status register whose contents may also be used as a vector to various service routines. S1DAT is the data shift register and S1ADR the slave address register. The least significant bit of S1ADR enables/disables general call address recognition.

FUNCTIONAL DESCRIPTION (continued)

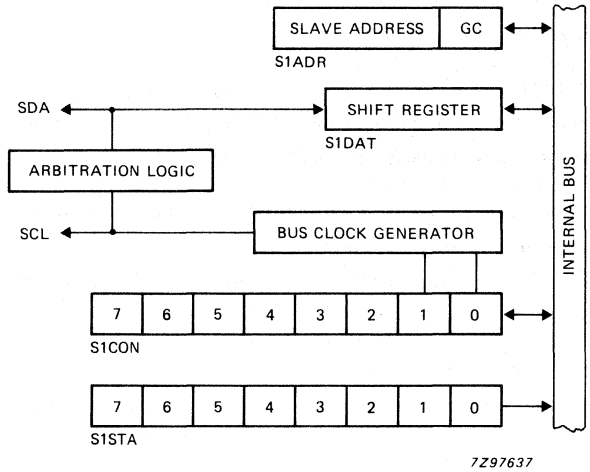


Fig. 7 Block diagram of I²C serial I/O.

The I²C serial I/O has complete autonomy in byte handling and operates in 4 modes:

1. Master transmitter
2. Master receiver
3. Slave transmitter
4. Slave receiver

Slave address recognition is performed by on-chip hardware.

The I²C-bus consists of two lines: a data line (SDA) and a clock line (SCL). These lines also function as the I/O port lines on P1.7 and P1.6. The system is unique because data transport, clock generation, address recognition and bus control arbitration are all controlled by hardware.

Serial control register S1CON

	7	6	5	4	3	2	1	0
S1CON(D8H)	X	ENS1	STA	STO	SI	AA	CR1	CR0

Bits CR1 and CR0 determine the clock frequency that is generated in the master mode of operation. Table 1 displays the clock rate when using a 12 MHz crystal.

Table 1 Clock rate when using a 12 MHz crystal

CR1 / CR0	bit frequency	f_{osc} divided by
0 0	12,5 kHz	960
0 1	100 kHz	120
1 0	200 kHz	60 ($f_{osc} < 6$ MHz meeting I²C)
1 1	62,5–0,5 kHz	96 x (256–reload value Timer 1) (reload value range: 0-254 in mode 2)

AA

Assert acknowledge bit. When this bit is set, an acknowledge is returned after any one of the following conditions:

- Own slave address is received
- General call address is received (S1ADR.0 = logic 1)
- A data byte is received, while the device is programmed to be a master receiver
- A data byte is received, while the device is a selected slave receiver.

When this bit is reset, no acknowledge is returned. Consequently, no interrupt is requested when the own address or general call address is received.

SI

SIO1 interrupt flag. This flag is set by hardware and an interrupt request is generated after any of the following events occur:

- A START condition is generated in MST mode
- The own slave address has been received during AA = logic 1
- The general call address has been received while S1ADR.0 and AA = logic 1
- A data byte has been received or transmitted in MST mode (even if arbitration is lost)
- A data byte has been received or transmitted as selected slave
- A STOP or START condition is received as selected slave receiver or transmitter.

While the SI flag is set, SCL remains LOW and the serial transfer is suspended.
SI must be reset by software.

STO

STOP flag. When in master mode,and this bit is set a STOP condition is generated. A STOP condition detected on the I^2C-bus clears this bit. This bit may also be set in slave mode in order to recover from an error condition. Then no STOP condition is generated to the I^2C-bus, but the hardware releases the SDA and SCL lines and switches to the not selected slave receiver mode. The STOP flag is cleared by the hardware.

STA

START flag. When this bit is set, the hardware checks the I^2C-bus and generates a START condition if the bus is free. If the device is already programmed as either master/transmitter or master/receiver, it will generate a repeated START condition.

ENS1

0 = Serial I/O Disabled and reset.Output ports P1.6 and P1.7 function with open drain

1 = Serial I/O Enabled. Output ports P1.6 and P1.7 must be set to logic 1.

FUNCTIONAL DESCRIPTION (continued)

Serial status register S1STA (S1STA is a read-only register)

	7	6	5	4	3	2	1	0
S1STA(D9H)	SC4	SC3	SC2	SC1	SC0	0	0	0

S1STA.3 - S1STA.7 hold a status code. S1STA.0 - S1STA.2 are held LOW. The contents of the status register may be used as a vector to a service routine. This optimizes the response time of the software and consequently that of the I^2C-bus.

Abbreviations used:

SLA : 7-bit slave address
R : Read bit
W : Write bit
$\underline{ACK}$: Acknowledgement (acknowledge bit = logic 0)
$\overline{ACK}$: Not acknowledgement (acknowledge bit = logic 1)
DATA : 8-bit data byte to or from I^2C bus
MST : Master
SLV : Slave
TRX : Transmitter
REC : Receiver

The following is a list of the status codes:

MST/TRX mode

S1STA value

- 08H - A START condition has been transmitted
- 10H - A repeated START condition has been transmitted
- 18H - SLA and W have been transmitted, $\underline{ACK}$ has been received
- 20H - SLA and W have been transmitted, $\overline{ACK}$ received
- 28H - DATA of S1DAT has been transmitted, $\underline{ACK}$ received
- 30H - DATA of S1DAT has been transmitted, $\overline{ACK}$ received
- 38H - Arbitration lost in SLA, R/W or DATA

MST/REC mode

S1STA value

- 38H - Arbitration lost while returning $\overline{ACK}$
- 40H - SLA and R have been transmitted, $\underline{ACK}$ received
- 48H - SLA and R have been transmitted, $\overline{ACK}$ received
- 50H - DATA has been received, $\underline{ACK}$ returned
- 58H - DATA has been received, $\overline{ACK}$ returned

SLV/REC mode

S1STA value

- 60H - Own SLA and W have been received, ACK returned
- 68H - Arbitration lost in SLA, R/W as MST. Own SLA and W have been received, ACK returned
- 70H - General CALL has been received, ACK returned
- 78H - Arbitration lost in SLA, R/W as MST. General call has been received
- 80H - Previously addressed with own SLA. DATA byte received, ACK returned
- 88H - Previously addressed with own SLA. DATA byte received, $\overline{\text{ACK}}$ returned
- 90H - Previously addressed with general call. DATA byte has been received, ACK has been returned
- 98H - Previously addressed with general call. DATA byte has been received, $\overline{\text{ACK}}$ has been returned
- A0H - A STOP condition or repeated START condition has been received while still addressed as SLV/REC or SLV/TRX.

SLV/TRX mode

S1STA value

- A8H - Own SLA and R have been received, ACK returned
- B0H - Arbitration lost in SLA, R/W as MST. Own SLA and R have been received, ACK returned
- B8H - DATA byte has been transmitted, ACK received
- C0H - DATA byte has been transmitted, $\overline{\text{ACK}}$ received
- C8H - Last DATA byte has been transmitted (AA = logic 0), ACK received.

Miscellaneous

S1STA value

- 00H - Bus error during MST mode or selected SLV mode, due to an erroneous START or STOP condition

The data shift register S1DAT

S1DAT(DAH)	7	6	5	4	3	2	1	0

This register contains the serial data to be transmitted or data which has just been received. Bit 7 is transmitted or received first; i.e. data is shifted from right to left.

Address register S1ADR

	slave address							GC
S1ADR (DBH)	7	6	5	4	3	2	1	0

S1ADR.0, GC : 0 = general call address is not recognized
1 = general call address is recognized

S1ADR.7-1 : own slave address

This 8-bit register may be loaded with the 7-bit slave address to which the controller will respond when programmed as a slave receiver/transmitter. The LSB (GC) is used to determine whether the general call address is recognized.

FUNCTIONAL DESCRIPTION (continued)

Idle and Power-down operation (see Fig. 8)

Idle mode operation permits the interrupt, serial ports and timer blocks to continue to function while the CPU is halted.

The following functions remain active during Idle mode. These functions may generate an interrupt or reset and thus end the Idle mode:

Timer 0, Timer 1
SIO0, SIO1
External interrupt

The Power-down operation freezes the oscillator. The Power-down mode can only be activated by setting the PD bit in the PCON register.

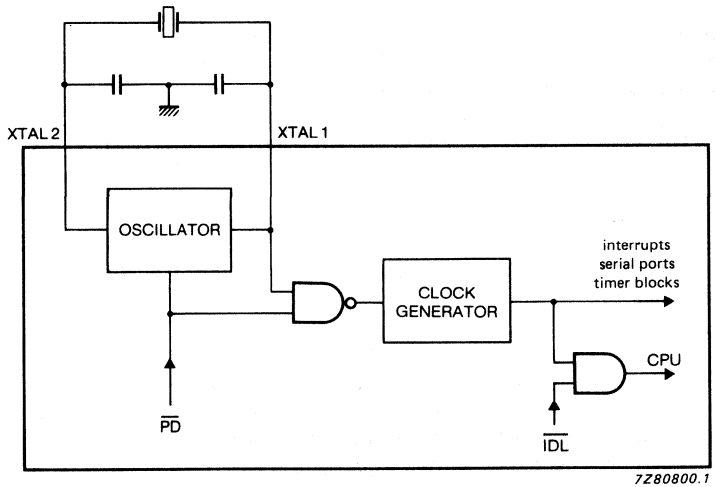


Fig. 8 Internal Idle and Power-down clock configuration.

Power control register

These special modes are activated by software via the Special Function Register PCON. Its hardware address is 87H. PCON is not bit addressable.

	7	6	5	4	3	2	1	0
PCON(87H)	SMOD	–	–	–	GF1	GF0	PD	IDL

Bit	Symbol	Function
PCON.7	SMOD	Double Baud rate bit. When set to logic 1 the baud rate is doubled when the serial port SIO0 is being used in modes 1, 2 or 3
PCON.6	–	(reserved)
PCON.5	–	(reserved)
PCON.4	–	(reserved)
PCON.3	GF1	General-purpose flag bit
PCON.2	GF0	General-purpose flag bit
PCON.1	PD	Power-down bit. Setting this bit activates Power-down mode
PCON.0	IDL	Idle mode bit. Setting this bit activates the Idle mode.

If logic 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is 0XXX0000.

Idle mode

The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before Idle mode is activated. Once in the Idle mode, the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during Idle mode. The status of the external pins during Idle mode is shown in Table 2.

There are two ways to terminate the Idle mode:

Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware terminating Idle mode. The interrupt is serviced, and following return from interrupt instruction RETI, the next instruction to be executed will be the one which follows the instruction that wrote a logic 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an interrupt, the service routine can examine the status of the flags bits.

The second way of terminating the Idle mode is with an external hardware reset. Since the oscillator is still running, the hardware reset is required to be active for two machine cycles (24 oscillator periods) to complete the reset operation.

Power-down mode

The instruction that sets PCON.1 is the last executed prior to going into the Power-down mode. Once in Power-down mode, the oscillator is stopped. Only the contents of the on-chip RAM are preserved. The Special Function Registers are not saved. A hardware reset is the only way of exiting the Power-down mode.

In the Power-down mode, V_{DD} may be reduced to minimize circuit power consumption. The voltage must not be reduced until the Power-down mode is entered, but must be restored before the hardware reset is applied which will free the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

The status of the external pins during Power-down mode is shown in Table 2. If the Power-down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to port 2. If the data is a logic 1, the port pin is held HIGH during the Power-down mode by the strong pull-up transistor p1 (see Fig. 6).

FUNCTIONAL DESCRIPTION (continued)

Table 2 Status of the external pins during Idle and Power-down modes.

mode	memory	ALE	$\overline{PSEN}$	Port 0	Port 1	Port 2	Port 3
Idle	internal	1	1	port data	port data	port data	port data
Idle	external	1	1	floating	port data	address	port data
Power-down	internal	0	0	port data	port data	port data	port data
Power-down	external	0	0	floating	port data	port data	port data

Note: Ports 1.7 and 1.6 if selected, function as SDA and SCL respectively in the Idle mode.

Interrupt system (see Fig. 9)

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution a multiple-source, two-priority-level, nested interrupt system is provided. Interrupt response latency is from 3 μs to 8 μs when using a 12 MHz crystal. The PCB83C654 acknowledges interrupt requests from six sources as follows:

- $\overline{INT0}$ and $\overline{INT1}$: two external interrupts
- Timer 0 and Timer 1: two internal counters
- I^2C serial I/O interrupt
- UART serial I/O port interrupt

Each interrupt vectors to a separate location in program memory for its service program. Each source can be individually enabled or disabled by a corresponding bit in the IE register, moreover each interrupt may be programmed to a high or low priority level using a corresponding bit in the IP register. Also all enabled sources can be globally disabled or enabled. Both external interrupts can be programmed to be level-activated or transition-activated; an active LOW level allows "wire-ORing" of several interrupt sources to the input pin.

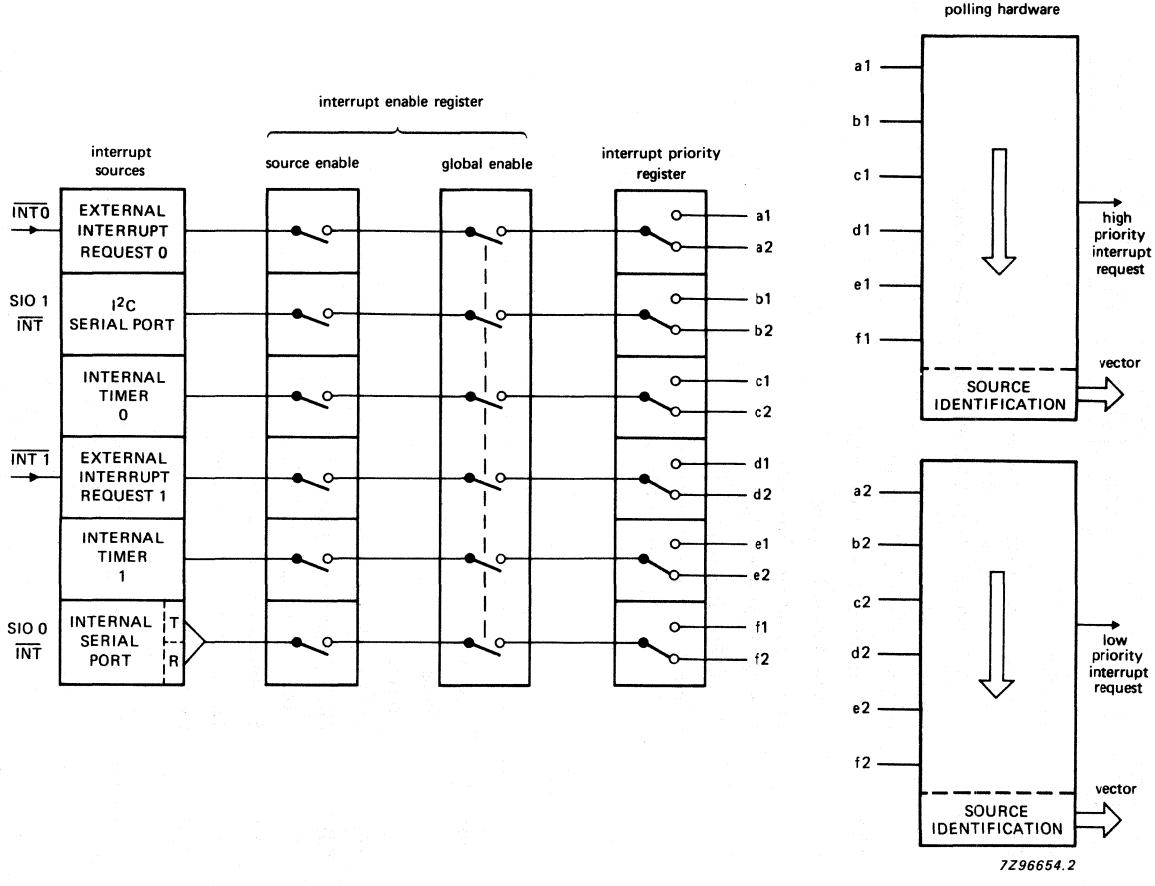


Fig. 9 Interrupt system.

FUNCTIONAL DESCRIPTION (continued)

Interrupt enable register

	7	6	5	4	3	2	1	0
IE(A8H)	EA	–	ES1	ES0	ET1	EX1	ET0	EX0

Bit	Symbol	Function
IE.7	EA	General enable/disable control 0 = No interrupt is enabled 1 = Any individually enabled interrupt will be accepted
IE.6	–	Unused
IE.5	ES1	Enable SIO1 (I^2C) interrupt
IE.4	ES0	Enable SIO0 (UART) interrupt
IE.3	ET1	Enable Timer 1 interrupt
IE.2	EX1	Enable External 1 interrupt
IE.1	ET0	Enable Timer 0 interrupt
IE.0	EX0	Enable External 0 interrupt
		where "0" = interrupt disabled and "1" = interrupt enabled

Interrupt priority register

	7	6	5	4	3	2	1	0
IP(B8H)	–	–	PS1	PS0	PT1	PX1	PT0	PX0

Bit	Symbol	Function
IP.7	–	Unused
IP.6	–	Unused
IP.5	PS1	SIO1 (I^2C) interrupt priority level
IP.4	PS0	SIO0 (UART) interrupt priority level
IP.3	PT1	Timer 1 interrupt priority level
IP.2	PX1	External interrupt 1 priority level
IP.1	PT0	Timer 0 interrupt priority level
IP.0	PX0	External interrupt 0 priority level

Interrupt priority levels are as follows: "0" – low priority
"1" – high priority

Table 3 shows the interrupt vectors. The vector indicates the ROM location where the appropriate interrupt service routine starts.

Table 3 Interrupt vectors

Source		Vector
External 0	X0	0003H
Timer 0 overflow	T0	000BH
External 1	X1	0013H
Timer 1 overflow	T1	001BH
Serial I/O 0 (UART)	S0	0023H
Serial I/O 1 (I^2C)	S1	002BH

Interrupt priority

Each interrupt source can be either high priority or low priority. If both priorities are requested simultaneously, the processor will branch to the high priority vector. If there are simultaneous requests from sources of the same priority, then interrupts will be serviced in the following order:

X0, S1, T0, X1, T1, S0

A low priority interrupt routine can only be interrupted by high priority interrupt. A high priority interrupt routine can not be interrupted.

Oscillator circuitry

The oscillator circuitry of the PCB83C654 is a single-stage inverting amplifier in a Pierce oscillator configuration. The circuitry between XTAL 1 and XTAL 2 is basically an inverter biased to the transfer point. Either a crystal or ceramic resonator can be used as the feedback element to complete the oscillator circuitry. Both are operated in parallel resonance. XTAL 1 is the high gain amplifier input, and XTAL 2 is the output (see Fig. 10). To drive the PCB83C654 externally, XTAL 1 is driven from an external source and XTAL 2 left open-circuit (see Fig. 11).

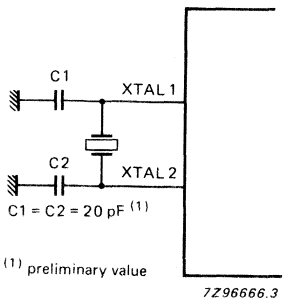


Fig. 10 PCB83C654 oscillator circuit.

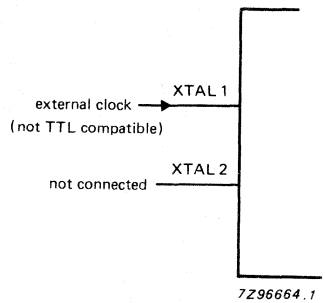


Fig. 11 Driving the PCB83C654 from an external source.

FUNCTIONAL DESCRIPTION (continued)

Reset circuitry (see Fig. 12)

The reset circuitry for the PCB83C654 is connected to the reset pin RST. A Schmitt trigger is used at the input for noise rejection. The output of the Schmitt trigger is sampled by the reset circuitry every machine cycle.

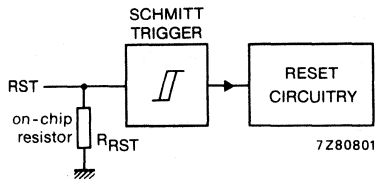


Fig. 12 On chip reset configuration.

A reset is accomplished by holding the RST pin HIGH for at least two machine cycles (24 oscillator periods). The CPU responds by executing an internal reset. During reset ALE and $\overline{PSEN}$ output a HIGH level. In order to perform a correct reset, this level must not be affected by external elements.

The internal reset is executed during the second cycle in which RST is HIGH and is repeated every cycle until RST goes LOW. It leaves the internal registers as follows:

Register	Content
ACC	0000 0000
B	0000 0000
DPL	0000 0000
DPH	0000 0000
IE	0x00 0000
IP	xx00 0000
PCH	0000 0000
PCL	0000 0000
PCON	0xxx 0000
PSW	0000 0000
P0 - P3	1111 1111
S0BUF	xxxx xxxx
S0CON	0000 0000
S1ADR	0000 0000
S1CON	x000 0000
S1DAT	0000 0000
S1STA	1111 1000
SP	0000 0111
TCON	0000 0000
TH0, TH1	0000 0000
TL0, TL1	0000 0000
TMOD	0000 0000

The internal RAM is not affected by reset. When V_{DD} is turned on, the RAM content is indeterminate.

Power-on reset (see Fig. 13)

When V_{DD} is turned on an automatic reset can be obtained by connecting the RST pin to V_{DD} via a 2,2 μF capacitor. When the power is switched on, the voltage on the RST pin is equal to V_{DD} minus the capacitor voltage, and decreases from V_{DD} as the capacitor charges through the internal resistor (R_{RST}) to ground. The larger the capacitor, the more slowly V_{RST} decreases. V_{RST} must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles.

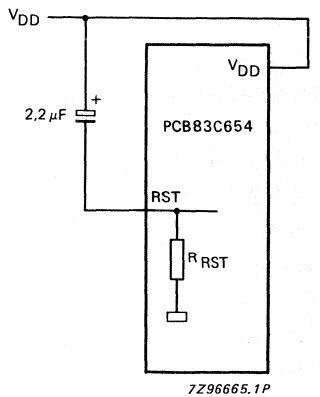


Fig. 13 Power-on reset.

INSTRUCTION SET

Table 4 Instruction set description

mnemonic	description	bytes/ cycles		opcode (hex.)
Arithmetic operations				
ADD A,Rr	Add register to A	1	1	2*
ADD A,direct	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect RAM to A	1	1	26, 27
ADD A,#data	Add immediate data to A	2	1	24
ADDC A,Rr	Add register to A with carry flag	1	1	3*
ADDC A,direct	Add direct byte to A with carry flag	2	1	35
ADDC A,@Ri	Add indirect RAM to A with carry flag	1	1	36, 37
ADDC A,#data	Add immediate data to A with carry flag	2	1	34
SUBB A,Rr	Subtract register from A with borrow	1	1	9*
SUBB A,direct	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect RAM from A with borrow	1	1	96, 97
SUBB A,#data	Subtract immediate data from A with borrow	2	1	94
INC A	Increment A	1	1	04

INSTRUCTION SET (continued)

mnemonic		description	bytes/ cycles		opcode (hex.)
Logic operations					
INC	Rr	Increment register	1	1	0*
INC	direct	Increment direct byte	2	1	05
INC	@Ri	Increment indirect RAM	1	1	06, 07
DEC	A	Decrement A	1	1	14
DEC	Rr	Decrement register	1	1	1*
DEC	direct	Decrement direct byte	2	1	15
DEC	@Ri	Decrement indirect RAM	1	1	16, 17
INC	DPTR	Increment data pointer	1	2	A3
MUL	AB	Multiply A & B	1	4	A4
DIV	AB	Divide A by B	1	4	84
DA	A	Decimal adjust A	1	1	D4
ANL	A,Rr	AND register to A	1	1	5*
ANL	A,direct	AND direct byte to A	2	1	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	1	54
ANL	direct,A	AND A to direct byte	2	1	52
ANL	direct,#data	AND immediate data to direct byte	3	2	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	1	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	1	44
ORL	direct,A	OR A to direct byte	2	1	42
ORL	direct,#data	OR immediate data to direct byte	3	2	43
XRL	A,Rr	Exclusive-OR register to A	1	1	6*
XRL	A,direct	Exclusive-OR direct byte to A	2	1	65
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	Exclusive-OR immediate data to A	2	1	64
XRL	direct,A	Exclusive-OR A to direct byte	2	1	62
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2	63
CLR	A	Clear A	1	1	E4
CPL	A	Complement A	1	1	F4
RL	A	Rotate A left	1	1	23
RLC	A	Rotate A left through the carry flag	1	1	33
RR	A	Rotate A right	1	1	03
RRC	A	Rotate A right through the carry flag	1	1	13
SWAP	A	Swap nibbles within A	1	1	C4

mnemonic	description	bytes/ cycles		opcode (hex.)
Data transfer				
MOV A,Rr	Move register to A	1	1	E*
MOV A,direct (**)	Move direct byte to A	2	1	E5
MOV A,@Ri	Move indirect RAM to A	1	1	E6, E7
MOV A,#data	Move immediate data to A	2	1	74
MOV Rr,A	Move A to register	1	1	F*
MOV Rr,direct	Move direct byte to register	2	2	A*
MOV Rr,#data	Move immediate data to register	2	1	7*
MOV direct,A	Move A to direct byte	2	1	F5
MOV direct,Rr	Move register to direct byte	2	2	8*
MOV direct,direct	Move direct byte to direct byte	3	2	85
MOV direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV direct,#data	Move immediate data to direct byte	3	2	75
MOV @Ri,A	Move A to indirect RAM	1	1	F6, F7
MOV @Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV @Ri,#data	Move immediate data to indirect RAM	2	1	76, 77
MOV DPTR,#data 16	Load data pointer with a 16-bit constant	3	2	90
MOVC A,@A+DPTR	Move code byte relative to DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative to PC to A	1	2	83
MOVX A,@Ri	Move external RAM (8-bit address) to A	1	2	E2, E3
MOVX A,@DPTR	Move external RAM (16-bit address) to A	1	2	E0
MOVX @Ri,A	Move A to external RAM (8-bit address)	1	2	F2, F3
MOVX @DPTR,A	Move A to external RAM (16-bit address)	1	2	F0
PUSH direct	Push direct byte onto stack	2	2	C0
POP direct	Pop direct byte from stack	2	2	D0
XCH A,Rr	Exchange register with A	1	1	C*
XCH A,direct	Exchange direct byte with A	2	1	C5
XCH A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD A,@Ri	Exchange LOW-order nibble indirect RAM with A	1	1	D6, D7

** MOV A,ACC is not permitted.

mnemonic		description	bytes/ cycles		opcode (hex.)
Boolean variable manipulation					
CLR	C	Clear carry flag	1	1	C3
CLR	bit	Clear direct bit	2	1	C2
SETB	C	Set carry flag	1	1	D3
SETB	bit	Set direct bit	2	1	D2
CPL	C	Complement carry flag	1	1	B3
CPL	bit	Complement direct bit	2	1	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C,bit	OR direct bit to carry flag	2	2	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C,bit	Move direct bit to carry flag	2	1	A2
MOV	bit,C	Move carry flag to direct bit	2	2	92
Program and machine control					
ACALL	addr11	Absolute subroutine call	2	2	●1addr
LCALL	addr16	Long subroutine call	3	2	12
RET		Return from subroutine	1	2	22
RETI		Return from interrupt	1	2	32
AJMP	addr11	Absolute jump	2	2	▲1addr
LJMP	addr16	Long jump	3	2	02
SJMP	rel	Short jump (relative address)	2	2	80
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2	73
JZ	rel	Jump if A is zero	2	2	60
JNZ	rel	Jump if A is not zero	2	2	70
JC	rel	Jump if carry flag is set	2	2	40
JNC	rel	Jump if carry flag is not set	2	2	50
JB	bit,rel	Jump if direct bit is set	3	2	20
JNB	bit,rel	Jump if direct bit is not set	3	2	30
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2	10
CJNE	A,direct,rel	Compare direct to A and jump if not equal	3	2	B5
CJNE	A,#data,rel	Compare immediate to A and jump if not equal	3	2	B4
CJNE	Rr,#data,rel	Compare immed. to reg. and jump if not equal	3	2	B*
CJNE	@Ri,#data,rel	Compare immed. to ind. and jump if not equal	3	2	B6, B7
DJNZ	Rr,rel	Decrement register and jump if not zero	2	2	D*
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2	D5
NOP		No operation	1	1	00

Notes to Table 4

Data addressing modes

Rr	Working register R0-R7.
direct	128 internal RAM locations and any special function register (SFR).
@Ri	Indirect internal RAM location addressed by register R0 or R1 of the actual register bank.
#data	8-bit constant included in instruction.
#data16	16-bit constant included as bytes 2 and 3 of instruction.
bit	direct addressed bit in internal RAM or SFR.
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 K-byte program memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 K-byte page of program memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is −128 to + 127 bytes relative to first byte of the following instruction.

Hexadecimal opcode cross-reference to Table 5

* : 8, 9, A, B, C, D, E, F.
● : 11, 31, 51, 71, 91, B1, D1, F1.
▲ : 01, 21, 41, 61, 81, A1, C1, E1.

Table 5 Instruction map

first hexadecimal chacter of opcode ↓ | second hexadecimal character of opcode →

	0	1	2	3	4	5	6 | 7	8 | 9 | A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC dir	INC @Ri 0 | 1	INC Rr 0 | 1 | 2	3	4	5	6	7
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC dir	DEC @Ri 0 | 1	DEC Rr 0 | 1 | 2	3	4	5	6	7
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,dir	ADD A,@Ri 0 | 1	ADD A,Rr 0 | 1 | 2	3	4	5	6	7
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,dir	ADDC A,@Ri 0 | 1	ADDC A,Rr 0 | 1 | 2	3	4	5	6	7
4	JC rel	AJMP addr11	ORL dir,A	ORL dir,#data	ORL A,#data	ORL A,dir	ORL A,@Ri 0 | 1	ORL A,Rr 0 | 1 | 2	3	4	5	6	7
5	JNC rel	ACALL addr11	ANL dir,A	ANL dir,#data	ANL A,#data	ANL A,dir	ANL A,@Ri 0 | 1	ANL A,Rr 0 | 1 | 2	3	4	5	6	7
6	JZ rel	AJMP addr11	XRL dir,A	XRL dir,#data	XRL A,#data	XRL A,dir	XRL A,@Ri 0 | 1	XRL A,Rr 0 | 1 | 2	3	4	5	6	7
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV dir,#data	MOV @Ri,#data 0 | 1	MOV Rr,#data 0 | 1 | 2	3	4	5	6	7
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV dir,dir	MOV dir,@Ri 0 | 1	MOV dir,Rr 0 | 1 | 2	3	4	5	6	7
9	MOV DPTR, #data	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,dir	SUBB A,@Ri 0 | 1	SUBB A,Rr 0 | 1 | 2	3	4	5	6	7
A	ORL C,/bit	AJMP addr11	MOV C,bit	INC DPTR	MUL AB		MOV @Ri,dir 0 | 1	MOV Rr,dir 0 | 1 | 2	3	4	5	6	7
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A, #data,rel	CJNE A,dir,rel	CJNE @Ri,#data,rel 0 | 1	CJNE Rr,#data,rel 0 | 1 | 2	3	4	5	6	7
C	PUSH dir	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,dir	XCH A,@Ri 0 | 1	XCH A,Rr 0 | 1 | 2	3	4	5	6	7
D	POP dir	ACALL addr11	SETB bit	SETB C	DA A	DJNZ dir,rel	XCHD A,@Ri 0 | 1	DJNZ Rr,rel 0 | 1 | 2	3	4	5	6	7
E	MOVX A,@DPTR	AJMP addr11	MOVX A,@Ri 0 | 1		CLR A	MOV * A,dir	MOV A,@Ri 0 | 1	MOV A,Rr 0 | 1 | 2	3	4	5	6	7
F	MOVX @DPTR,A	ACALL addr11	MOVX @Ri,A 0 | 1		CPL A	MOV dir,A	MOV @Ri,A 0 | 1	MOV Rr,A 0 | 1 | 2	3	4	5	6	7

* MOV A,ACC is not a valid instruction.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Input voltage on any pin with respect to ground (V_{SS})	V_I	−0,5	+ 6,5	V
Input, output current	I_I, I_O	−	± 5,0	mA
Input, output current on any single pin	I_I, I_O	−	± 10	mA
Total power dissipation	P_{tot}	−	1,0	W
Storage temperature range	T_{stg}	−65	+ 150	°C
Operating ambient temperature range				
PCB83C654	T_{amb}	0	+ 70	°C
PCF83C654	T_{amb}	−40	+ 85	°C
PCA83C654	T_{amb}	−40	+ 125	°C

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 5 V (± 10%); V_{SS} = 0 V; T_{amb} = 0 to 70 °C (PCB83C654), −40 to + 85 °C (PCF83C654).
All voltages measured with respect to V_{SS} unless otherwise specified.

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_{DD}	4,5	5,5	V
Supply current operating	(note 1) f_{CLK} = 12 MHz; V_{DD} = 5,5 V	I_{DD}	−	tbf	mA
Idle mode	(note 2) f_{CLK} = 12 MHz; V_{DD} = 5 V ± 10%	I_{ID}	−	tbf	mA
Power-down current	2 V < V_{PD} < V_{DD} max. (note 3)	I_{PD}	−	tbf	μA
Inputs					
LOW level input voltage (except $\overline{EA}$, P1.6/SCL, P1.7/SDA)		V_{IL}	−0,5	$0{,}2V_{DD}-0{,}1$	V
LOW level input voltage ($\overline{EA}$)		V_{IL1}	−0,5	$0{,}2V_{DD}-0{,}3$	V
LOW level input voltage (P1.6/SCL, P1.7/SDA)	(note 6)	V_{IL2}	−0,5	$0{,}3V_{DD}$	V
HIGH level input voltage (except RST, XTAL1, P1.6/SCL, P1.7/SDA)		V_{IH}	$0{,}2V_{DD}+0{,}9$	$V_{DD}+0{,}5$	V
HIGH level input voltage (RST and XTAL1)		V_{IH1}	$0{,}7V_{DD}$	$V_{DD}+0{,}5$	V

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	max.	unit
Outputs					
HIGH level input voltage (P1.6/SCL, P1.7/SDA)	(note 6)	V_{IH2}	$0{,}7V_{DD}$	6,0	V
Input current logic 0 (Ports 1, 2 and 3; except P1.6/SDA, P1.7/SCL)	V_I = 0,45 V	$-I_{IL}$	–	50	μA
Input current logic 1 to 0 transition (Ports 1, 2, 3; except P1.6/SCL, P1.7/SDA)	V_I = 2,0 V	$-I_{TL}$	–	650	μA
Input leakage current (Port 0, $\overline{EA}$)	V_I = 0,45 V	$\pm I_{LI1}$	–	10	μA
Input leakage current (P1.6/SCL, P1.7/SDA)	$0 V < V_I < 6{,}0$ V $0 V < V_{DD} < 5{,}5$ V	$\pm I_{LI2}$	–	10	μA
LOW level output voltage (Ports 1, 2 and 3; except P1.6/SCL, P1.7/SDA)	(note 4) I_{OL} = 1,6 mA	V_{OL}	–	0,45	V
LOW level output voltage (Port 0, ALE, $\overline{PSEN}$)	(note 4) I_{OL} = 3,2 mA	V_{OL1}	–	0,45	V
LOW level output voltage (P1.6/SCL, P1.7/SDA)	I_{OL} = 3,0 mA	V_{OL2}	–	0,40	V
HIGH level output voltage (Ports 1, 2 and 3)	V_{DD} = 5 V ± 10% $-I_{OH}$ = 60 μA $-I_{OH}$ = 25 μA $-I_{OH}$ = 10 μA	V_{OH} V_{OH} V_{OH}	2,4 $0{,}75V_{DD}$ $0{,}9V_{DD}$	– – –	V V V
HIGH level output voltage (Port 0 in external bus mode, ALE, $\overline{PSEN}$)	(note 5) V_{DD} = 5 V ± 10% $-I_{OH}$ = 400 μA $-I_{OH}$ = 150 μA $-I_{OH}$ = 40 μA	V_{OH1} V_{OH1} V_{OH1}	2,4 $0{,}75V_{DD}$ $0{,}9V_{DD}$	– – –	V V V
RST pull-down resistor		R_{RST}	50	150	kΩ
Capacitance of I/O buffer	Test freq. = 1 MHz T_{amb} = 25 °C	$C_{I/O}$	–	10	pF

DC CHARACTERISTICS

AV_{DD} = 5,0 V ± 10%; AV_{SS} = 0 V; V_{REF} = 5,0 V; T_{amb} = −40 °C to + 125 °C (PCA83C654).
All voltages measured with respect to V_{SS} unless otherwise specified.

parameter	conditions	symbol	min.	max.	unit
Supply voltage		V_{DD}	4,5	5,5	V
Supply current operating	(note 1) f_{CLK} = 12 MHz; V_{DD} = 5,5 V	I_{DD}	–	tbf	mA
Idle mode	(note 2) f_{CLK} = 12 MHz; V_{DD} = 5 V ± 10%	I_{ID}	–	tbf	mA
Power-down current	2 V < V_{PD} < V_{DD} max. (note 3)	I_{PD}	–	tbf	μA
Inputs					
LOW level input voltage (except $\overline{EA}$, P1.6/SCL, P1.7/SDA)		V_{IL}	−0,5	$0,2V_{DD}-0,25$	V
LOW level input voltage ($\overline{EA}$)		V_{IL1}	−0,5	$0,2V_{DD}-0,45$	V
LOW level input voltage (P1.6/SCL, P1.7/SDA)	(note 6)	V_{IL2}	−0,5	$0,3V_{DD}$	V
HIGH level input voltage (except RST, XTAL1, P1.6/SCL, P1.7/SDA)		V_{IH}	$0,2V_{DD}+1,0$	$V_{DD}+0,5$	V
HIGH level input voltage (RST and XTAL1)		V_{IH1}	$0,7V_{DD}+0,1$	$V_{DD}+0,5$	V
HIGH level input voltage (P1.6/SCL, P1.7/SDA)	(note 6)	V_{IH2}	$0,7V_{DD}$	6,0	V
Input current logic 0 (Ports 1, 2 and 3; except P1.6/SDA, P1.7/SCL)	V_I = 2,0 V	$-I_{IL}$	–	75	μA
Input current logic 1 to 0 transition (Ports 1, 2 and 3; except P1.6/SCL, P1.7/SDA)	V_I = 2,0 V	$-I_{TL}$	–	750	μA
Input leakage current (Port 0, $\overline{EA}$)	0,45 < V_I < V_{DD}	$\pm I_{LI1}$	–	10	μA
Input leakage current (P1.6/SCL, P1.7/SDA)	0 V < V_I < 6,0 V 0 V < V_{DD} < 5,5 V	$\pm I_{LI2}$	–	10	μA

DC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	max.	unit
Outputs					
LOW level output voltage (Ports 1, 2 and 3; except P1.6/SCL, P1.7/SDA)	(note 4) I_{OL} = 1,6 mA	V_{OL}	–	0,45	V
LOW level output voltage (Port 0, ALE, $\overline{PSEN}$)	(note 4) I_{OL} = 3,2 mA	V_{OL1}	–	0,45	V
LOW level output voltage (P1.6/SCL, P1.7/SDA)	I_{OL} = 3,0 mA	V_{OL2}	–	0,40	V
HIGH level output voltage (Ports 1, 2 and 3)	V_{DD} = 5 V ± 10%				
	$-I_{OH}$ = 60 μA	V_{OH}	2,4	–	V
	$-I_{OH}$ = 25 μA	V_{OH}	$0,75V_{DD}$	–	V
	$-I_{OH}$ = 10 μA	V_{OH}	$0,9V_{DD}$	–	V
HIGH level output voltage (Port 0 in external bus mode, ALE, $\overline{PSEN}$)	(note 5) V_{DD} = 5 V ± 10%				
	$-I_{OH}$ = 400 μA	V_{OH1}	2,4	–	V
	$-I_{OH}$ = 150 μA	V_{OH1}	$0,75V_{DD}$	–	V
	$-I_{OH}$ = 40 μA	V_{OH1}	$0,9V_{DD}$	–	V
RST pull-down resistor		R_{RST}	50	150	kΩ
Capacitance of I/O buffer	Test freq. = 1 MHz T_{amb} = 25 °C	$C_{I/O}$	–	10	pF

Notes to the DC characteristics

1. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$ + 0,5 V; $V_{IH} = V_{DD}$ −0,5 V; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = V_{DD}.
2. The Idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 10 ns; $V_{IL} = V_{SS}$ + 0,5 V; $V_{IH} = V_{DD}$ −0,5 V; XTAL2 not connected; $\overline{EA}$ = Port 0 = V_{DD}; RST = V_{SS}.
3. The power-down current is measured with all output pins disconnected; XTAL2 not connected; $\overline{EA}$ = Port 0 = V_{DD}; RST = V_{SS}.
4. Capacitive loading on Port 0 and Port 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1 and Port 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make a 1-to-0 transition during bus operations. In the most adverse condition (capacitive loading > 100 pF) the noise pulse on ALE line may exceed 0,8 V. In this event it may be required to qualify ALE with a Schmitt trigger, or use an address latch with a Schmitt trigger STROBE input.

5. Capacitive loading on Port 0 and Port 2 may cause the HIGH level output voltage on ALE and $\overline{PSEN}$ to momentarily fall below the 0,9 V_{DD} specification when the address bits are stabilizing.
6. The input threshold voltage of P1.6 and P1.7 (SI01) meets the I^2C-bus specification. A voltage below 0,3 V_{DD} will therefore be recognised as a logic 0, while an input voltage above 0,7 V_{DD} will be recognised as a logic 1.

AC CHARACTERISTICS

V_{DD} = 5 V ± 20% (PCB83C654), V_{SS} = 0 V, $t_{CKmin} = 1/f_{max}$ (maximum operating frequency)

V_{DD} = 5 V ± 20% (PCF83C654), V_{SS} = 0 V, $t_{CKmin} = 1/f_{max}$ (maximum operating frequency)

V_{DD} = 5 V ± 10% (PCA83C654), V_{SS} = 0 V, $t_{CKmin} = 1/f_{max}$ (maximum operating frequency)

T_{amb} = 0 to + 70 °C, t_{CKmin} = 83 ns (PCB83C654 see notes 1 and 2)

T_{amb} = −40 to + 85 °C, t_{CKmin} = 83 ns (PCF83C654 see notes 1 and 2)

T_{amb} = −40 to + 125 °C, t_{CKmin} = 83 ns (PCA83C654 see notes 1 and 2)

C_L = 100 pF for Port 0, ALE and $\overline{PSEN}$; C_L = 80 pF for all other outputs unless otherwise specified. (See waveforms Figs 16, 17 and 18).

DEVELOPMENT DATA

parameter	symbol	10 MHz		12 MHz		variable clock		unit
		min.	max.	min.	max.	min.	max.	
Program memory								
ALE pulse duration	t_{LL}	160	–	127	–	$2t_{CK}-40$	–	ns
Address set-up time to ALE	t_{AL}	45	–	28	–	$t_{CK}-55$	–	ns
Address hold time after ALE	t_{LA}	65	–	48	–	$t_{CK}-35$	–	ns
Time from ALE to valid instruction input	t_{LIV}	–	300	–	233	–	$4t_{CK}-100$	ns
Time from ALE to control pulse $\overline{PSEN}$	t_{LC}	60	–	43	–	$t_{CK}-40$	–	ns
Control pulse duration $\overline{PSEN}$	t_{CC}	255	–	205	–	$3t_{CK}-45$	–	ns
Time from $\overline{PSEN}$ to valid instruction input	t_{CIV}	–	195	–	145	–	$3t_{CK}-105$	ns
Input instruction hold time after $\overline{PSEN}$	t_{CI}	0	–	0	–	0	–	ns
Input instruction float delay after $\overline{PSEN}$	t_{CIF}	–	75	–	59	–	$t_{CK}-25$	ns
Address to valid instruction input	t_{AIV}	–	395	–	312	–	$5t_{CK}-105$	ns
Address float delay after $\overline{PSEN}$	t_{AFC}	–	10	–	10	–	10	ns

AC CHARACTERISTICS

parameter	symbol	10 MHz		12 MHz		variable clock		unit
		min.	max.	min.	max.	min.	max.	
External data memory								
$\overline{RD}$ pulse duration	t_{RR}	500	–	400	–	$6t_{CK}-100$	–	ns
$\overline{WR}$ pulse duration	t_{WW}	500	–	400	–	$6t_{CK}-100$	–	ns
Address hold time after ALE	t_{LA}	–	–	48	–	$t_{CK}-35$	–	ns
$\overline{RD}$ to valid data input	t_{RD}	–	355	–	252	–	$5t_{CK}-165$	ns
Data hold time after $\overline{RD}$	t_{DR}	0	–	0	–	0	–	ns
Data float delay after $\overline{RD}$	t_{DFR}	–	130	–	97	–	$2t_{CK}-70$	ns
Time from ALE to valid data input	t_{LD}	–	650	–	517	–	$8t_{CK}-150$	ns
Address to valid data input	t_{AD}	–	735	–	585	–	$9t_{CK}-165$	ns
Time from ALE to $\overline{RD}$ or $\overline{WR}$	t_{LW}	250	350	200	300	$3t_{CK}-50$	$3t_{CK}+50$	ns
Time from address to $\overline{RD}$ or $\overline{WR}$	t_{AW}	270	–	203	–	$4t_{CK}-130$	–	ns
Time from $\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	t_{WHLH}	60	140	43	123	$t_{CK}-40$	$t_{CK}+40$	ns
Data valid to $\overline{WR}$ transition	t_{DWX}	40	–	23	–	$t_{CK}-60$	–	ns
Data set-up time before $\overline{WR}$	t_{DW}	550	–	433	–	$7t_{CK}-150$	–	ns
Data hold time after $\overline{WR}$	t_{WD}	50	–	33	–	$t_{CK}-50$	–	ns
Address float delay after $\overline{RD}$	t_{AFR}	–	0	–	0	–	0	ns

Notes to AC characteristics:

1. The maximum and minimum operating frequency for all versions is 12 MHz and 1,2 MHz respectively.
2. The minimum operating frequency is limited to 1,2 MHz for all versions.
3. Interfacing the PCB83C654 to devices with float times up to 75 ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.

AC CHARACTERISTICS (continued)

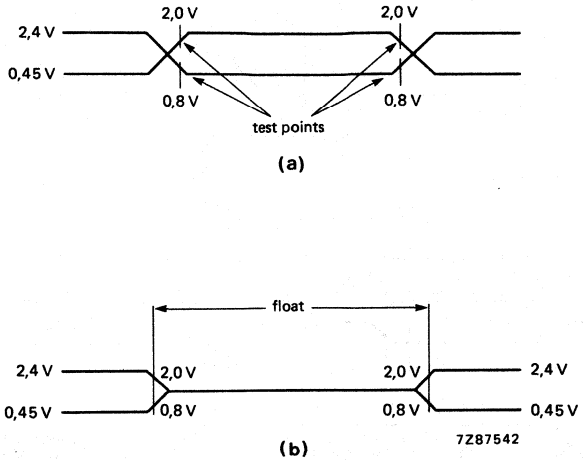


Fig. 14 AC testing input, output waveform (a) and float waveform (b).

AC testing inputs are driven at 2,4 V for a logic 1 and 0,45 V for a logic 0. Timing measurements are taken at 2,0 V for a logic 1 and 0,8 V for logic 0. The float state is defined as the point at which a Port 0 pin sinks 3,2 mA or sources 400 μA at the voltage test levels.

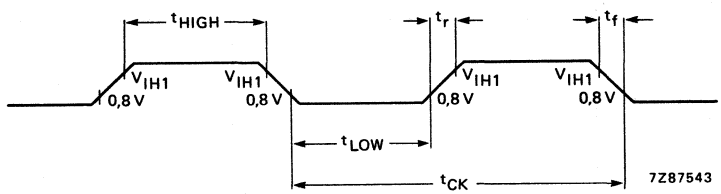


Fig. 15 External clock drive XTAL 1 (see Table 6).

Table 6 External clock drive XTAL 1 (see Fig. 15)

parameter	symbol	variable clock (f = 1,2 to 12 MHz)		unit
		min.	max.	
oscillator clock period	t_{CK}	83,3	833	ns
HIGH time	t_{HIGH}	20	$t_{CK}-t_{LOW}$	ns
LOW time	t_{LOW}	20	$t_{CK}-t_{HIGH}$	ns
rise time	t_r	–	20	ns
fall time	t_f	–	20	ns
cycle time	t_{CY} (1)	1	3,43	μs

(1) $t_{CY} = 12\ t_{CK}$.

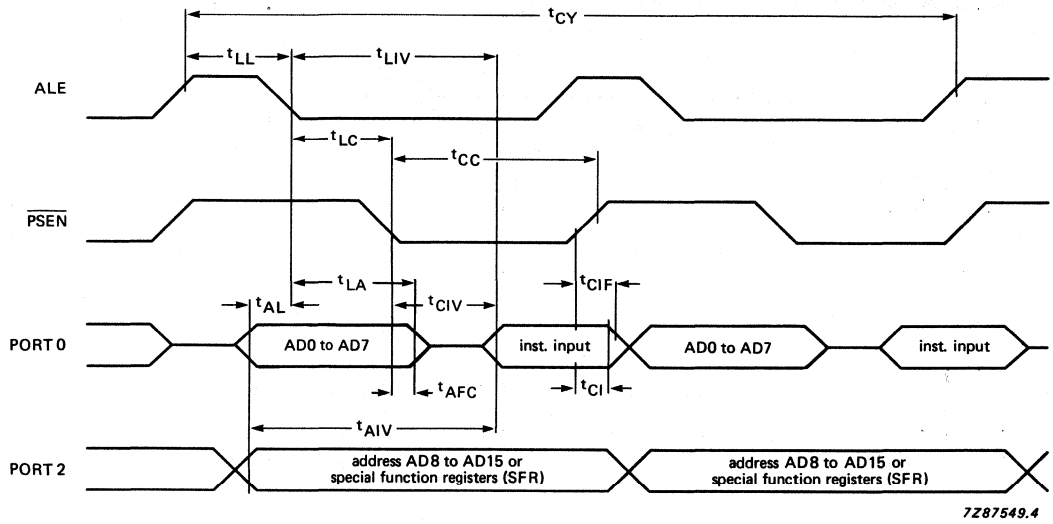


Fig. 16 Read from program memory.

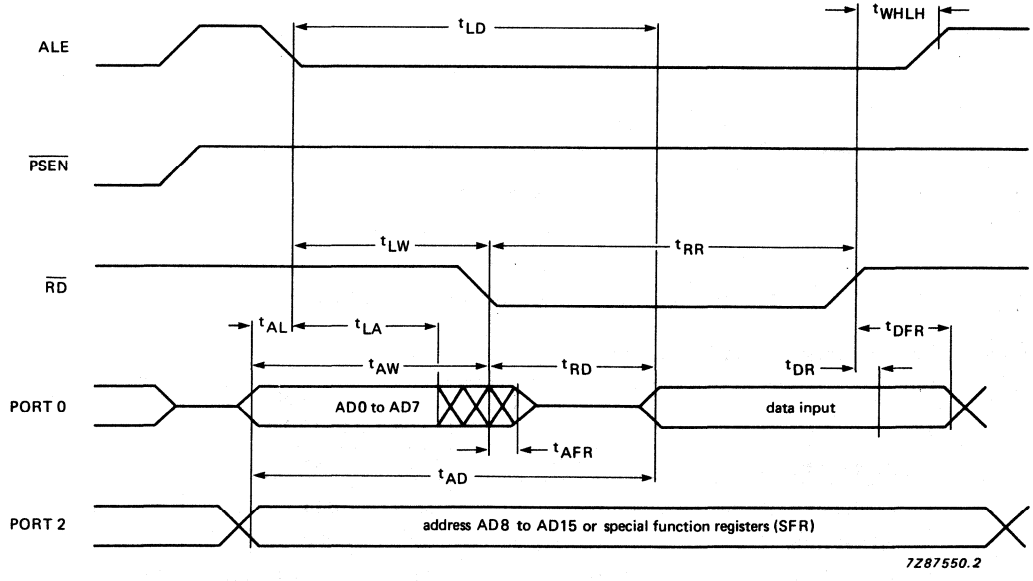


Fig. 17 Read from data memory.

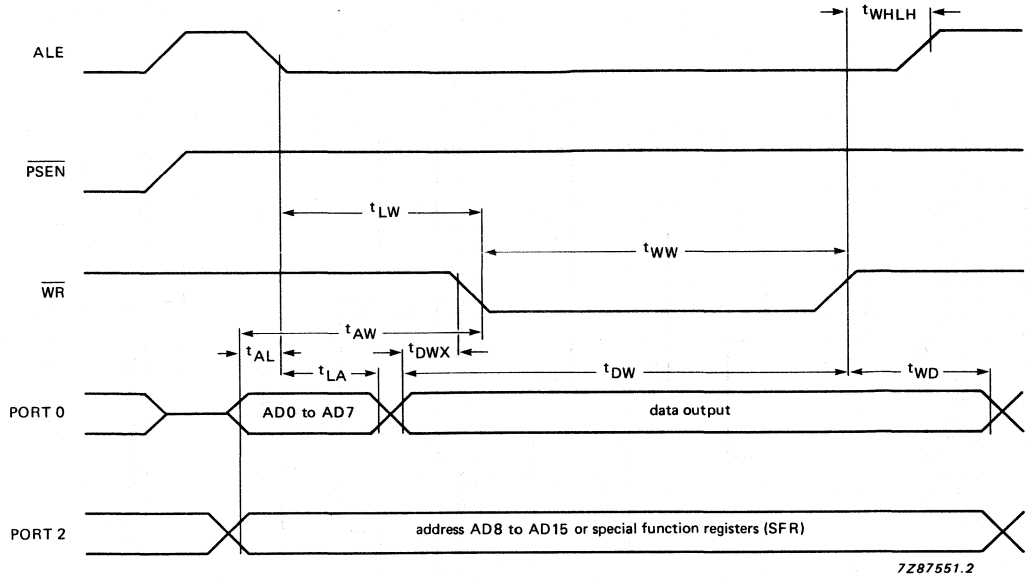
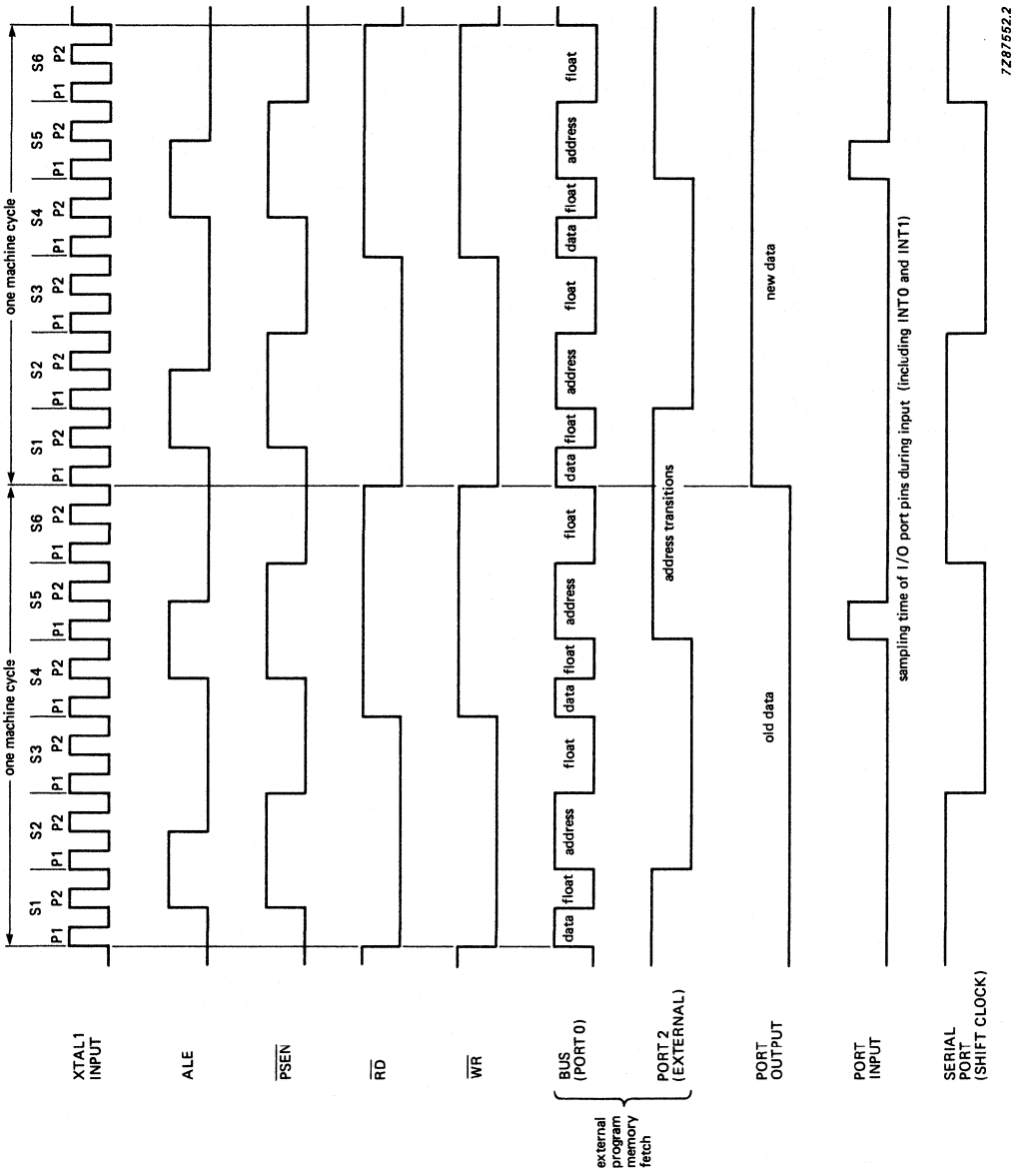


Fig. 18 Write to data memory.

DEVELOPMENT DATA


one machine cycle
one machine cycle
S1 P1 P2 S2 P1 P2 S3 P1 P2 S4 P1 P2 S5 P1 P2 S6 P1 P2
XTAL1 INPUT
ALE
PSEN
RD
WR
BUS (PORT 0)
PORT 2 (EXTERNAL)
PORT OUTPUT
PORT INPUT
SERIAL PORT (SHIFT CLOCK)
data float address float data float address float data float address float
address transitions
old data
new data
sampling time of I/O port pins during input (including INT0 and INT1)
external program memory fetch
7Z87552.2

DTMF / SINGLE -TONE GENERATOR

GENERAL DESCRIPTION

The PCD3311A is a single-chip silicon gate CMOS integrated circuit. It is intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialling systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3,58 MHz quartz crystal-controlled oscillator.

The device can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I^2C bus).

With its on-chip voltage reference the PCD3311A provides constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT CS 203 recommendations.

In addition to the standard DTMF frequencies the device provides 32 single frequencies.

Features

- Stabilized output voltage level
- Low output distortion with on-chip filtering (CEPT CS 203 compatible)
- Latched inputs for data bus applications
- I^2C bus compatible
- Mode select input (selection of parallel or serial data input)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current	I_{DD}	–	–	0,9	mA
Static standby current	I_{DDO}	–	–	3	μA
DTMF output voltage level (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion	THD	–	–25	–	dB
Operating ambient temperature range	T_{amb}	–25	–	+70	°C

PACKAGE OUTLINE

PCD3311AT: 16-lead mini-pack; plastic (SO16L; SOT162A).

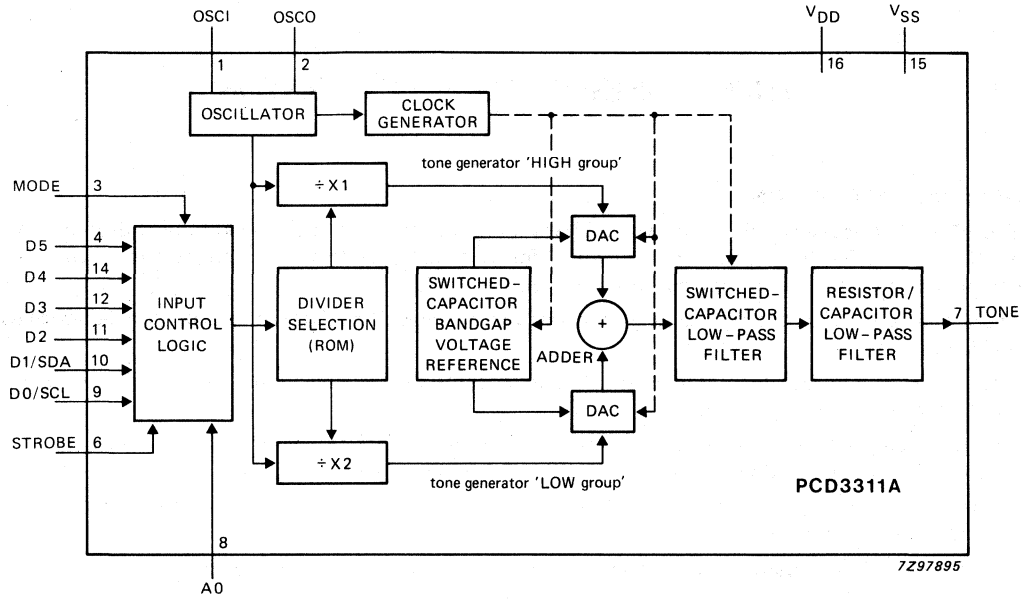


Fig. 1 Block diagram.

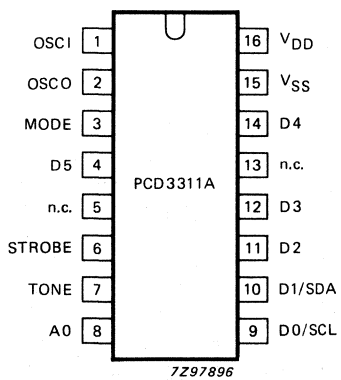


Fig. 2 Pinning diagram.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D5	parallel data input*
6	STROBE	strobe input; used for the loading of data in the parallel mode
7	TONE	frequency output for single or dual tones
8	A0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
9	D0/SCL	parallel data input* or serial clock line (I^2C bus)
10	D1/SDA	parallel data input* or serial data line (I^2C bus)
11	D2	parallel data inputs*
12	D3	parallel data inputs*
14	D4	parallel data inputs*
15	V_{SS}	negative supply
16	V_{DD}	positive supply
5;13	n.c.	not connected

* MODE = HIGH.

FUNCTIONAL DESCRIPTION

Clock/oscillator (OSCI and OSCO)

The timebase for the PCD3311A is a crystal-controlled oscillator with a 3,58 MHz quartz crystal connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock.

Mode select (MODE)

This input selects the data input mode. When connected to V_{DD}, data can be received in the parallel mode or, when connected to V_{SS} or left open, data can be received via the serial I^2C bus.

Parallel mode can only be obtained by setting MODE input HIGH.

Data inputs (D0, D1, D2, D3, D4 and D5)

Inputs D0 and D1 have no internal pulll-down or pull-up resistors and must not be left open in any application. Inputs D2 to D5 have internal pull-down.

Tables 1, 2 and 3 show all input codes and their corresponding output frequencies.

Strobe input (STROBE)

This input (with internal pull-down) allows the loading of parallel data into D0 to D5 when MODE is HIGH.

The data inputs must be stable preceeding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received.

Serial mode can only be obtained by setting MODE input LOW.

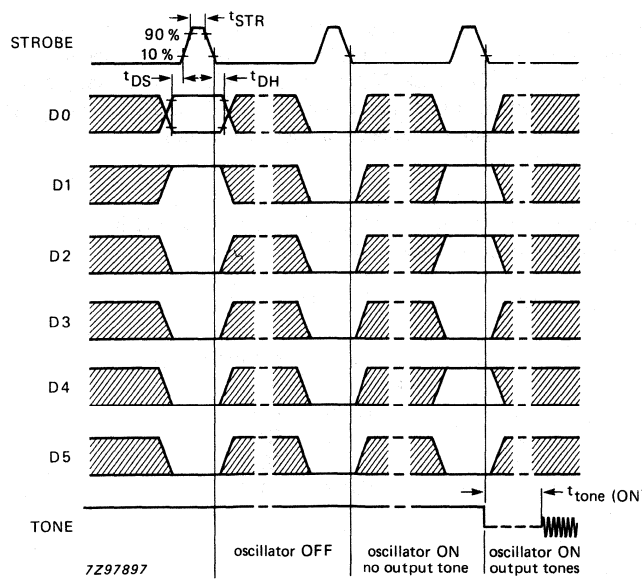


Fig. 3 Timing diagram showing control possibilities of the oscillator and the TONE output (e.g. 770 Hz + 1477 Hz) in the parallel mode (MODE = HIGH).

FUNCTIONAL DESCRIPTION (continued)

Serial clock and data inputs (SCL and SDA)

SCL and SDA are combined with D0 and D1 respectively. For the PCD3311A the selection of SCL and SDA is controlled by the MODE input. SCL and SDA are serial clock and data lines according to the I²C bus specification (see "CHARACTERISTICS OF THE I²C BUS"). Both inputs must be pulled-up externally to V_{DD}.

Address input (A0)

A0 is the slave address input and it identifies the device when up to two PCD3311 devices are connected to the same I²C bus. However, A0 must be connected to V_{DD} or V_{SS}.

I²C bus data configuration (see Fig. 4)

The PCD3311 is always a slave receiver in the I²C bus configuration (R/$\overline{W}$ bit = 0).

The slave address consists of 7 bits in the serial mode where the least significant bit is selectable by hardware on input A0, and the other more significant bits are internally fixed. In the serial mode the same input codes are used as in the parallel mode (see Tables 1, 2 and 3). D6 and D7 are don't care (X) bits.

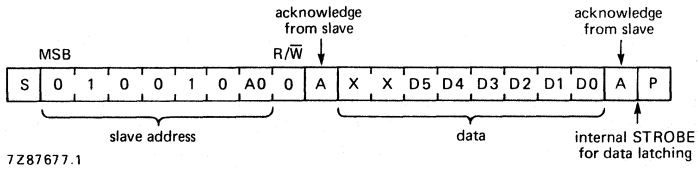


Fig. 4 I²C bus data format.

Tone output (TONE)

The single and the dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 2 shows the frequency tolerance of the output tones for DTMF signalling; Table 3 for the single tones.

Power-on reset

In order to avoid undefined states of the devices when the power is switched ON, an internal reset circuit sets them to the standby mode (oscillator OFF).

Table 1 Input data for control (no output tone; TONE at V_{DD})

D5	D4	D3	D2	D1	D0	HEX	oscillator
X	0	0	0	0	0	00/20	ON
X	0	0	0	0	1	01/21	OFF
X	0	0	0	1	0	02/22	OFF
X	0	0	0	1	1	03/23	OFF

Where:

1 = H = HIGH voltage level
0 = L = LOW voltage level
X = don't care.

Table 2 Input data for DTMF

D5	D4	D3	D2	D1	D0	HEX	symbol	standard frequency Hz	tone output freq. Hz*	frequency deviation %	frequency deviation Hz
0	0	1	0	0	0	08		697	697,90	+ 0,13	+ 0,90
0	0	1	0	0	1	09		770	770,46	+ 0,06	+ 0,46
0	0	1	0	1	0	0A		852	850,45	−0,18	−1,55
0	0	1	0	1	1	0B		941	943,23	+ 0,24	+ 2,23
0	0	1	1	0	0	0C		1209	1206,45	−0,21	−2,55
0	0	1	1	0	1	0D		1336	1341,66	+ 0,42	+ 5,66
0	0	1	1	1	0	0E		1477	1482,21	+ 0,35	+ 5,21
0	0	1	1	1	1	0F		1633	1638,24	+ 0,32	+ 5,24
0	1	0	0	0	0	10	0	941+1336			
0	1	0	0	0	1	11	1	697+1209			
0	1	0	0	1	0	12	2	697+1336			
0	1	0	0	1	1	13	3	697+1477			
0	1	0	1	0	0	14	4	770+1209			
0	1	0	1	0	1	15	5	770+1336			
0	1	0	1	1	0	16	6	770+1477			
0	1	0	1	1	1	17	7	852+1209			
0	1	1	0	0	0	18	8	852+1336			
0	1	1	0	0	1	19	9	852+1477			
0	1	1	0	1	0	1A	A	697+1633			
0	1	1	0	1	1	1B	B	770+1633			
0	1	1	1	0	0	1C	C	852+1633			
0	1	1	1	0	1	1D	D	941+1633			
0	1	1	1	1	0	1E	*	941+1209			
0	1	1	1	1	1	1F	#	941+1477			

Where:

1 = H = HIGH voltage level
0 = L = LOW voltage level

DEVELOPMENT DATA

* Tone output frequency when using a 3,579 545 MHz crystal.

FUNCTIONAL DESCRIPTION (continued)

Table 3 Input data for single frequencies

D5	D4	D3	D2	D1	D0	HEX	standard frequency (Hz)	tone output (Hz)*	frequency deviation	
									%	Hz
0	0	0	1	0	0	04	680	679,62	−0,06	−0,38
0	0	0	1	0	1	05	740	741,11	+0,15	+1,11
0	0	0	1	1	0	06	810	810,59	+0,07	+0,59
0	0	0	1	1	1	07	873	874,34	+0,15	+1,34
1	0	0	1	0	0	24	886	884,28	−0,20	−1,73
1	0	0	1	0	1	25	930	931,93	+0,21	+1,93
1	0	0	1	1	0	26	970	972,70	+0,28	+2,70
1	0	0	1	1	1	27	991	991,29	+0,03	+0,29
1	0	1	0	0	0	28	1055	1051,57	−0,33	−3,43
1	0	1	0	0	0	28	1060	1051,57	−0,80	−8,43
1	0	1	0	0	1	29	1124	1127,77	+0,34	+3,77
1	0	1	0	1	0	2A	1160	1161,44	+0,12	+1,44
1	0	1	0	1	1	2B	1197	1197,17	+0,01	+0,17
1	0	1	1	0	0	2C	1270	1275,68	+0,45	+5,68
1	0	1	1	0	0	2C	1275	1275,68	+0,05	+0,68
1	0	1	1	0	1	2D	1358	1353,33	−0,34	−4,68
1	0	1	1	1	0	2E	1400	1402,09	+0,15	+2,09
1	0	1	1	1	1	2F	1446	1441,04	−0,34	−4,96
1	1	0	0	0	0	30	1520	1525,81	+0,38	+5,81
1	1	0	0	0	0	30	1530	1525,81	−0,27	−4,19
1	1	0	0	0	1	31	1540	1540,92	+0,06	+0,92
1	1	0	0	1	0	32	1640	1638,24	−0,11	−1,76
1	1	0	0	1	1	33	1670	1673,47	+0,21	+3,47
1	1	0	1	0	0	34	1747	1748,68	+0,10	+1,68
1	1	0	1	0	1	35	1830	1830,97	+0,05	+0,97
1	1	0	1	1	0	36	1860	1852,77	−0,39	−7,23
1	1	0	1	1	1	37	1960	1970,03	+0,51	+10,03
1	1	0	1	1	1	37	1981	1970,03	−0,55	−10,97
1	1	1	0	0	0	38	2000	2021,20	+1,06	+21,20
1	1	1	0	0	1	39	2110	2103,14	−0,33	−6,86
1	1	1	0	1	0	3A	2200	2192,01	−0,36	−7,99
1	1	1	0	1	1	3B	2247	2255,54	+0,38	+8,54
1	1	1	1	0	0	3C	2280	2288,71	+0,38	+8,71
1	1	1	1	0	1	3D	2400	2394,34	−0,24	−5,66
1	1	1	1	1	0	3E	2600	2593,87	−0,24	−6,13
1	1	1	1	1	1	3F	2800	2779,15	−0,75	−20,85

Where:

1 = H = HIGH voltage level
0 = L = LOW voltage level

* Tone output frequency when using a 3,579545 MHz crystal.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

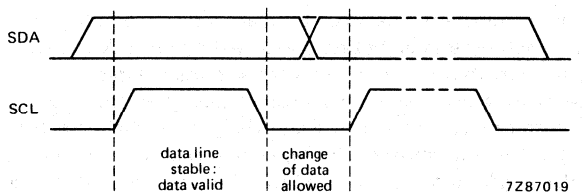


Fig. 5 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

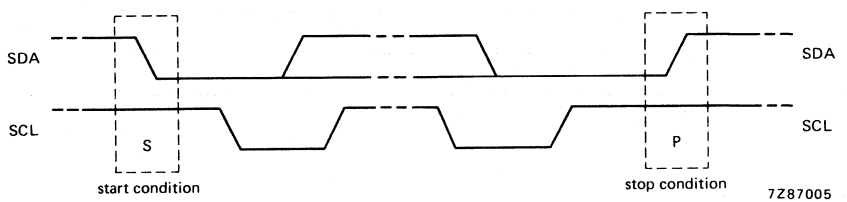


Fig. 6 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

CHARACTERISTICS OF THE I²C BUS (continued)

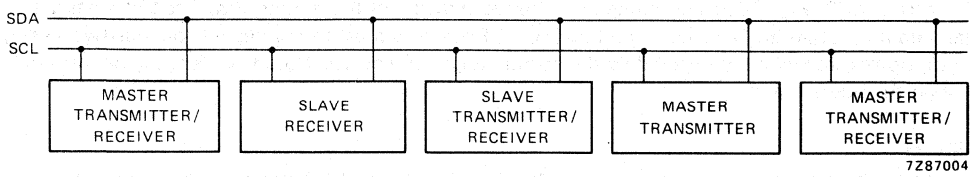


Fig. 7 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

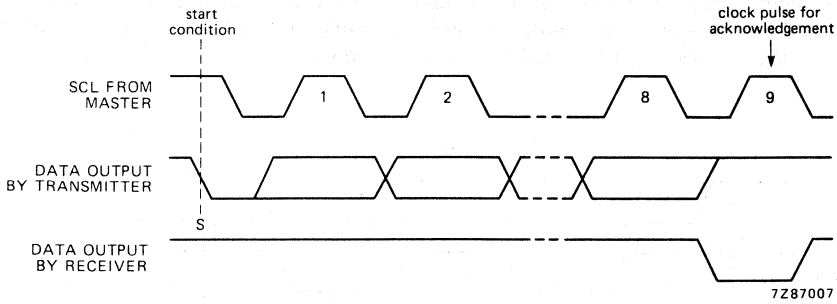


Fig. 8 Acknowledgement on the I²C bus.

DEVELOPMENT DATA

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The ICs operate in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 9.

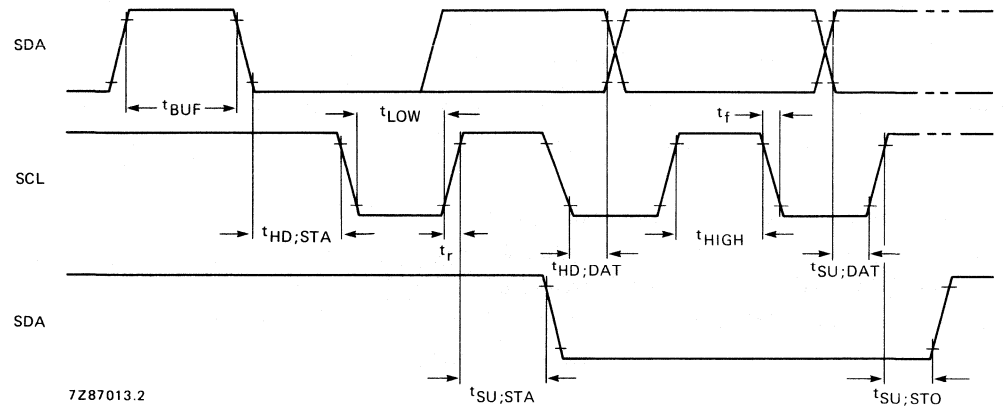


Fig. 9 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

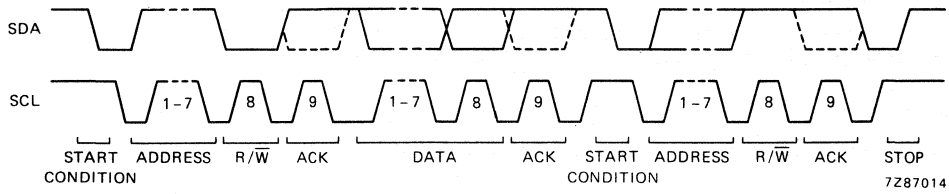


Fig. 10 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 11.

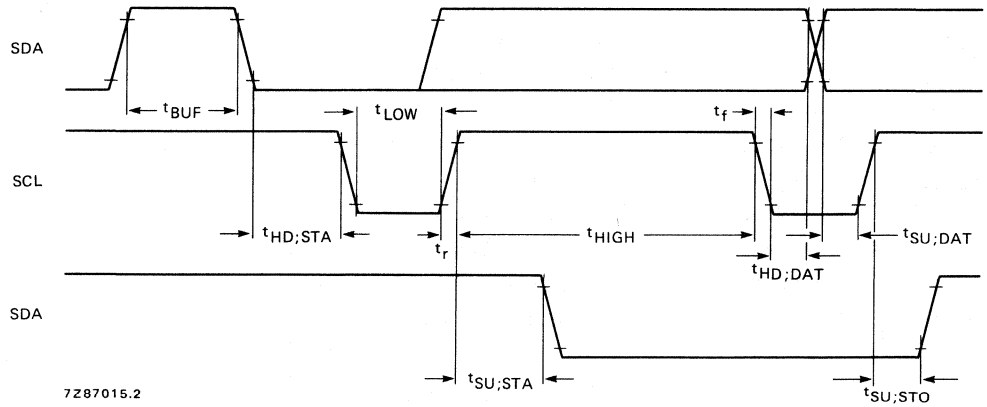


Fig. 11 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_r	$t \leqslant 1\ \mu s$
t_f	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

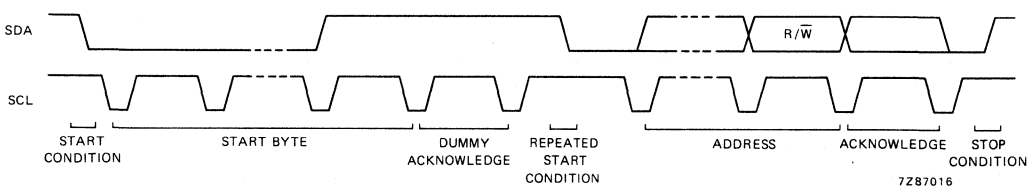


Fig. 12 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,8	+ 8,0	V
Input voltage range (any input)	V_I	−0,8	V_{DD}+0,8	V
DC input current (any input)	$\pm I_I$	–	10	mA
DC output current (any output)	$\pm I_O$	–	10	mA
Supply current	$\pm I_{DD}$; $\pm I_{SS}$	–	50	mA
Power dissipation per output	P_O	–	50	mW
Total power dissipation per package	P_{tot}	–	300	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579 545 MHz, R_{Smax} = 100 Ω; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current (note 1) oscillator ON; V_{DD} = 3 V					
no output tone	I_{DD}	–	50	100	μA
single output tone	I_{DD}	–	0,5	0,9	mA
dual output tone	I_{DD}	–	0,6	0,9	mA
Static standby current oscillator OFF; note 1	I_{DDO}	–	–	3	μA
Inputs/outputs (SDA)					
D0 to D5; MODE; STROBE					
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
D2 to D5; MODE; STROBE; A0					
Pull-down input current V_I = V_{DD}	$-I_{IL}$	30	150	300	nA
SCL (D0); SDA (D1)					
Output current LOW (SDA) V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Clock frequency (see Fig. 10)	f_{SCL}	–	–	100	kHz
Input capacitance; V_I = V_{SS}	C_I	–	–	7	pF
Allowable input spike pulse width	t_I	–	–	100	ns

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 13)					
DTMF output voltage levels (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
DC voltage level	V_{DC}	–	½ V_{DD}	–	V
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion T_{amb} = 25 °C					
dual tone; note 2	THD	–	−25	–	dB
modem tone, note 3	THD	–	−29	–	dB
Output impedance	$\|Z_O\|$	–	0,1	0,5	kΩ
OSCI input					
Maximum allowable amplitude at OSCI	$V_{OSC(p-p)}$	–	–	$V_{DD}-V_{SS}$	V
Timing (V_{DD} = 3 V)					
Oscillator start-up time	$t_{OSC(ON)}$	–	3	–	ms
TONE start-up time; note 4	$t_{TONE(ON)}$	–	0,5	–	ms
STROBE pulse width; note 5	t_{STR}	400	–	–	ns
Data set-up time; note 5	t_{DS}	150	–	–	ns
Data hold time; note 5	t_{DH}	100	–	–	ns

DEVELOPMENT DATA

Notes to the characteristics

1. Crystal is connected between OSCI and OSCO; D0/SCL and D1/SDA via a resistance of 5,6 kΩ to V_{DD}; all other pins left open.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Related to the level of the fundamental frequency.
4. Oscillator must be running.
5. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

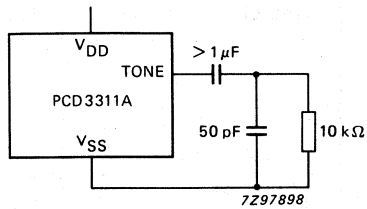


Fig. 13 TONE output test circuit.

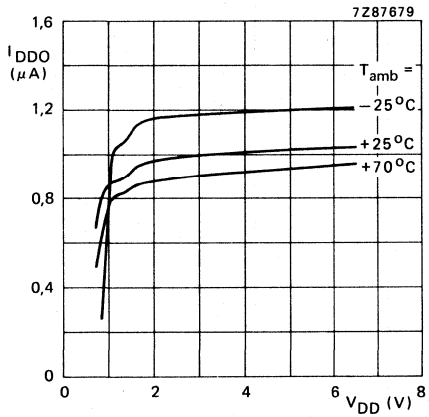


Fig. 14 Standby supply current as a function of supply voltage; oscillator OFF.

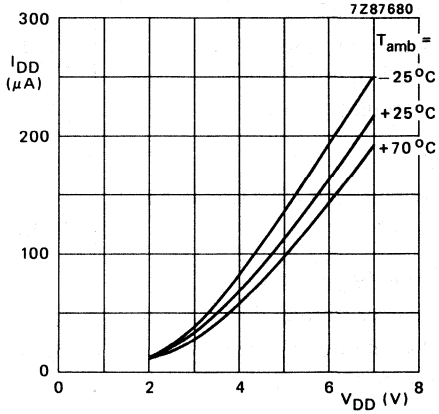


Fig. 15 Operating supply current as a function of supply voltage; oscillator ON; no output at TONE.

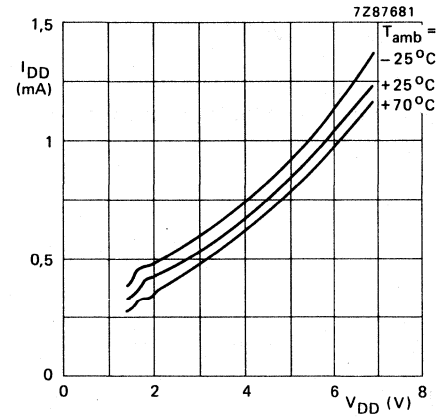


Fig. 16 Operating supply current as a function of supply voltage; oscillator ON; dual tone at TONE.

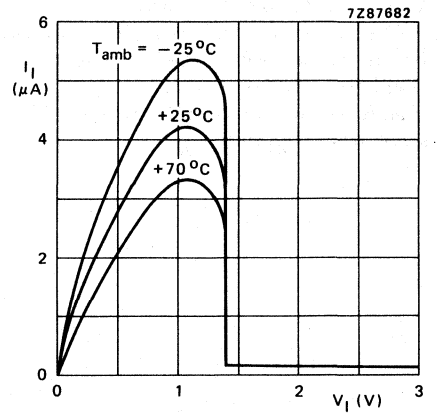


Fig. 17 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

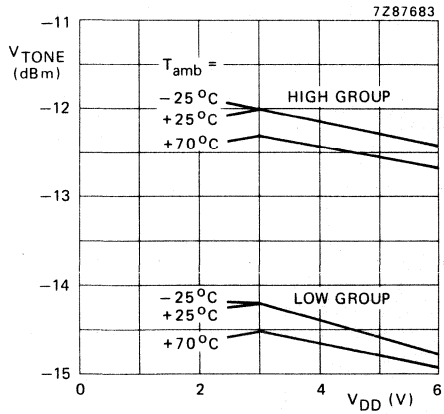


Fig. 18 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

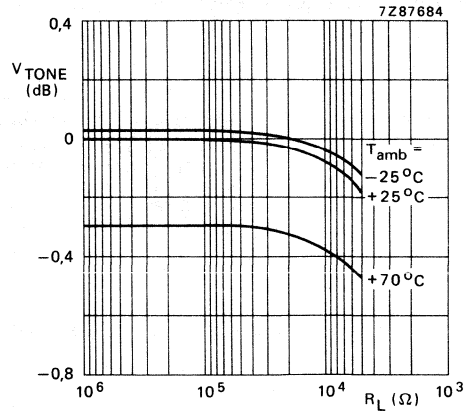
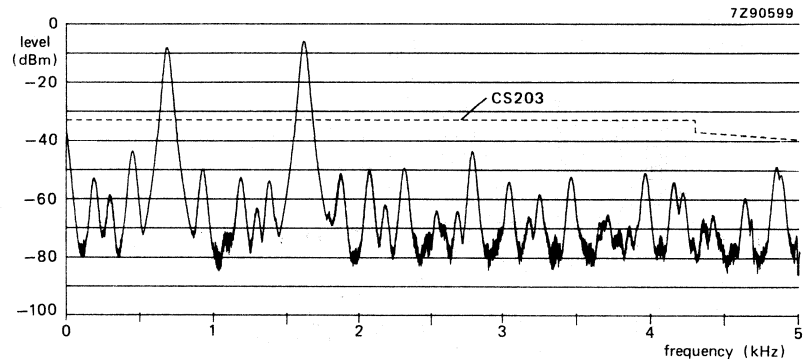


Fig. 19 Dual tone output voltage level as a function of output load resistance.

DEVELOPMENT DATA



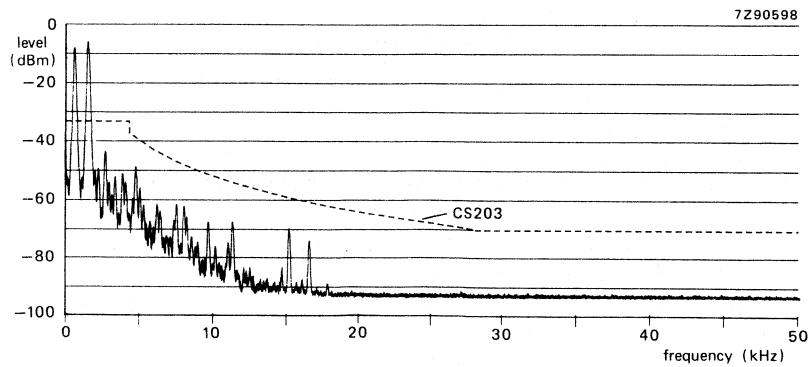


Fig. 20 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

APPLICATION INFORMATION

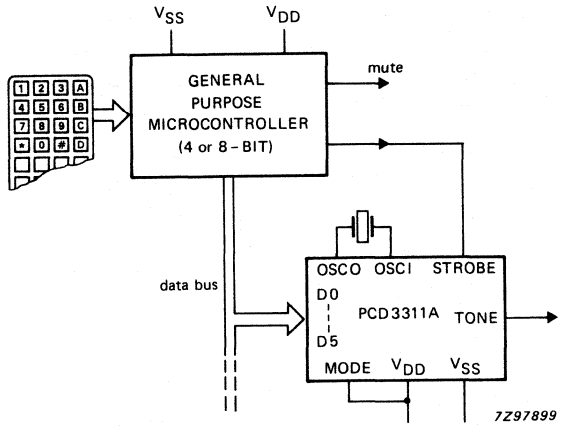


Fig. 21 PCD3311A driven by a microcontroller with parallel data-bus.

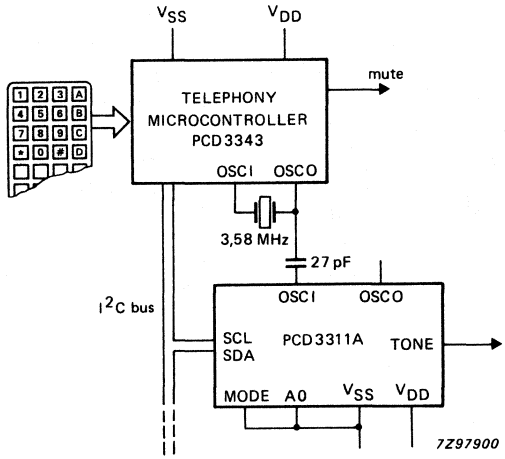


Fig. 22 PCD3311A driven by telephony microcontroller PCD3343 with serial I/O (I^2C bus).
The PCD3343 is a single-chip 8-bit microcontroller with 3K ROM/224 RAM bytes.

DTMF/MODEM/MUSICAL-TONE GENERATORS

GENERAL DESCRIPTION

The PCD3311 and PCD3312 are single-chip silicon gate CMOS integrated circuits. They are intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialling systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3,58 MHz quartz crystal-controlled oscillator.

The devices can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I^2C bus).

With their on-chip voltage reference the PCD3311 and PCD3312 provide constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT CS 203 recommendations.

In addition to the standard DTMF frequencies the devices provide 12 MODEM frequencies (300 to 1200 bits per second) used in simplex MODEM applications and two octaves of musical scale in steps of semitones.

Features

- Stabilized output voltage level
- Low output distortion with on-chip filtering (CEPT CS 203 compatible)
- Latched inputs for data bus applications
- I^2C bus compatible
- Mode select input (selection of parallel or serial data input)
- MODEM and melody tone generators

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current	I_{DD}	–	–	1,2	mA
Static standby current	I_{DDO}	–	–	3	μA
DTMF output voltage level (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion	THD	–	–25	–	dB
Operating ambient temperature range	T_{amb}	–25	–	+70	°C

PACKAGE OUTLINES

PCD3311P: 14-lead DIL; plastic (SOT27).
PCD3311T: 16-lead mini-pack; plastic (SO16L; SOT162A).
PCD3312P: 8-lead DIL; plastic (SOT97).
PCD3312T: 8-lead mini-pack; plastic (SO8L; SOT176A).

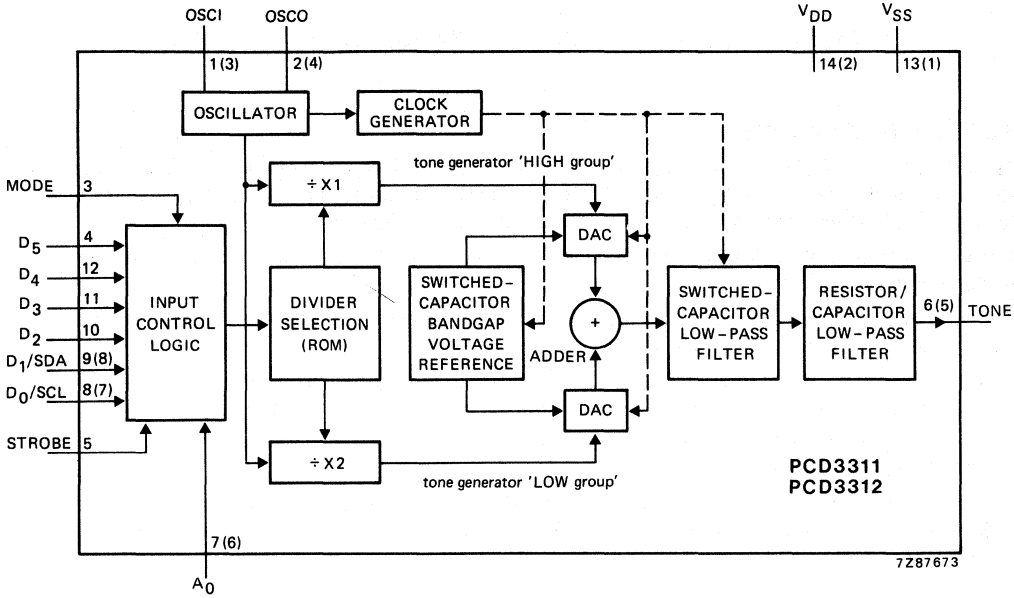


Fig. 1 Block diagram; the pin numbers in parenthesis refer to the PCD3312.

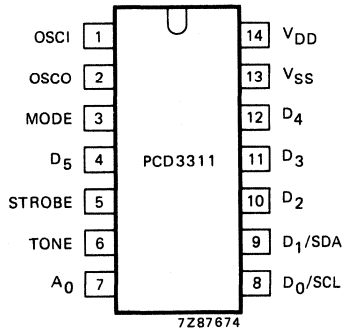


Fig. 2 Pinning diagram for the PCD3311.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D_5	parallel data input*
5	STROBE	strobe input; used for the loading of data in the parallel mode
6	TONE	frequency output for single or dual tones
7	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
8	D_0/SCL	parallel data input* or serial clock line (I^2C bus)
9	D_0/SDA	parallel data input* or serial data line (I^2C) bus)
10	D_2	parallel data inputs*
11	D_3	
12	D_4	
13	V_{SS}	negative supply
14	V_{DD}	positive supply

* MODE = HIGH.

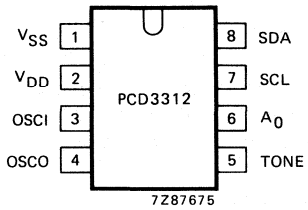


Fig. 3 Pinning diagram for the PCD3312.

PINNING

1	V_{SS}	negative supply
2	V_{DD}	positive supply
3	OSCI	oscillator input
4	OSCO	oscillator output
5	TONE	frequency output for single or dual tones
6	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
7	SCL	serial clock line (I^2C bus)
8	SDA	serial data line (I^2C bus)

FUNCTIONAL DESCRIPTION

Clock/oscillator (OSCI and OSCO)

The timebase for the PCD3311 and PCD3312 is a crystal-controlled oscillator with a 3,58 MHz quartz crystal connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock.

DEVELOPMENT DATA

Mode select (MODE)

This input selects the data input mode. When connected to V_{DD}, data can be received in the parallel mode (only for the PCD3311), or, when connected to V_{SS} or left open, data can be received via the serial I^2C bus (for both PCD3311 and PCD3312).

Parallel mode can only be obtained for the PCD3311 by setting MODE input HIGH.

Data inputs (D_0, D_1, D_2, D_3, D_4 and D_5)

Inputs D_0 and D_1 have no internal pull-down or pull-up resistors and must not be left open in any application. Inputs D_2 to D_5 have internal pull-down. D_5 and D_4 are used to select between DTMF dual, DTMF single, MODEM and melody tones (see Table 1). D_3 to D_0 select the combination of the tones for DTMF or single-tone itself.

Table 1 D_5 and D_4 in accordance with the selected application

D_5	D_4	application
0	0	DTMF single tones; standby; melody tones
0	1	DTMF dual tones (all 16 combinations)
1	0	MODEM tones; standby; melody tones
1	1	melody tones

1 = H = HIGH voltage level
0 = L = LOW voltage level

Note: Tables 2, 3, 4 and 5 show all input codes and their corresponding output frequencies.

FUNCTIONAL DESCRIPTION (continued)

Strobe input (STROBE, only for the PCD3311)

This input (with internal pull-down) allows the loading of parallel data into D_0 to D_5 when MODE is HIGH.

The data inputs must be stable preceeding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received.

Serial mode can only be obtained for the PCD3311 by setting MODE input LOW.

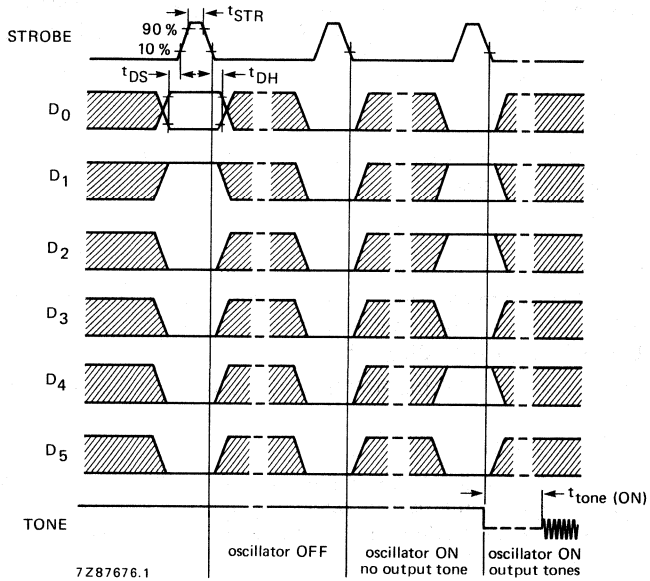


Fig. 4 Timing diagram showing control possibilities of the oscillator and the TONE output (e.g. 770 Hz + 1477 Hz) in the parallel mode (MODE = HIGH).

Serial clock and data inputs (SCL and SDA)

SCL and SDA are combined with D_0 and D_1 respectively. For the PCD3311 the selection of SCL and SDA is controlled by the MODE input. SCL and SDA are serial clock and data lines according to the I^2C bus specification (see "CHARACTERISTICS OF THE I^2C BUS"). Both inputs must be pulled-up externally to V_{DD}.

Address input (A_0)

A_0 is the slave address input and it identifies the device when up to two PCD3311 or PCD3312 devices are connected to the same I^2C bus. In any case A_0 must be connected to V_{DD} or V_{SS}.

I^2C bus data configuration (see Fig. 5)

The PCD3311 and PCD3312 are always slave receivers in the I^2C bus configuration (R/$\overline{W}$ bit = 0).

The slave address consists of 7 bits in the serial mode for the PCD3311 as well as for the PCD3312, where the least significant bit is selectable by hardware on input A_0 and the other more significant bits are internally fixed. In the serial mode the same input codes are used as in the parallel mode (see Tables 2, 3, 4, and 5). D_6 and D_7 are don't care (X) bits.

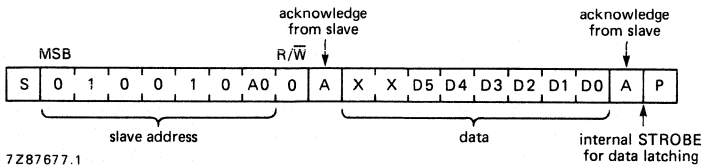


Fig. 5 I^2C bus data format.

Tone output (TONE)

The single and the dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 3 shows the frequency tolerance of the output tones for DTMF signalling; Tables 4 and 5 for the modem and melody tones.

Power-on reset

In order to avoid undefined states of the devices when the power is switched ON, an internal reset circuit sets them to the standby mode (oscillator OFF).

DEVELOPMENT DATA

Table 2 Input data for control (no output tone; TONE at V_{DD})

D_5	D_4	D_3	D_2	D_1	D_0	HEX	oscillator
X	0	0	0	0	0	00/20	ON
X	0	0	0	0	1	01/21	OFF
X	0	0	0	1	0	02/22	OFF
X	0	0	0	1	1	03/23	OFF

1 = H = HIGH voltage level
0 = L = LOW voltage level
X= don't care

FUNCTIONAL DESCRIPTION (continued)

Table 3 Input data for DTMF

D_5	D_4	D_3	D_2	D_1	D_0	HEX	symbol	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz
0	0	1	0	0	0	08		697	697,90	+ 0,13	+ 0,90
0	0	1	0	0	1	09		770	770,46	+ 0,06	+ 0,46
0	0	1	0	1	0	0A		852	850,45	−0,18	−1,55
0	0	1	0	1	1	0B		941	943,23	+ 0,24	+ 2,23
0	0	1	1	0	0	0C		1209	1206,45	−0,21	−2,55
0	0	1	1	0	1	0D		1336	1341,66	+ 0,42	+ 5,66
0	0	1	1	1	0	0E		1477	1482,21	+ 0,35	+ 5,21
0	0	1	1	1	1	0F		1633	1638,24	+ 0,32	+ 5,24
0	1	0	0	0	0	10	0	941+1336			
0	1	0	0	0	1	11	1	697+1209			
0	1	0	0	1	0	12	2	697+1336			
0	1	0	0	1	1	13	3	697+1477			
0	1	0	1	0	0	14	4	770+1209			
0	1	0	1	0	1	15	5	770+1336			
0	1	0	1	1	0	16	6	770+1477			
0	1	0	1	1	1	17	7	852+1209			
0	1	1	0	0	0	18	8	852+1336			
0	1	1	0	0	1	19	9	852+1477			
0	1	1	0	1	0	1A	A	697+1633			
0	1	1	0	1	1	1B	B	770+1633			
0	1	1	1	0	0	1C	C	852+1633			
0	1	1	1	0	1	1D	D	941+1633			
0	1	1	1	1	0	1E	*	941+1209			
0	1	1	1	1	1	1F	#	941+1477			

Table 4 Input data for MODEM frequencies

D_5	D_4	D_3	D_2	D_1	D_0	HEX	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz	remarks
1	0	0	1	0	0	24	1300	1296,94	−0,24	−3,06	V.23
1	0	0	1	0	1	25	2100	2103,14	+ 0,15	+ 3,14	
1	0	0	1	1	0	26	1200	1197,17	−0,24	−2,83	Bell 202
1	0	0	1	1	1	27	2200	2192,01	−0,36	−7,99	
1	0	1	0	0	0	28	980	978,82	−0,12	−1,18	V.21
1	0	1	0	0	1	29	1180	1179,03	−0,08	−0,97	
1	0	1	0	1	0	2A	1070	1073,33	+ 0,31	+ 3,33	Bell 103
1	0	1	0	1	1	2B	1270	1265,30	−0,37	−4,70	
1	0	1	1	0	0	2C	1650	1655,66	+ 0,34	+ 5,66	V.21
1	0	1	1	0	1	2D	1850	1852,77	+ 0,15	+ 2,77	
1	0	1	1	1	0	2E	2025	2021,20	−0,19	−3,80	Bell 103
1	0	1	1	1	1	2F	2225	2223,32	−0,08	−1,68	

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level
0 = L = LOW voltage level

Table 5 Input data for melody tones

D_5	D_4	D_3	D_2	D_1	D_0	HEX	note	standard frequency Hz*	tone output frequency Hz**
1	1	0	0	0	0	30	D#5	622,3	622,5
1	1	0	0	0	1	31	E5	659,3	659,5
1	1	0	0	1	0	32	F5	698,5	697,9
1	1	0	0	1	1	33	F#5	740,0	741,1
1	1	0	1	0	0	34	G5	784,0	782,1
1	1	0	1	0	1	35	G#5	830,6	832,3
1	1	0	1	1	0	36	A5	880,0	879,3
1	1	0	1	1	1	37	A#5	932,3	931,9
1	1	1	0	0	0	38	B5	987,8	985,0
1	1	1	0	0	1	39	C6	1046,5	1044,5
1	1	1	0	1	0	3A	C#6	1108,7	1111,7
1	0	1	0	0	1	29	D6	1174,7	1179,0
1	1	1	0	1	1	3B	D#6	1244,5	1245,1
1	1	1	1	0	0	3C	E6	1318,5	1318,9
1	1	1	1	0	1	3D	F6	1396,9	1402,1
0	0	1	1	1	0	0E	F#6	1480,0	1482,2
1	1	1	1	1	0	3E	G6	1568,0	1572,0
1	0	1	1	0	0	2C	G#6	1661,2	1655,7
1	1	1	1	1	1	3F	A6	1760,0	1768,5
0	0	0	1	0	0	04	A#6	1864,7	1875,1
0	0	0	1	0	1	05	B6	1975,5	1970,0
1	0	0	1	0	1	25	C7	2093,0	2103,1
1	0	1	1	1	1	2F	C#7	2217,5	2223,3
0	0	0	1	1	0	06	D7	2349,3	2358,1
0	0	0	1	1	1	07	D#7	2489,0	2470,4

* Standard scale based on A4 = 440 Hz.

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level

0 = L = LOW voltage level

DEVELOPMENT DATA

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

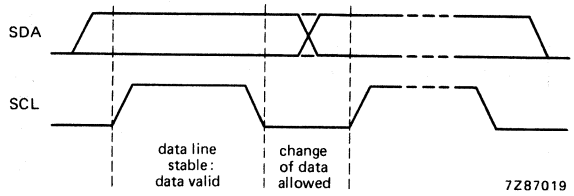


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

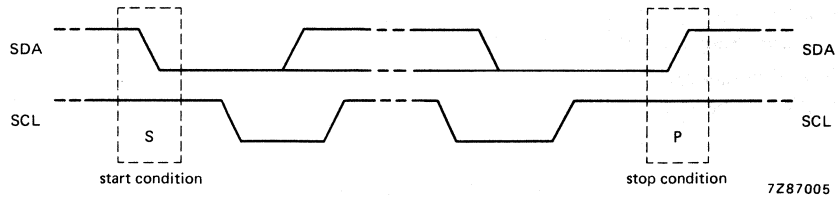


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

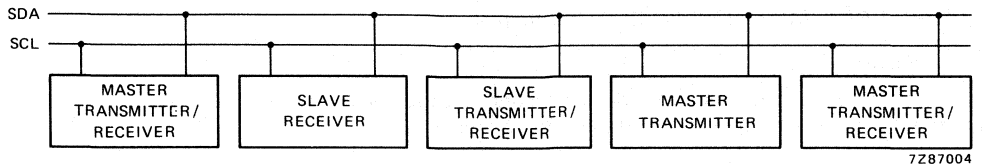


Fig. 8 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

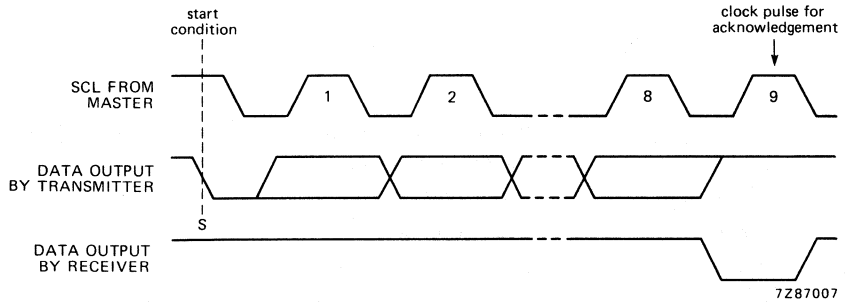


Fig. 9 Acknowledgement on the I^2C bus.

CHARACTERISTICS OF THE I²C BUS (continued)

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The ICs operate in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

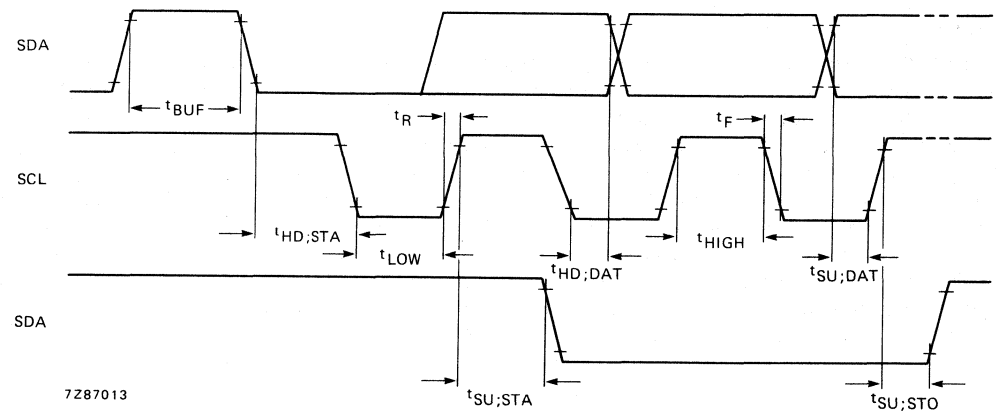


Fig. 10 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

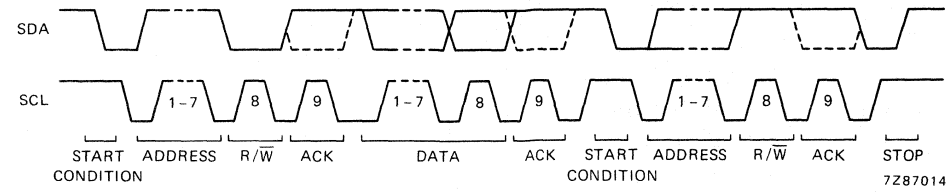


Fig. 11 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 12.

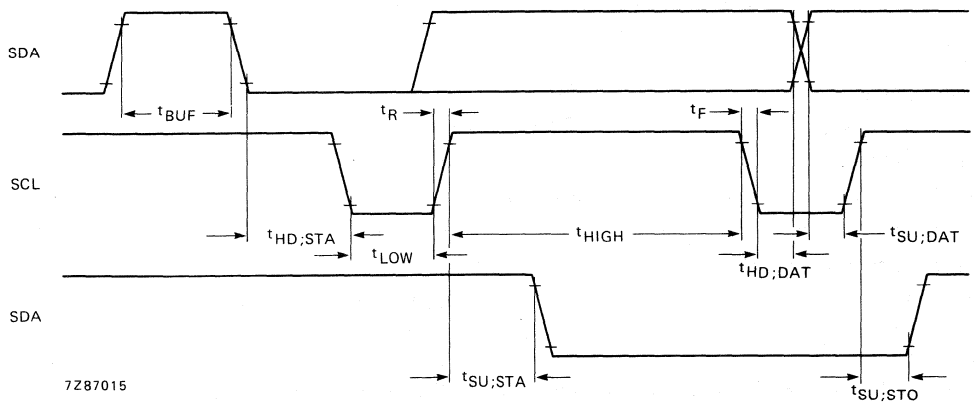


Fig. 12 Timing of the low-speed mode.

DEVELOPMENT DATA

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

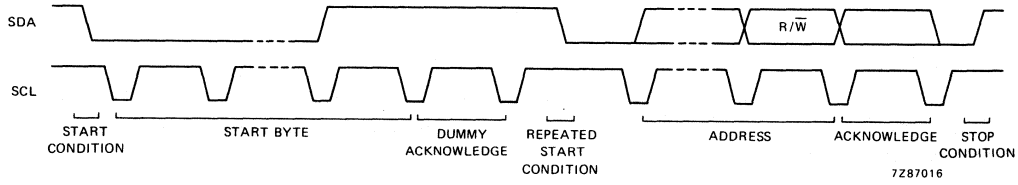


Fig. 13 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,8	+ 8,0	V
Input voltage range (any input)	V_I	−0,8	V_{DD}+0,8	V
D.C. input current (any input)	$\pm I_I$	—	10	mA
D.C. output current (any output)	$\pm I_O$	—	10	mA
Supply current	$\pm I_{DD}$; $\pm I_{SS}$	—	50	mA
Power dissipation per output	P_O	—	50	mW
Total power dissipation per package	P_{tot}	—	300	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579 545 MHz, R_{Smax} = 50 Ω; T_{amb} = −25 to + 70 °C; unless otherwise specified

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	—	6,0	V
Operating supply current (note 1) oscillator ON; V_{DD} = 3 V					
no output tone	I_{DD}	—	50	100	μA
single output tone	I_{DD}	—	0,5	1,0	mA
dual output tone	I_{DD}	—	0,6	1,2	mA
Static standby current oscillator OFF; note 1	I_{DDO}	—	—	3	μA
Inputs/outputs (SDA)					
D_0 to D_5; MODE; STROBE					
Input voltage LOW	V_{IL}	0	—	0,3 x V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	—	V_{DD}	V
D_2 to D_5; MODE; STROBE; A_0					
Pull-down input current $V_I = V_{DD}$	$-I_{IL}$	30	150	300	nA
SCL (D_0); SDA (D_1)					
Output current LOW (SDA) V_{OL} = 0,4 V	I_{OL}	3	—	—	mA
Clock frequency (see Fig. 10)	f_{SCL}	—	—	100	kHz
Input capacitance; $V_I = V_{SS}$	C_I	—	—	7	pF
Allowable input spike pulse width	t_I	—	—	100	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 14)					
DTMF output voltage levels (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
D.C. voltage level	V_{DC}	–	½ V_{DD}	–	V
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion T_{amb} = 25 °C					
dual tone; note 2	THD	–	–25	–	dB
modem tone, note 3	THD	–	–29	–	dB
Output impedance	$\|Z_O\|$	–	0,1	0,5	kΩ
OSCI input					
Maximum allowable amplitude at OSCI	$V_{OSC(p-p)}$	–	–	$V_{DD}-V_{SS}$	V
Timing (V_{DD} = 3 V)					
Oscillator start-up time	$t_{OSC(ON)}$	–	3	–	ms
TONE start-up time; note 4	$t_{TONE(ON)}$	–	0,5	–	ms
STROBE pulse width; note 5	t_{STR}	400	–	–	ns
Data set-up time; note 5	t_{DS}	150	–	–	ns
Data hold time; note 5	t_{DH}	100	–	–	ns

Notes to the characteristics

1. Crystal is connected between OSCI and OSCO; D_0/SCL and D_1/SDA via a resistance of 5,6 kΩ to V_{DD}; all other pins left open.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Related to the level of the fundamental frequency.
4. Oscillator must be running.
5. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

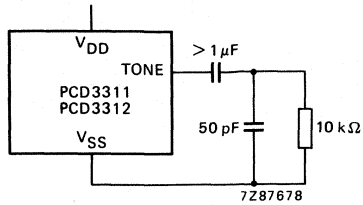


Fig. 14 TONE output test circuit.

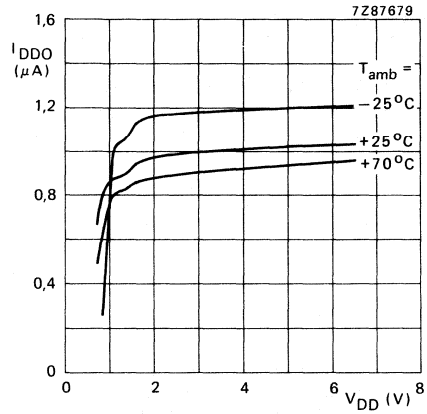


Fig. 15 Standby supply current as a function of supply voltage; oscillator OFF.

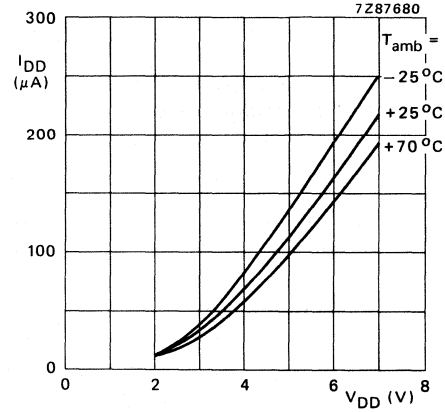


Fig. 16 Operating supply current as a function of supply voltage; oscillator ON; no output at TONE.

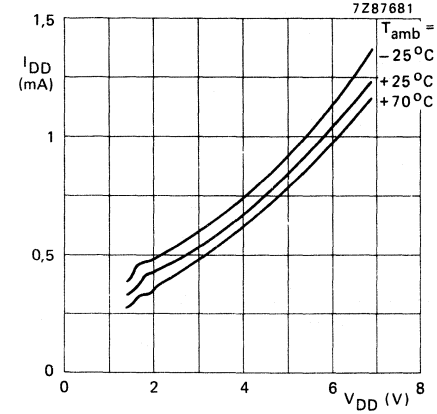


Fig. 17 Operating supply current as a function of supply voltage; oscillator ON; dual tone at TONE.

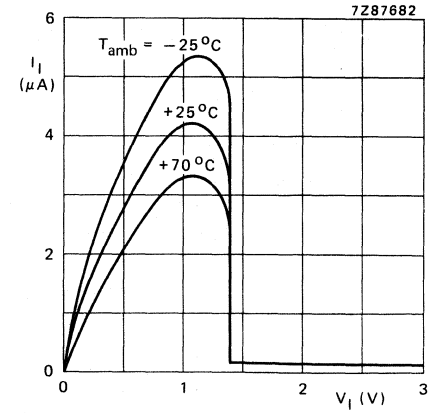


Fig. 18 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

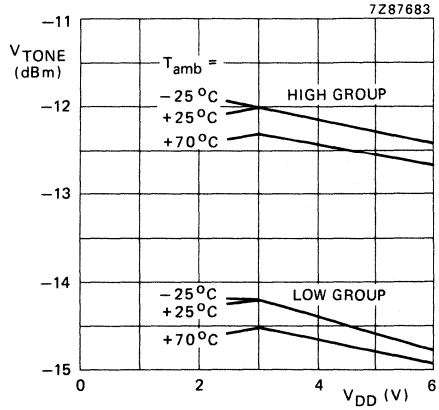


Fig. 19 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

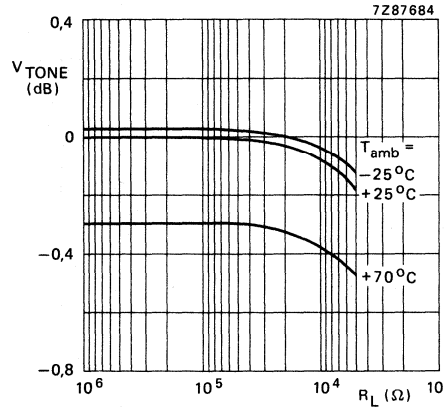


Fig. 20 Dual tone output voltage level as a function of output load resistance.

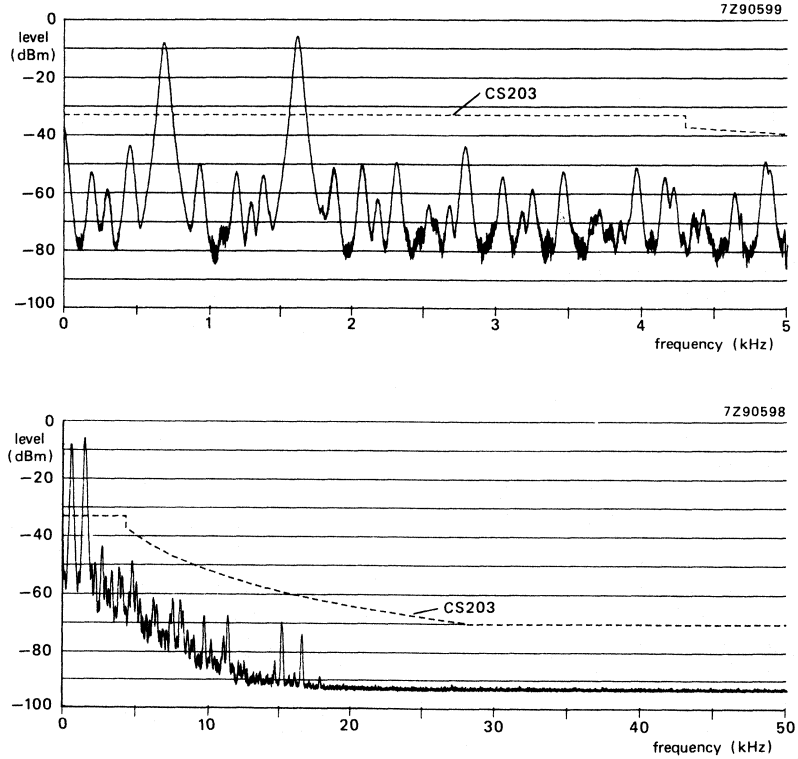


Fig. 21 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

APPLICATION INFORMATION

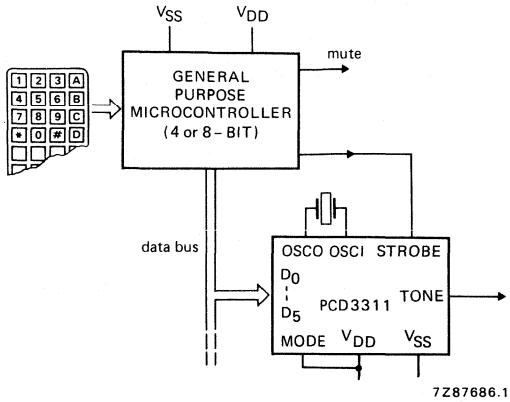


Fig. 22 PCD3311 driven by a microcontroller with parallel data-bus.

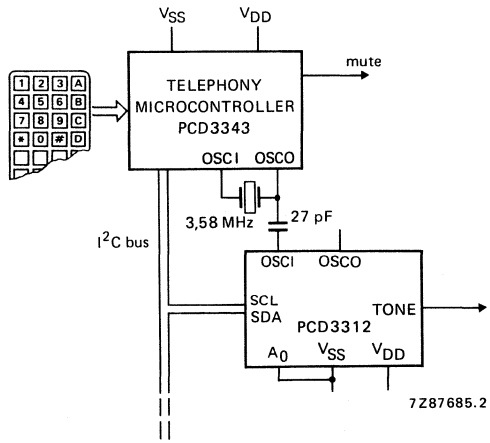
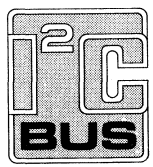


Fig. 23 PCD3312 driven by telephony microcontroller PCD3343 with serial I/O (I^2C bus).
The PCD3343 is a single-chip 8-bit microcontroller with 3K ROM/224 RAM bytes. The same application is possible with the PCD3311 with MODE = V_{SS}.



Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

CMOS MICROCONTROLLER FOR TELEPHONE SETS

GENERAL DESCRIPTION

The PCD3315C is a single-chip 8-bit microcontroller fabricated in CMOS and is a member of the PCD3343 family. It has special on-chip features for application in telephone sets.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 1536 ROM bytes
- 160 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048, MAB8400, PCD3343 and PCF8500)
- All instructions 1 or 2 cycles
- Clock frequency 100 kHz to 10 MHz
- Single supply voltage from 1,8 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator with output drive capability for peripherals
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3315CP: 28-lead DIL; plastic (SOT117).
PCD3315CT: 28-lead mini-pack; plastic (SO28; SOT136A).

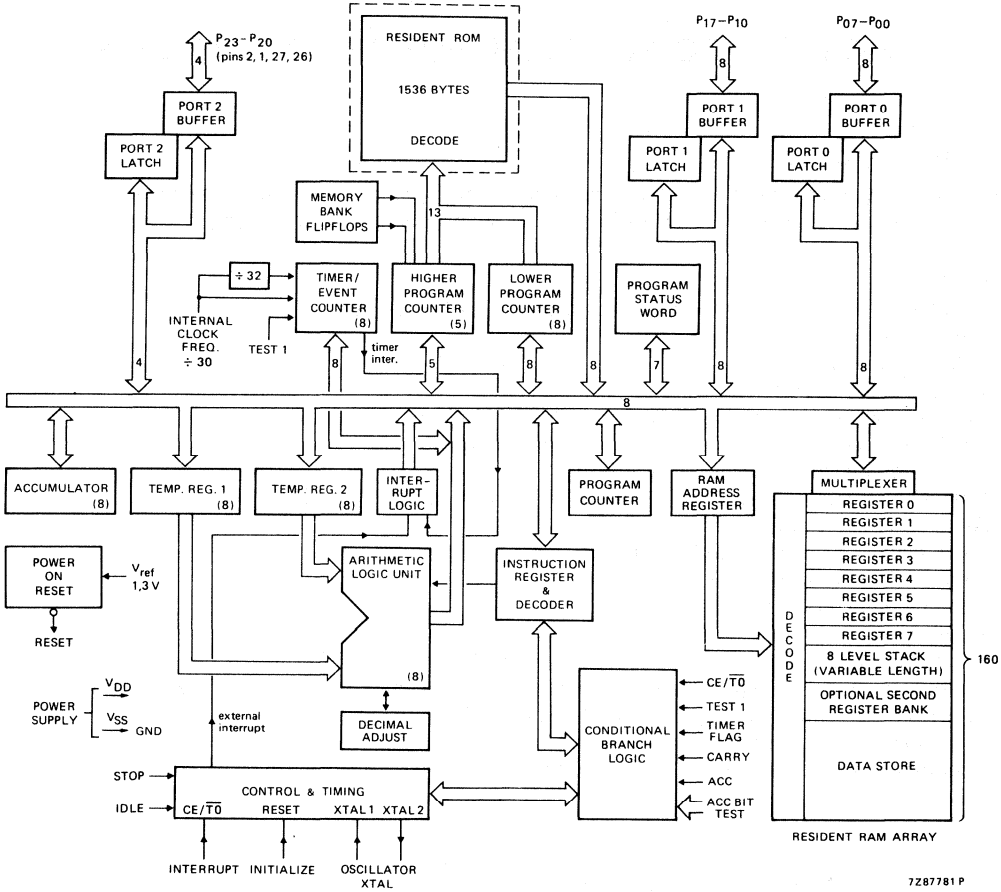
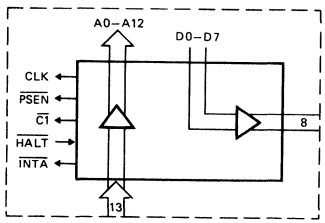
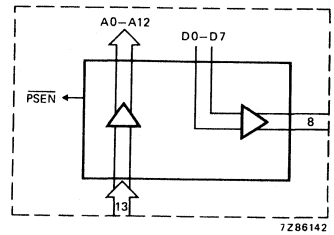


Fig. 1 Block diagram; PCD3315C.



(a)

Fig. 1a Replacement of dotted part in Fig. 1, for the PCD8500F bond-out version.



(b)

Fig. 1b Replacement of dotted part in Fig. 1, for the PCF8500B 'Piggy-back' version.

DEVELOPMENT DATA

PINNING

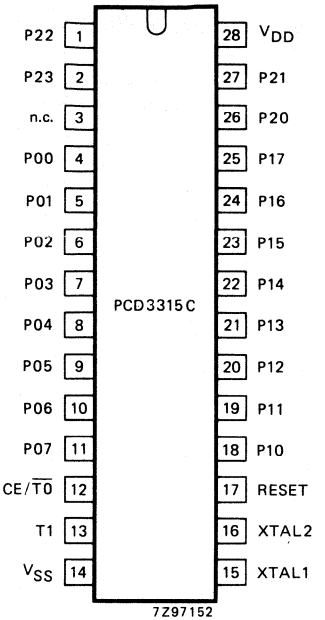


Fig. 2 Pinning diagram: PCD3315C.

PIN DESIGNATION

3	n.c.	not connected
4-11	P00-P07	**Port 0**: 8-bit quasi-bidirectional I/O port.
12	CE/$\overline{T0}$	**Interrupt/Test 0**: external interrupt input (sensitive to positive-going edge edge)/test input pin; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
13	T1	**Test 1**: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
14	V_{SS}	**Ground**: circuit earth potential.
15	XTAL 1	**Crystal input**: connection to timing component (crystal) which determines the frequency of the internal oscillator; also the input for an external clock source.
16	XTAL 2	connection to the other side of the timing component.
17	RESET	**Reset input**: used to initialize the processor (active HIGH), or output of power-on-reset circuit.
18-25	P10-P17	**Port 1**: 8-bit quasi-bidirectional I/O port.
26, 27, 1, 2	P20-P23	**Port 2**: 4-bit quasi-bidirectional I/O port.
28	V_{DD}	**Power supply**: 1,8 V to 6 V.

D.C. CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 50 Ω; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating	V_{DD}	1,8	–	6	V
STOP mode for RAM retention	V_{DD}	1,0	–	6	V
Supply current					
operating					
at V_{DD} = 3 V	I_{DD}	–	350	–	μA
IDLE mode					
at V_{DD} = 3 V	I_{DD}	–	150	–	μA
STOP mode (note 1)					
at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 1,8 V; T_{amb} = 55 °C	I_{DD}	–	–	5	μA
at V_{DD} = 1,8 V; T_{amb} = 70 °C	I_{DD}	–	–	10	μA
RESET I/O					
Switching level	V_{RESET}	–	1,2	–	V
Sink current					
at $V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current					
at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at $V_I = V_{SS}$ or V_{DD}; $\|I_O\| < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 3 V; V_O = 0,4 V	I_{OL}	0,6	1,5	–	mA
Pull-up output source current HIGH					
at V_{DD} = 3 V; $V_O = 0{,}9V_{DD}$	$-I_{OH}$	10	–	–	μA
at V_{DD} = 3 V; $V_O = V_{SS}$	$-I_{OH}$	–	–	200	μA
Push-pull output source current HIGH					
at V_{DD} = 3 V; $V_O = V_{DD}$−0,4 V	$-I_{OH}$	0,6	1,5	–	mA

Note 1

Crystal connected between XTAL 1 and XTAL 2; pin 2 pulled to V_{DD} via 5,6 kΩ resistor; CE and T1 at V_{SS}.

CMOS REPERTORY DIALLER TELEPHONE SET CONTROLLER

GENERAL DESCRIPTION

The PCD3341 is a low threshold voltage IC fabricated in CMOS. It is designed to control display, redial and repertory dialling in a telephone set. The IC has two dialling modes; pulse dialling (PD) and dual tone multi-frequency (DTMF). The architecture of the PCD3341 is identical to that of the PCD3343. It comprises an 8-bit CPU, 224 RAM bytes and 3K ROM bytes (the ROM is already programmed). The operating supply voltage is 2,5 to 6,0 V with a low current consumption in all operating modes: standby, conversation and dialling modes.
Up to 18 digits and 2 manual access pauses can be stored for redial, extended redial and direct dial purposes together with on-chip storage for 10 repertory numbers.
For expansion of the system the PCD3341 provides a two wire serial input/output port, in accordance with the I^2C bus specifications, to control the DTMF tone generator, LCD drivers and additional RAMs for additional repertory numbers.

Features

- Pulse dialling
- DTMF dial control of tone generator PCD3312
- Redial
- Extended redial
- Electronic notepad
- Direct dialling (emergency call)
- On-chip storage for 10 repertory dial numbers
- 18-digit capacity for each autodial memory
- Flash or register recall
- Access pause generation and termination
- Manual reset of autodial RAM
- On-chip power-on reset
- Programmed for improved noise immunity
- Extention possible with external RAM for up to 110 repertory dial numbers
- Uses standard 4 x 4 keyboard (single or double contact)
- Additional 10-digits first in first out memory, for infinite long numbers control an LCD via the I^2C bus.
- Four extra function keys: program/autodial, flash, redial, access pause
- Keyboard expansion possible for 10 separated repertory dialled numbers
- Automatic recognition of PABX-digits; resulting in an access pause insertion
- Hold input and access pause output (APO) to adjust the duration of the access pause and facilitate use of tone recognizers
- Six diode or strap functions: mark-to-space ratio, tone burst time, inter-digit pause time, access pause time, normal or expanded keyboard, normal or direct dialling

QUICK REFERENCE DATA

Operating supply voltage	V_{DD}	2,5 to 6,0	V
Standby supply voltage	V_{DD}	min. 1,8	V
Operating currents at V_{DD} = 3 V			
conversation mode	I_{DDC}	typ. 270	μA
dialling mode	I_{DDD}	typ. 600	μA
Standby supply current at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DDO}	typ. 1,2	μA
Crystal frequency	f	3,58	MHz
Operating ambient temperature range	T_{amb}	−25 to + 70	°C

PACKAGE OUTLINES

PCD3341P: 28-lead DIL; plastic (SOT117).
PCD3341T: 28-lead mini-pack; plastic (SO28; SOT136A).

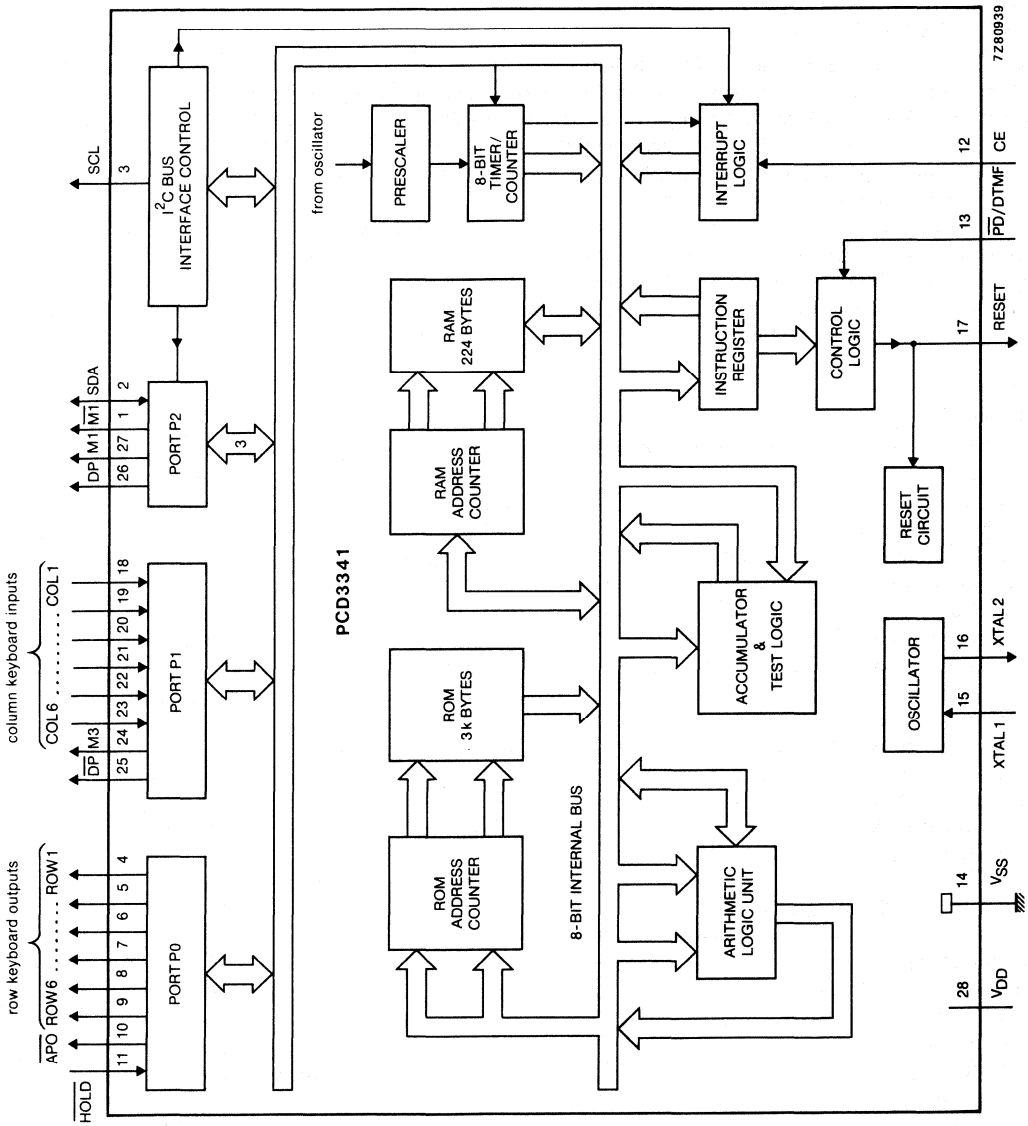


Fig. 1 Block diagram.

DEVELOPMENT DATA

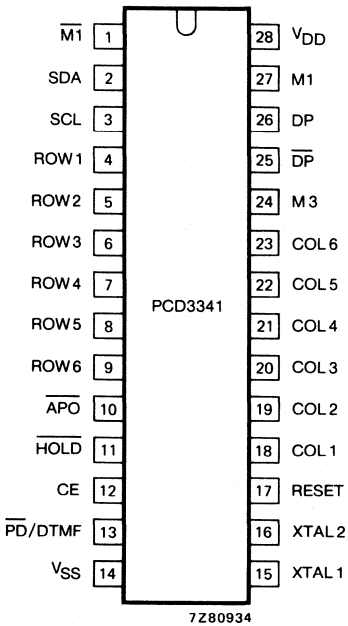


Fig. 2 Pinning diagram.

PINNING

1	$\overline{M1}$	inverted output of M1
2	SDA	serial data
3	SCL	serial clock
4	ROW 1	scanning row keyboard outputs
5	ROW 2	
6	ROW 3	
7	ROW 4	
8	ROW 5	
9	ROW 6	
10	$\overline{APO}$	access pause output
11	$\overline{HOLD}$	hold input
12	CE	chip enable input
13	$\overline{PD}$/DTMF	input to select pulse or DTMF dialling
14	V_{SS}	negative supply
15	XTAL 1	input to on-chip oscillator
16	XTAL 2	output from on-chip oscillator
17	RESET	reset input/output
18	COL 1	sense column keyboard inputs
19	COL 2	
20	COL 3	
21	COL 4	
22	COL 5	
23	COL 6	
24	M3	muting output
25	$\overline{DP}$	inverted pulse dialling output
26	DP	pulse dialling output
27	M1	muting output
28	V_{DD}	positive supply

FUNCTIONAL DESCRIPTION

Power supply (V_{DD}; V_{SS})

Power supply must be retained for data storage.

Clock oscillator (XATL 1; XTAL 2)

The time base for the PCD3341 is a crystal controlled on-chip oscillator which is completed by connecting a 3,58 MHz crystal between XTAL 1 and XTAL 2. The oscillator starts when V_{DD} reaches the operating voltage level and CE = HIGH. The output XTAL 2 can be used to drive the oscillator input of the PCD3312.

Chip Enable (CE)

This active HIGH input is used to initialize part of the system, to select the operational or standby mode and to handle line power breaks.

Pulse dialling outputs (DP; $\overline{DP}$)

DP output drives an external switching transistor or relay in pulse dialling mode. This output is also used to pulse out a calibrated FLASH pulse (recall register) of 90 ms duration as soon as the keyboard input FLASH is activated by depressing the key F. The FLASH function acts like CE with respect to redial.

Muting outputs (M1; $\overline{M1}$; M3)

M1 output is used for muting during the dialling sequence. For pulse dialling M1 goes HIGH with the first inter-digit pause and remains active for 33 or 40 ms (mark-to-space selection) following the last break pulse after the last digit held in store has been transmitted. In DTMF dialling, input $\overline{PD}$/DTMF is HIGH. M1 is HIGH as long as two out of the eight frequency signals are sent, then remains HIGH for an additional 80 ms (hold-over time).
$\overline{M1}$ output is the inverted output of M1.
M3 output is an AND function with $\overline{DP}$ and M1 as input, used for direct drive of a switching transistor for dialling pulses and muting.

Hold input ($\overline{HOLD}$); **access pause output** ($\overline{APO}$)

The hold input suspends dialling after completion of the current digit, or in pulse dialling during an inter-digit pause.
The hold function facilitates an extra time delay during dialling under control of external circuits (dialling tone recognizer). In the hold state ($\overline{HOLD}$ = LOW) the muting output is also LOW, thus the IC is in the conversation mode. The $\overline{HOLD}$ input can be controlled by the access pause output (APO) directly or indirectly via a dialling tone recognizer (see Fig. 3). The tone recognizer automatically terminates access pauses upon receipt of the access tone, regardless of whether this occurs during or after the access pause time (t_{ap}). The $\overline{APO}$ output will go LOW when an access pause is recognized.

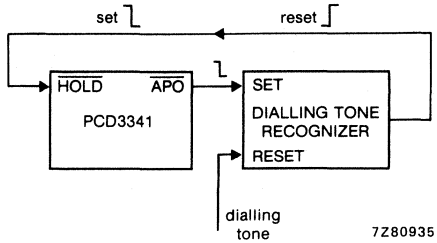


Fig. 3 Automatic variation of length of an access pause under control of a dialling tone recognizer.

Serial data (SDA); **serial clock** (see Fig. 8)

The serial I/O lines SDA and SCL are used to control the PCD3312 in the DTMF dialling mode, additional RAMs (PCD8570) for repertory dialling and LCD drivers (PCF8577). Both outputs require external pull-up resistors.

Keyboard inputs/outputs (COL 1 to 6; ROW 1 to 6)

The sense column inputs COL 1 to COL 6 and the scanning row outputs ROW 1 to ROW 6 are directly connected to a 4 x 4 single contact keyboard matrix. The keyboard organization is shown in Fig. 4.
In pulse dialling mode the valid keys are the 10 numeric keys (0 to 9). The 6 non-numeric keys (A, B, C, D, *, #) have no effect on the dialling.
In DTMF dialling mode the 10 numeric keys and the 6 non-numeric keys are valid. On-chip repertory dialling uses the 10 numeric numbers (no external RAM).
With extended repertory dialling 10 extra keys (M1 to M10) are used (on-chip or external RAM).
Row 5 of the keyboard contains the following special function keys:

- P memory clear and programming (notepad)
- FL flash or register recall
- R redial
- AP manual access pause entry

Diode options (ROW 6)

Row 6 is added to the keyboard matrix to provide the following selections:

Mark-to-space ratio (M/S)
OFF M/S 3:2
ON M/S 2:1

Tone burst time (t_{tb})
OFF t_{tb} = 70 ms
ON t_{tb} = 100 ms

Inter-digit pause (IDP)
OFF IDP = 900 ms
ON IDP = 500 ms

Access pause time (t_{ap})
OFF t_{ap} = 1,5 s (DTMF); 3 s (PD)
ON t_{ap} = 2,5 s (DTMF); 5 s (PD)

Keyboard expansion (EKB)
OFF normal keyboard
ON expanded keyboard

Normal/direct call (N/D)
OFF normal call mode
ON direct call (emergency)

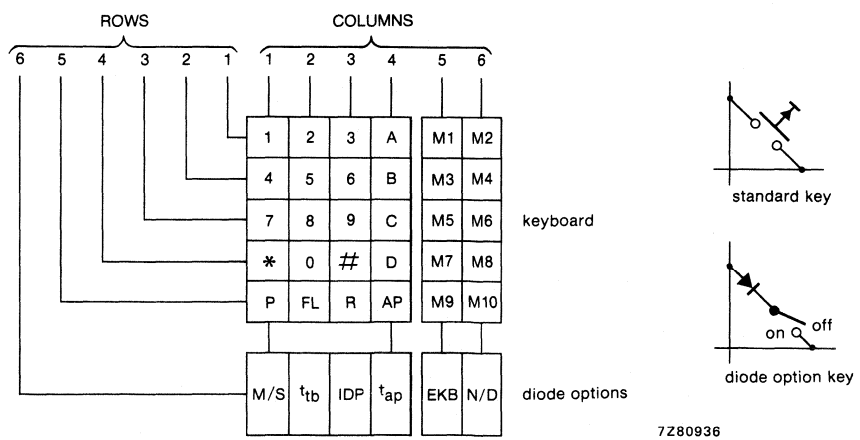


Fig. 4 Keyboard organization.

FUNCTIONAL DESCRIPTION (continued)

Dialling mode selection input ($\overline{PD}$/DTMF)

This input selects the dialling mode:

- $\overline{PD}$/DTMF = LOW selects pulse dialling
- $\overline{PD}$/DTMF = HIGH selects DTMF dialling

Reset input/output (RESET)

When the reset input is active HIGH it can be used to initialize the IC.
In normal application this is achieved by the CE input.
Reset is also an output of the internal power-on-reset circuit, which generates a reset pulse if V_{DD} drops below 1,3 V (typ.).

OPERATION

The PCD3341 has 3 operating modes:

- Standby
- Conversation
- Dialling

Standby mode

When the chip enable input (CE) is LOW the IC is disabled. In the standby mode the only current drawn is from a back up supply (battery or line powered), for memory retention, holding up to 13 call numbers for repertory and redialling.

Conversation mode

After the handset is lifted CE is activated and V_{DD} rises to the working voltage. M1 muting is inactive and speech or dial tone can be heard. With the oscillator operating the chip is ready to accept keyboard entries. Current consumption is $< 300\ \mu A$.

Dialling mode

The dialling mode starts with first valid keyboard entry when it initiates:

- a normal call of a newly dialled number
  or
- a repertory or redialling cycle of previously entered and stored numbers

The current consumption is $< 600\ \mu A$.

Pulse dialling ($\overline{PD}$/DTMF = LOW)

The keyboard entry initiates a recall from a previously stored number or is a simultaneous keying-in and pulsing-out activity, with storing for possible later recall. If in the recalled number or at keying-in the keys *, #, A, B, C, D keys are used these digits will not be transmitted. Normally, keying-in is faster than pulsing-out (fed from the redial register). Pulsing sequences start with M1 going HIGH followed by an inter-digit pause of 900 or 500 ms duration (diode option IDP), followed by a sequence of pulses corresponding to the present digit in store. Each pulse starts with a mark (line break) followed by space (line make).
The pulse period is 100 ms with a mark-to-space ratio of 3:2 or 2:1 (diode option). After transmission os a digit, the next digit will be processed again starting with an inter-digit pause. The pulsing is suspensed if $\overline{HOLD}$ goes LOW. It will be terminated if the current memory content has been transmitted or the handset is replaced (CE = LOW $< t_{rd}$). The pulses are available on the DP line. After completion of the number string M1 goes LOW and the circuit changes from dialling mode to conversation mode.

Dual Tone Multi Frequency dialling ($\overline{PD}$/DTMF = HIGH)

The PCD3341 converts keyboard inputs into serial data, via the I^2 bus lines SDA and SCL, suitable for control of the PCD3312 DTMF tone generator. These tones are transmitted with minimum tone burst durations of 70, 70 ms. The maximum tone burst duration is equal to the key depression time. With redial and repertory dialling tones are automatically fed at a rate of 70, 70 ms. After dialling the muting output goes LOW after a hold-over time of 80 ms and the circuit is switched to the conversation mode.

SYSTEM EXTENSION

The PCD3341 can control the extensions of a telephone set via its I²C bus. Both in DTMF dialling and pulse dialling, an extended repertory dialler provides more than 10 stored on-chip numbers and the indication on a L.C. display of all keys pressed (programming or dialling procedure).
The following ICs can be used in combination with the PCD3341:

- PCD3312 DTMF generator
- PCD8570 256 x 8 static CMOS RAM
- PCF8577 2 LCD drivers in LCD module

DTMF dialling

By using a PCD3312 DTMF generator with I²C bus interface, the PCD3341 may be extended to Dual Tone Multi Frequency dialling applications. This is selected when the input pin $\overline{PD}$/DTMF = HIGH.
DTMF dialling is much faster than pulse dialling. Each keypad digit corresponds to a unique combination of two frequencies; one from a group of 4 high frequencies, and one from a group of 4 low frequencies. Both frequencies are applied simultaneously to the line.
The PCD3341 is capable of directly driving the PCD3312 oscillator.

Repertory dialling

If more than 10 stored numbers are required repertory dialling can be extended by the I²C bus lines and external CMOS RAMs (PCD8570) with serial interface. With a RAM capacity of 256 x 8 bits another 20 stored numbers can be added. A maximum of 5 external RAMs can be served by the PCD3341 directly. This provides a telephone with a total capacity of 110 (100) stored numbers.
The number of external RAMs connected on the I²C bus lines is automatically checked by the PCD3341 at initial turn-on.
To identify each RAM, the PCD8570 has 3 hardware address pins (A2, A1, A0) which allows a maximum of 8 RAMs to be connected.

Table 1 Repertory number organisation

PCD8570 address			Keyboard digit(s)	
A2	A1	A0	Without EKB	With EKB
0	0	0	10 to 29	00 to 19
0	0	1	30 to 49	20 to 39
0	1	0	50 to 69	40 to 59
0	1	1	70 to 89	60 to 79
1	0	0	90 to 99	80 to 99
PCD3341			00 to 09	M1 to M10

Display

To display the dialled phone number or programmed number the PCD3341 provides the signals to control a LC Display module using two PCD8577 duplex drivers. These signals are fed via the I²C bus lines.
In the dialling and programming modes the digits are displayed from right to left in the sequence entered by the keyboard. The access pause is indicated by the bar. If the number of digits exceeds 16, they drop out on the left side of the display.

OPERATING PROCEDURE

Initialization

At the first application of the standby power supply, the PCD3341 will clear the RAM in order to avoid a wrong content.
By lifting the handset the buffer capacitor for V_{DD} is charged to the operating voltage. CE will than be activated. Within start-up time the oscillator starts and the initialization program begins.

Automatic access pause setting

Before the start procedure, the system can also be initialized by setting the access pause system (e.g. for PABX applications). The circuit will automatically insert an access pause after recognition of access of a number within a digit group. This (or these) digit(s) must be programmed. Up to a maximum of 3 digits per group can be programmed.
The procedure is as follows:

- Depress and hold pushbutton P
- Press and release pushbutton R
- Enter 1, 2 or 3 digits as access digit for first group
- Release pushbutton P (only if no second group is required)
- Press and release pushbutton R
- Enter 1, 2 or 3 digits for second group
- Release pushbutton P

Apart from the procedure that automatically detectes and insertes access pause(s), a telephone number with up to 2 additional manually inserted access pauses can be dialled or programmed, by pressing button AP. In DTMF dialling mode each access pause has a duration of 1,5 or 2,5 seconds. In PD mode each access pause has a duration of 3 or 5 seconds.

Data entry

The debounce keyboard entries are written into the on-chip CMOS RAM in consecutive order.

Dialling

If the first pushbutton pressed is 0 to 9 in pulse dialling or 0-9, A to D, *, # in DTMF dialling, digits are entered into the redial register after initial clearing. During the data entry the circuit starts with the transmission of the call and is unaffected by the speed of entry. Transmission continues as long as further data input has to be processed. Up to 18 digits can be stored in the redial register. After the main store overflows, a 10 digit First-In First-Out register (FIFO) takes over as buffer. After transmitting the first digit of the FIFO register this position is automatically cleared to provide space for the storage of new data. In this way, the total number that can be transmitted is unlimited, provided the key-in rate is not excessive. However, if the FIFO register overflows (more than 10 digits in store) further input will be ignored.

Redial

If the first digit entered is "REDIAL" R, the stored number in the redial register will be recalled and transmitted.
If the current content is less than 18 digits, new digits entered are appended automatically to the redial number. After the 18th digit has been entered the FIFO register will take over as previously described in the dialling section.

OPERATING PROCEDURE (continued)

Extended Redial

The dialled number is saved in the extended redial buffer if pushbutton P is the last key pressed before the handset is replaced.
By pressing and releasing pushbutton P followed by pressing and releasing pushbutton R, will cause the extended redial register to be recalled and transmitted in the same manner as by redial. If less than 18 digits are contained in the extended redial register, digits can be added until the total content is 18. After the 18th digit the FIFO register will take over as before. The original number is not affected by the new digits

Direct call/Emergency call

This is a diode option usually operated by a turn key switch. If set the programmed number will be dialled by pressing ANY key. In normal mode the turn key switch is positioned OFF with the diode option OFF.
Programmed is achieved by lifting the handset, depressing the P pushbutton with key in the OFF position, then turning the key switch to ON position (diode option ON). The required telephone number is now entered. Pushbutton P can now be released and the handset replaced.
After programming, the key switch can remain in the ON position (activating emergency call) or be switched off (normal mode). If the key switch is the ON position, emergency calling is possible by removing the handset and pressing ANY pushbutton.

Repertory dialling

The PCD3341 has an on-chip CMOS RAM to store up to ten 18 digit numbers, and can be extended up to 100 (110) numbers using external CMOS RAMs with 2-line serial interface. The circuit automatically checks the number of external RAMs. If no external RAM is connected the on-chip repertory is limited to 10 numbers. In this application the standard keypad (0 to 9) and one digit address can be used. With the diode option EKB (expanded keyboard) ON the extended keypad matrix (M1 to M10) can be used to access the on-chip repertory. If external RAMs are connected the capacity of the repertory can be increased up to 100 (110) numbers. In this application the standard keypad (0 to 9) and/or the extended keypad (M1 to M10) can be used to access the repertory (see Table 1).
Programming is possible only after the handset is lifted and no pushbutton is operated before P.
Programming is achieved by pushbutton P being continually depressed, entering the repertory address of one or two digits, followed by the number (including access digits) then releasing pushbutton P.
The designated telephone number, including access digits, is dialled after pressing pushbutton P followed by the address. With extended keypad a single address pushbutton is required. After transmission of the repertory sequence, it is possible to manually enter additional digits (see redial).

Successive repertory dialling during a call (chain dialling)

It is possible to dial more than one repertory number during one single telephone call.
The following procedures are possible:

- Redial, extended redial or a repertory number followed by new digits
- Repertory number followed by one or more repertory numbers
- Normal dial, redial or extended redial followed by one or more repertory numbers

Note pad

Note pad provides the facility to store a number during conversation mode without dialling and muting. This number will be stored in the extended redial register and recalled with the extended redial procedure.
The programming procedure is as follows:

- Depress and release pushbutton P
- Depress and release pushbutton P
- Enter the telephone number
- Depress and release pushbutton P

If a wrond number is entered, correction is achieved by re-starting the programming procedure.

Memory clear

A built-in manually total clear facilitates resetting of the autodial RAM after servicing, maintenance or telephone set delivery.
The procedure is as follows:

- Hook-on, depress and keep depressed keys 2, 5, 8, 0
- Hook-off, release keys 2, 5, 8, 0

Table 2 Display indications

procedure	key procedure	display indication
Programming automatic access pauses after access digits	$\bar{P}$R00R9	Pr–00–9
dialling	004627530	00–4627530
redial	R	r=00–4627530
Extended redial		
programming	004627530P	00–4627530P
dialling	PR	Pr=00–4627530
emergency redial		
programming	N/D OFF, $\bar{P}$, N/D ON(+ TN)	PH–00–4627530
dialling	N/D ON any key	H=00–4627530
repertory programming	$\bar{P}$12004627530	P12–00–4627530
programming	$\bar{P}$12004627530	P12–00–4627530
dialling	P12	P12=00–4627530
repertory with extended keyboard		
programming	$\bar{P}$ M1 004627530	PM1–00–4627530
dialling	M1	M1=00–4627530
note pad programming	PP0080808P	7530PP00–808080P
note pad dialling	PR	00–808080
error	incorrect key procedure	≡

Where: TN = telephone number
P = depress and release pushbutton P
$\bar{P}$ = depress pushbutton P continually during programming
R = depress and release pushbutton R

RATINGS

Limiting values in accordance with the Absolute maximum System (IEC 134)

Supply voltage range (pin 28)	V_{DD}		−0,8 to 8	V
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
All input voltages	V_I	V_{SS} −0,8 V to V_{DD}	+ 0,8	V
Total power dissipation	P_{tot}	max.	500	mW
Power dissipation per output	P_O	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,57954 MHz; R_S = 50 Ω max.; T_{amb} = 25 °C; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Operating supply voltage	V_{DD}	2,5	3	6,0	V
Operating supply current					
conversation mode (CE = 1)	I_{DDC}	–	270	–	μA
dialling mode (CE = 1)	I_{DDD}	–	600	–	μA
Standby supply voltage (CE = 0)	V_{DDO}	1,8	3	6,0	V
Standby supply current (CE = 0)	I_{DDO}	–	–	2,5	μA
RESET I/O					
Switching level					
at $V_{DD} < V_{RESET}$	V_{RESET}	–	1,3	1,5	V
Sink current					
at $V_{DD} < V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW (any pin)	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH (any pin)	V_{IH}	$0{,}7V_{DD}$	–	–	V
Input leakage current; CE					
at $V_I = V_{SS}$ to V_{DD}	$-I_{IL}$	–	–	100	nA
at CE = 1	I_{IL}	–	–	1	μA
Keyboard contact resistance					
Keyboard ON	R_{KON}	–	–	1	kΩ
Keyboard OFF	R_{KOFF}	100	–	–	kΩ
Outputs					
M1, $\overline{M1}$, M3, DP, $\overline{DP}$					
Output sink current					
at V_{OL} = 0,4 V	I_{OL}	–	1,5	–	mA
Output source current					
at V_{OH} = 2,6 V (push-pull)	$-I_{OH}$	–	1,5	–	mA
SDA, SCL					
Output sink current					
at V_{OL} = 0,4 V	I_{OL}	1,5	–	–	mA
Output source leakage current					
at V_{OH} = 0 to V_{DD} (open drain)	$-I_{OH}$	–	–	1	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Inputs/Outputs					
COL 1 to 6, ROW 1 to 6, $\overline{HOLD}$, $\overline{APO}$					
Output sink current at V_{OL} = 0,4 V	I_{OL}	0,6	1,5	–	mA
Output source current at V_{OH} = 2,6 V	$-I_{OH}$	25	–	–	μA
Output source current at $V_{OH} = V_{SS}$	$-I_{OH}$	–	–	200	μA
TIMING (see Figs. 5, 6 and 7)					
Clock start-up time	t_{ON}	–	–	10	ms
Oscillator period	C_P	–	–	0,279	μs
Pulse dialling ($\overline{PD}$/DTMF input LOW; M/S diode OFF)					
Mark-to-space ratio 3:2					
Dialling pulse frequency	f_{DP}	–	9,94	–	Hz
Dialling pulse period	t_{DP}	–	100,6	–	ms
Break time	t_b	–	60,3	–	ms
Make time	t_m	–	40,3	–	ms
Mark-to-space ratio 2:1 (M/S diode ON)					
Dialling pulse frequency	f_{DP}	–	9,94	–	Hz
Dialling pulse period	t_{DP}	–	100,6	–	ms
Break time	t_b	–	67	–	ms
Make time	t_m	–	33,5	–	ms
Access pause					
t_{ap} diode OFF	t_{ap}	–	3	–	s
t_{ap} diode ON	t_{ap}	–	5	–	s
Mute hold-over time during access pause	t_h	–	1	–	s
Inter-digit pause					
IDP diode OFF	t_{id}	–	892	–	ms
IDP diode ON	t_{id}	–	496	–	ms
Reset delay time	t_{rd}	–	160,9	180	ms
Reset delay time during access pause	t_{rd}	–	302	320	ms
Debounce time	t_e	13,5	–	–	ms
Flash pulse duration	t_{FL}	–	94	–	ms

parameter	symbol	min.	typ.	max.	unit
DTMF dialling ($\overline{PD}$/DTMF input HIGH; SDA timing via PCD3312)					
Tone transmission time (t_{tb} diode OFF)	t_t	–	74	–	ms
Tone break time	t_b	–	74	–	ms
Mute hold-over time during dialling	t_h	–	154	–	ms
Tone transmission time (t_{tb} diode ON)	t_t	–	101	–	ms
Tone break time	t_b	–	101	–	ms
Mute hold-over time during dialling	t_h	–	101	–	ms
Access pause					
t_{ap} diode OFF	t_{ap}	–	1,5	–	s
t_{ap} diode ON	t_{ap}	–	2,5	–	s
Mute hold-over time during access pause	t_h	–	1	–	s

DEVELOPMENT DATA

Timing diagrams

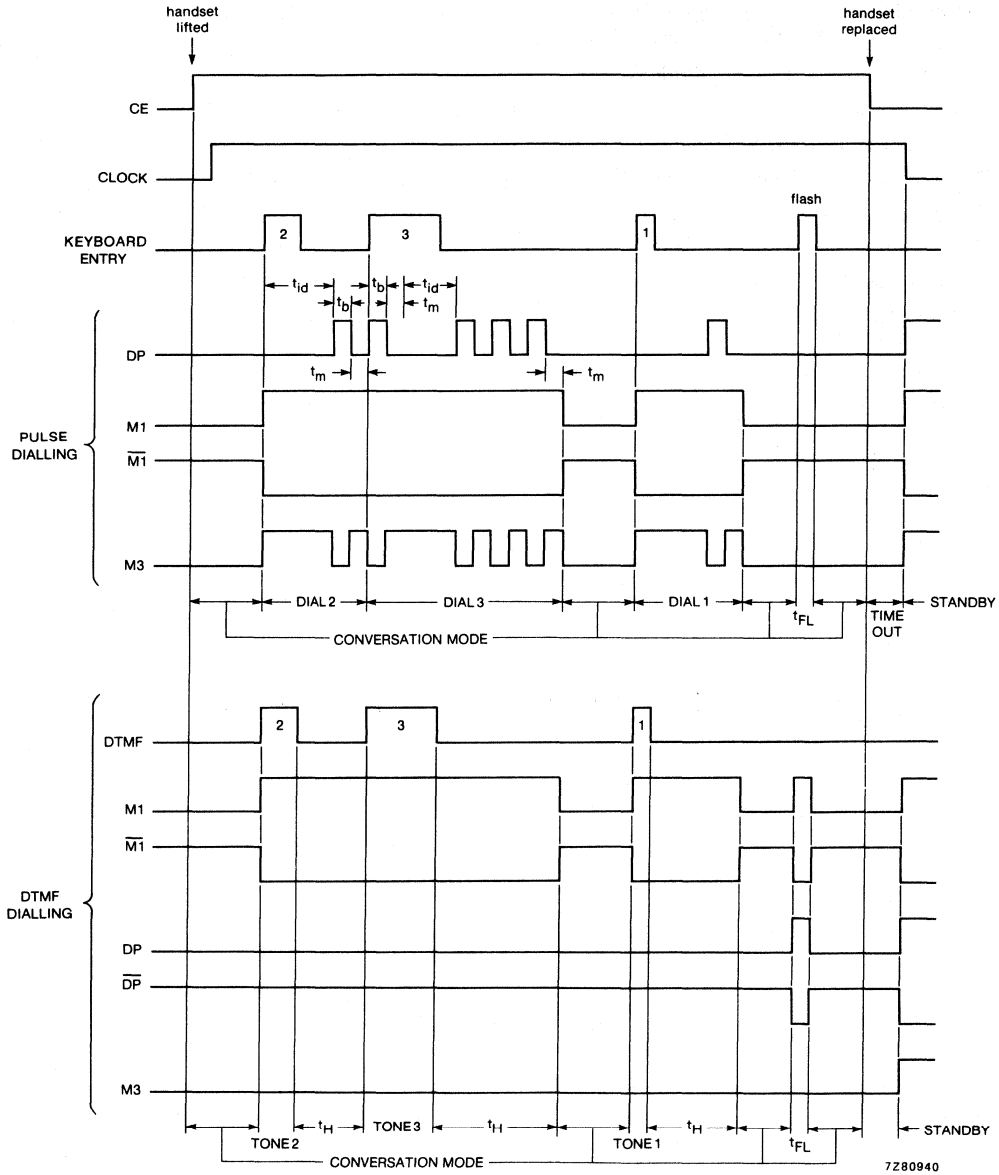


Fig. 5 Pulse dialling; DTMF dialling.

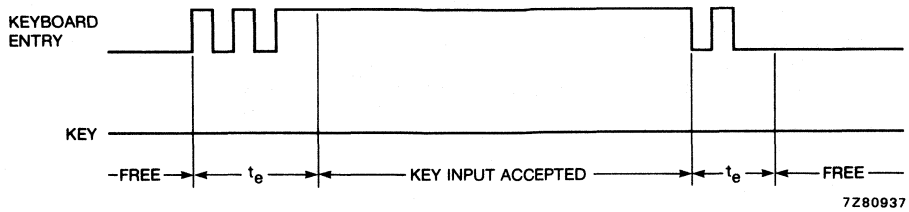


Fig. 6 Keyboard entry with noise debounced.

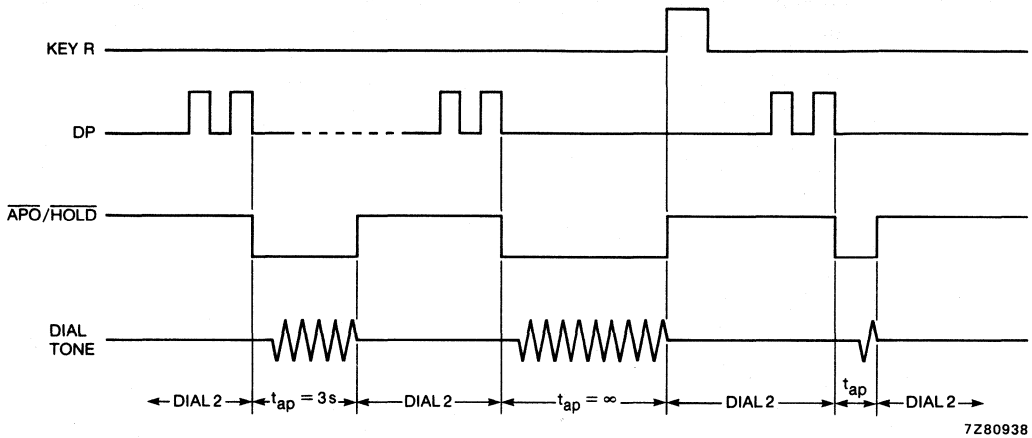


Fig. 7 Access pause with reset by; internal 3 s timer, key R, tone recognizer.

DEVELOPMENT DATA

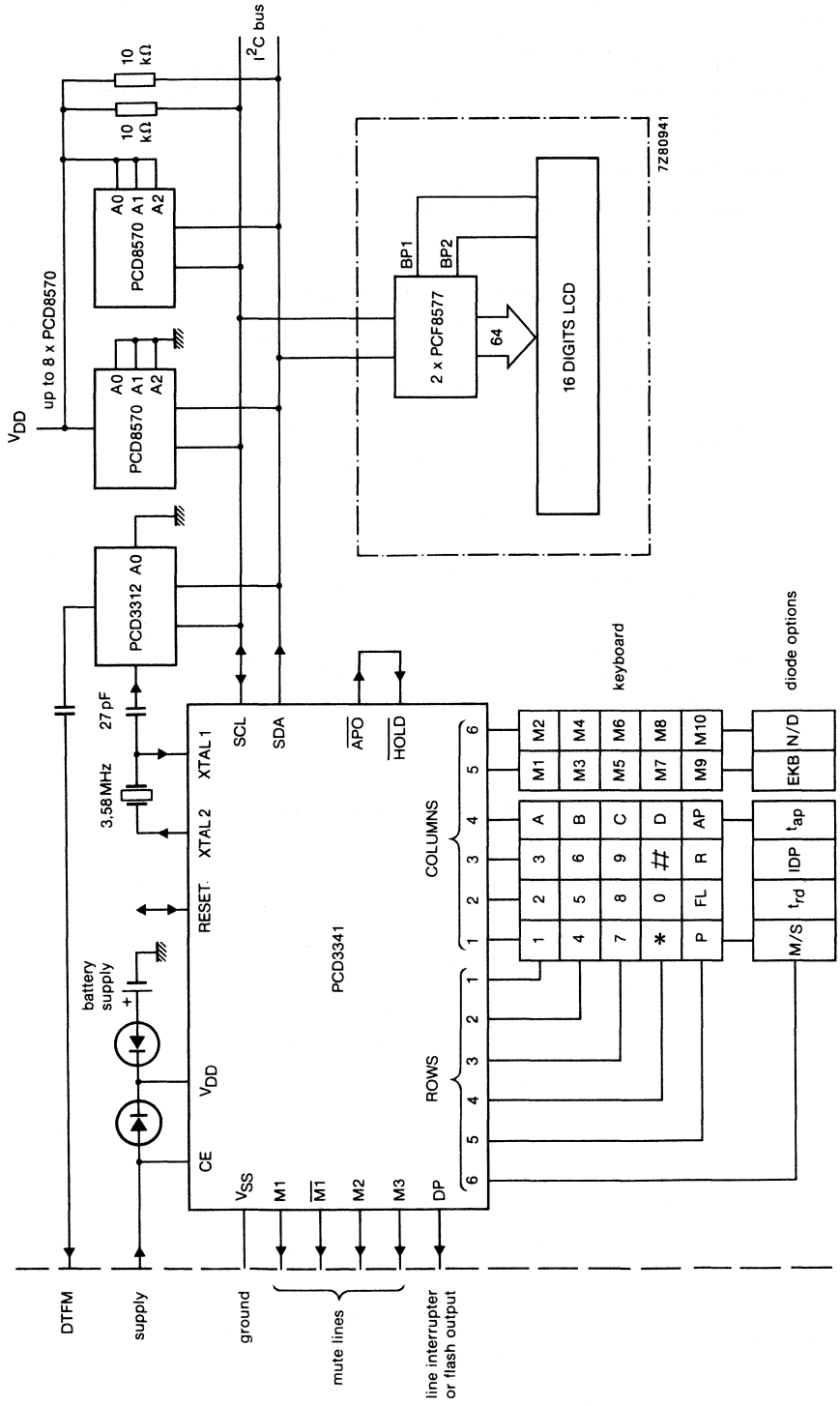


Fig. 8 PCD3341 in combination with PCD3312 (DTMF dialler), PCD8570 (2 K RAM) and PCF8577 (display drivers).

CMOS MICROCONTROLLER FOR TELEPHONE SETS

GENERAL DESCRIPTION

The PCD3343 is a single-chip 8-bit microcontroller fabricated in CMOS. It has special on-chip features for application in telephone sets.
The device is mask programmable, designed to provide telephone dialling facilities such as redial, repertory dial, emergency call, keyboard scan and control for liquid crystal display, pulse dial and/or DTMF dial via dedicated peripheral.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 3 K ROM bytes
- 224 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/$\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- Serial I/O which can be used in bus systems with more than one master (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048, MAB8400 and PCF8500)
- All instructions 1 or 2 cycles
- Clock frequency 100 kHz to 10 MHz
- Single supply voltage from 1,8 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator with output drive capability for peripherals (e.g. PCD3312 DTMF generator)
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: −25 to + 70 °C

PACKAGE OUTLINES

PCD3343P : 28-lead DIL; plastic (SOT117).
PCD3343D: 28-lead DIL; ceramic (CERDIP) (SOT135A).
PCD3343T : 28-lead mini-pack; plastic (SO28; SOT136A).

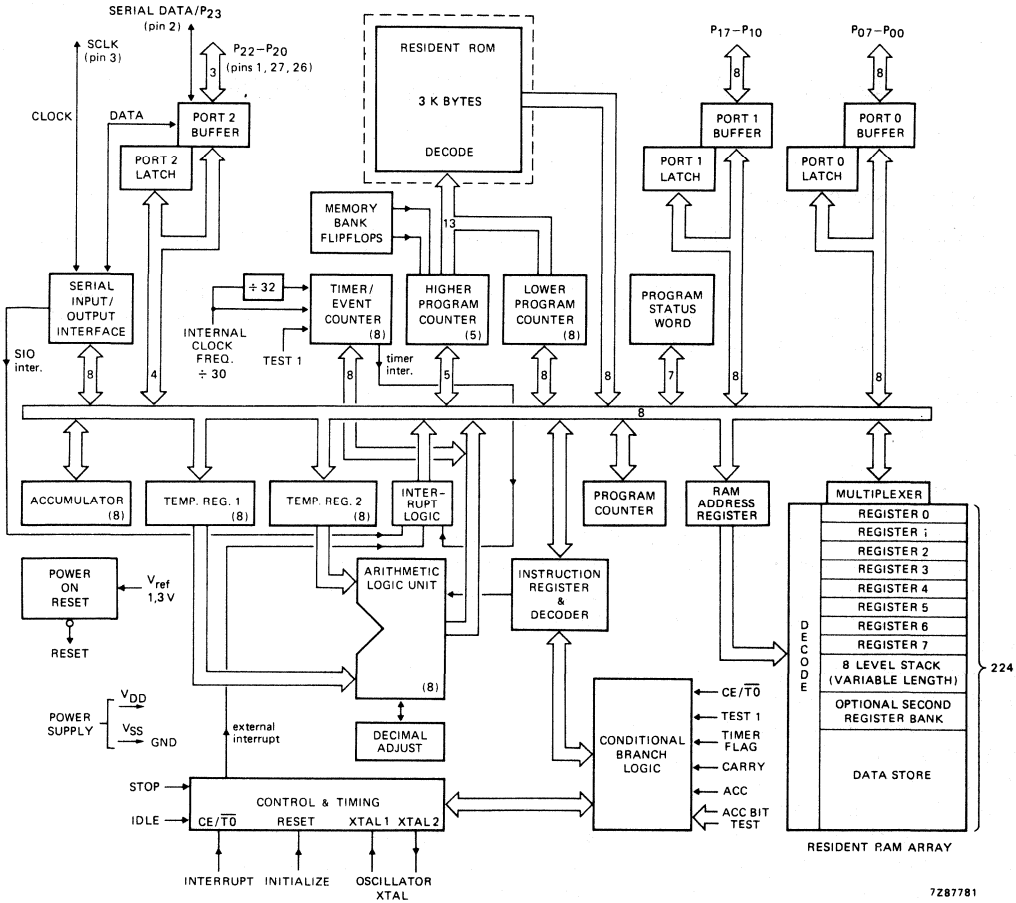
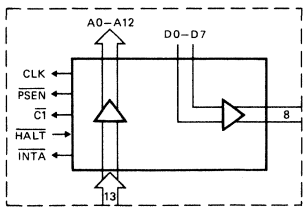
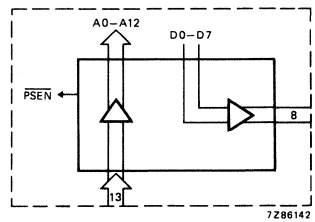


Fig. 1 Block diagram; PCD3343.



(a)

Fig. 1a Replacement of dotted part in Fig. 1, for the PCF8500F bond-out version.

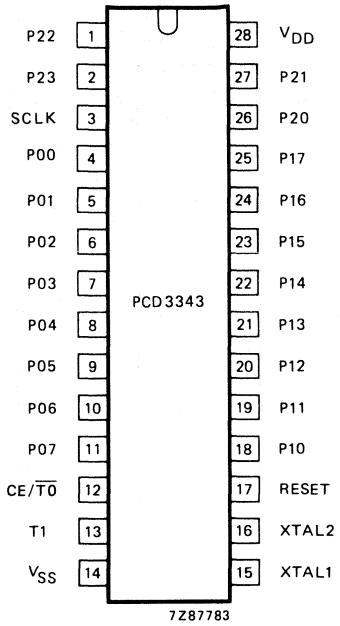


(b)

Fig. 1b Replacement of dotted part in Fig. 1, for the PCF8500B 'Piggy-back' version.

DEVELOPMENT DATA

PINNING



Note CE/$\overline{T0}$ is labelled $\overline{INT}$/T0 on the PCF8500B and has inverted polarity.

Fig. 2 Pinning diagram: PCD3343 and bottom pinning PCF8500B.

PIN DESIGNATION

3	SCLK	**Clock**: bidirectional clock for serial I/O.
4-11	P00-P07	**Port 0**: 8-bit quasi-bidirectional I/O port.
12	CE/$\overline{T0}$	**Interrupt/Test 0**: external interrupt input (sensitive to positive-going edge)/test input pin; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
13	T1	**Test 1**: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
14	V_{SS}	**Ground**: circuit earth potential.
15	XTAL 1	**Crystal input**: connection to timing component (crystal) which determines the frequency of the internal oscillator; also the input for an external clock source.
16	XTAL 2	connection to the other side of the timing component.
17	RESET	**Reset input**: used to initialize the processor (active HIGH), or output of power-on-reset circuit.
18-25	P10-P17	**Port 1**: 8-bit quasi-bidirectional I/O port.
26, 27, 1, 2	P20-P23	**Port 2**: 4-bit quasi-bidirectional I/O port. P23 is the serial data input/output in serial I/O mode.
28	V_{DD}	**Power supply**: 1,8 V to 6 V.

PINNING (continued)

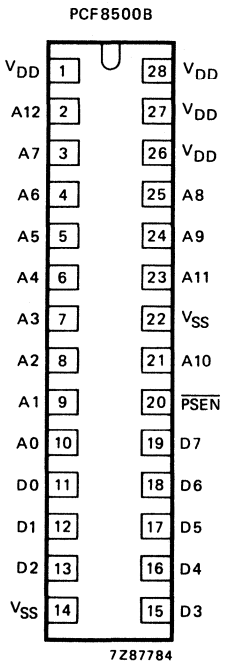


Fig. 3 Pinning diagram: PCF8500B 'Piggy-back' version top pinning; to access a 2732 or 2764 EPROM.

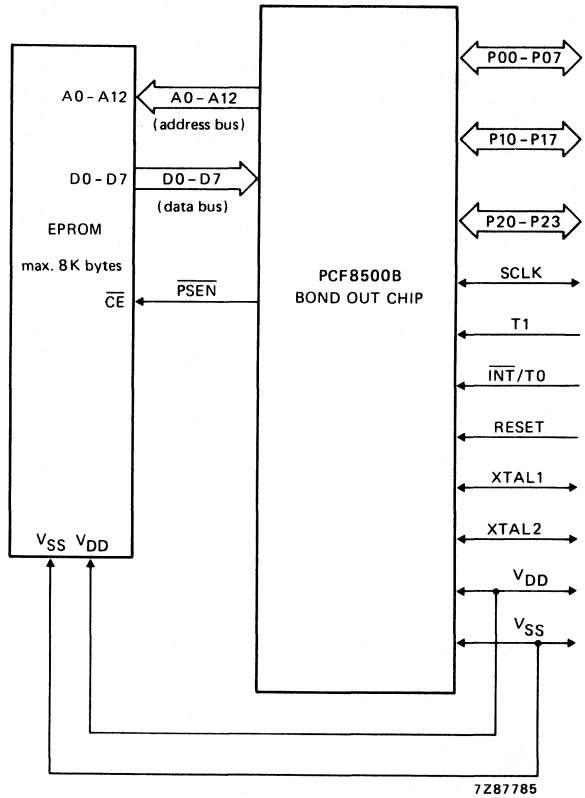


Fig. 3a Connection of EPROM to 'Piggy-back' package PCF8500B.

PIN DESIGNATION

14, 22	V_{SS}	**Ground**
1, 26-28	V_{DD}	**Power supply**
10-3, 25, 24, 21, 23, 2	A0-A12	**Address outputs**
11-13, 15-19	D0-D7	**Data**
20	$\overline{PSEN}$	**Program store enable**

Notes

1. RAM capacity of PCF8500B is 256 bytes.
2. Access time for ROMS/EPROMS to be below 7 x $1/f_{XTAL}$.
3. Pin 12 CE/$\overline{T0}$ is on the PCF8500B, inverted and labelled $\overline{INT}$/T0.

FUNCTIONAL DESCRIPTION

Bond-out version PCF8500F

The PCF8500F is a microcontroller that contains no on-board ROM, but has all address and data lines brought-out to access an external ROM or EPROM. This version has more pins than the PCD3343 with on-board ROM (see Fig. 1a). The RAM has 256 bytes. It can address 8 K bytes of ROM.

'Piggy-back' version PCF8500B

The PCF8500B is a special package that has standard pinning to the bottom which facilitates insertion as a mask-programmed device. An EPROM can be mounted on top in an additional socket. The total package height is greater than the standard DIL package. The RAM has 256 bytes and can also address 8 K bytes of program memory.

Program memory PCD3343

The program memory consists of 3072 bytes (8-bit words), in a read-only memory (ROM). Each location is directly addressable by the program counter. The memory is mask-programmed at the factory. Figure 4 shows the program memory map.

Four program memory locations are of special importance:

- Location 0; contains the first instruction to be executed after the processor is initialized (RESET),
- Location 3; contains the first byte of an external interrupt service subroutine,
- Location 5; contains the first byte of a serial I/O interrupt service subroutine,
- Location 7; contains the first byte of a timer/event counter interrupt service subroutine.

Program memory is arranged in banks of 2 K bytes, which are selected by SEL MB instructions. The program memory is further divided into location 'pages', each of 256 bytes. This latter division applies only for conditional branches. Memory bank boundaries can be crossed only by using the unconditional branch instructions after the appropriate memory bank has been selected. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory PCD3343

Data memory consists of 224 bytes (8-bit words), random-access data memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 5 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

FUNCTIONAL DESCRIPTION (continued)

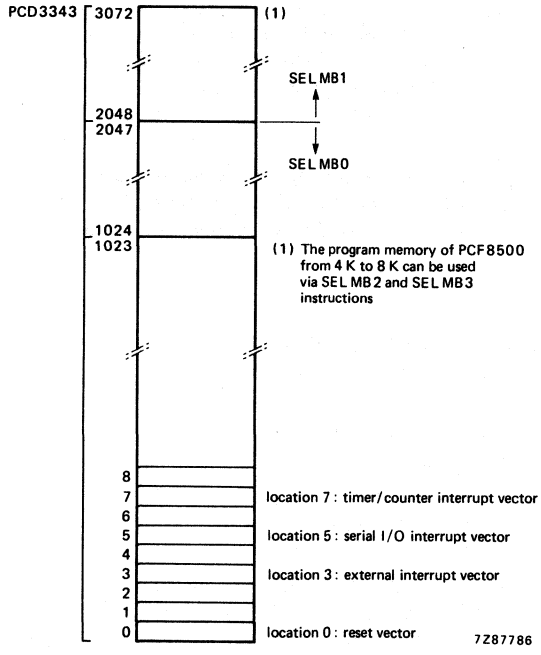


Fig. 4 Program memory map.

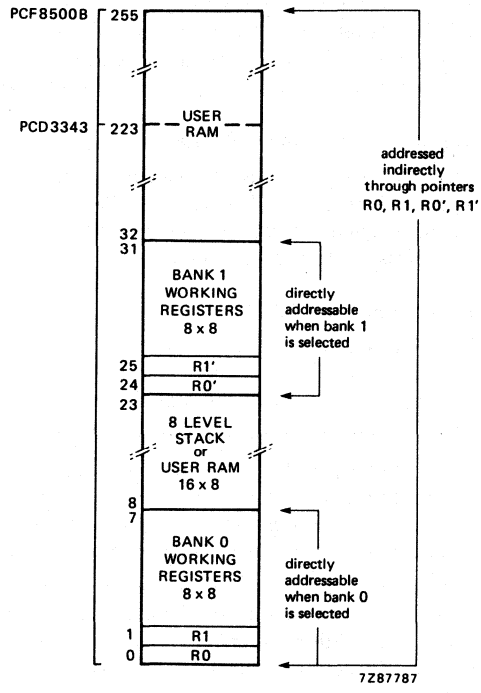


Fig. 5 Data memory map.

Program counter stack

Locations 8 to 23 may be designated as an 8-level program counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Fig. 6) enables the processor to keep track of the return addresses and status generated by interrupts or CALL instructions by storing the contents of the program counter prior to servicing the subroutine. A 3-bit stack pointer determines which of the eight register pairs of the program counter stack will be loaded with next generated return address.

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11 ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If not all 8 levels of subroutine and interrupt nesting are used, the unused portion of the stack may be used as any other indirectly addressable RAM locations. Possible locations from 32 to 223 may be used for storage of program variables or data.

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

The value of the saved contents of the program counter is different for an interrupt CALL compared to a normal CALL to subroutine. With an interrupt CALL, the program counter return address is saved; with a subroutine CALL, the saved program counter value is one less than the program counter return address.

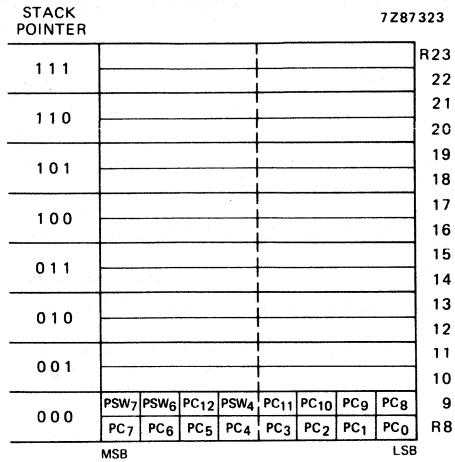


Fig. 6 Program counter stack.

IDLE and STOP modes

IDLE mode

When the microcontroller enters the IDLE mode via the IDLE instruction (H'01') the oscillator, timer/counter and serial I/O are kept running. The microcontroller exits from the IDLE mode by one of three interrupts if they are enabled or by activating a RESET. If the interrupt is not enabled the processor will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig. 7).

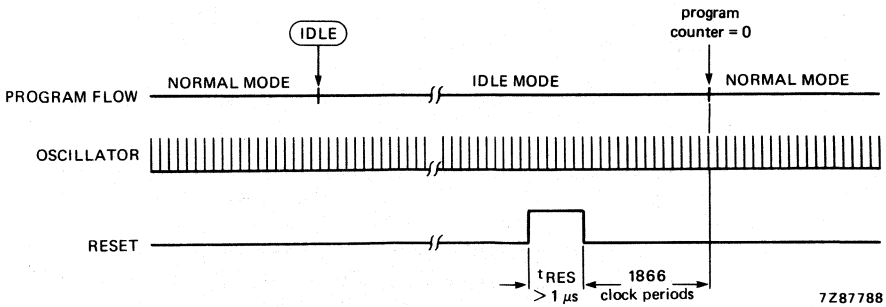


Fig. 7 Exit from IDLE mode via a RESET.

FUNCTIONAL DESCRIPTION (continued)

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A LOW-to-HIGH transition on the external interrupt pin (CE/$\overline{T0}$) reactivates the microcontroller. A HIGH level applied to CE/$\overline{T0}$ will reactivate the microcontroller only in the STOP mode. Thus, if CE/$\overline{T0}$ was HIGH before the microcontroller entered the IDLE mode, it must go LOW before the microcontroller can be reactivated (see Fig. 8).

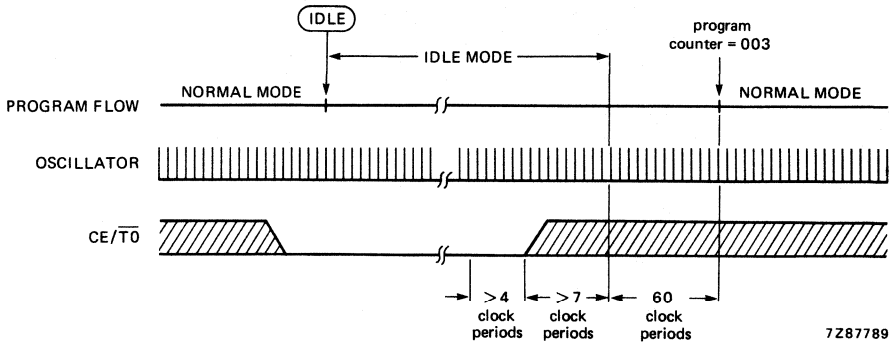


Fig. 8 Exit from IDLE mode via an interrupt.

Wake-up from the IDLE mode is ensured when CE/$\overline{T0}$ is LOW for 4 CP (clock periods) followed by a HIGH for 7 CP. After the initial forced CALL H'003' operation (60 CP) the program continues with the external interrupt service routine.

STOP mode

The microcontroller enters the STOP mode by the STOP instruction (H'22'). The oscillator is switched off. The internal status of the CPU, RAM contents and the state of I/O ports are not affected. The microcontroller can be brought-out of the STOP mode by an active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied an internal delay of 1866 CP is provided to ensure that all internal clocks are operating correctly before restart (see Fig. 9).

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence is executed.

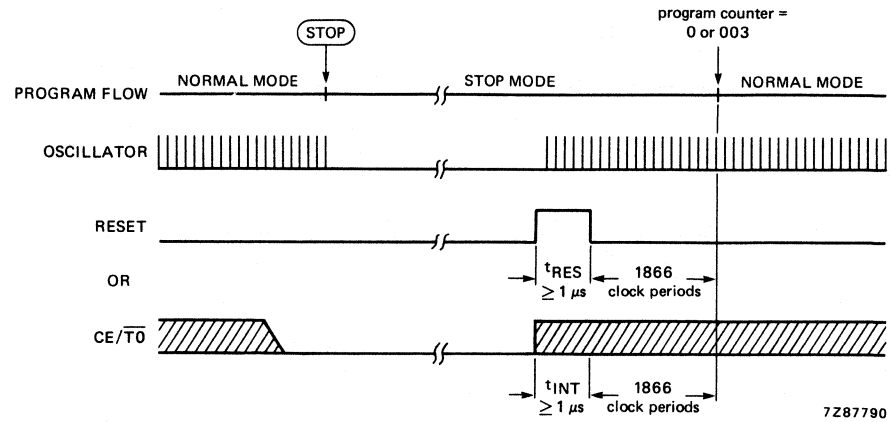


Fig. 9 Entering and exiting the STOP mode.

If the microcontroller exits the STOP mode by pulling the external interrupt input pin HIGH, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence, executing the instruction following the STOP instruction.

The microcontroller is restarted by a HIGH level applied at the CE/$\overline{T0}$ pin, and not by a LOW-to-HIGH transition as in a normal interrupt mechanism.

When the CE/$\overline{T0}$ level is active during the STOP instruction then no STOP is executed.

A HIGH level on the external interrupt input of at least 1 μs will cause the microcontroller to exit the STOP mode.

I/O facilities

The PCD3343 family has 23 I/O lines arranged as:

- Port 0 parallel port of 8 lines (P00 to P07)
- Port 1 parallel port of 8 lines (P10 to P17)
- Port 2 parallel port of 4 lines (P20 to P23)
- SCLK serial I/O consisting of a data line shared with a parallel port line (P23) and a separate clock line SCLK
- CE/$\overline{T0}$ external interrupt and test input. When used as a test input can be directly tested by conditional branch instructions JT0 and JNT0
- T1 test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter.

Parallel ports

All parallel ports can be used as outputs or inputs, their structure is quasi-bidirectional.
Output data written to a port is latched and remains unchanged until rewritten.
Input data is not latched and so must be present until read by an input instruction.

Input lines are fully CMOS compatible, output lines can drive one LS-TTL or CMOS load.

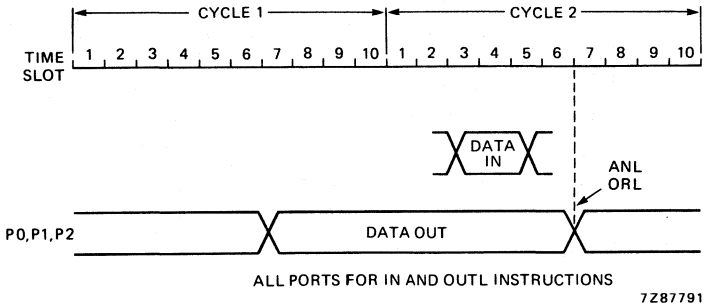


Fig. 10 Timing diagram of all ports on IN and OUTL instructions; for ANL and ORL instructions, the ports change on the time slot 7 of cycle 2.

Fig. 11 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source.
Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current provides sufficient source current for a TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output.

FUNCTIONAL DESCRIPTION (continued)

When a logic 1 is written to the line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period), to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to the port lines will not switch TR2 on. This prevents unnecessary current through external components connected to the port lines of the same port which might be in the input mode and also connected to ground.

When a logic 0 is written to the line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the line, otherwise TR1 will remain low impedance.

In telephone applications this switched pull-up source may not be sufficient. Therefore the PCD3343 offers the possibility to select individually 19 of the 20 parallel port pins (not P23), by the following mask options:

Option 1- STANDARD PORT; quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and P-channel booster transistor TR2 (1,5 mA). TR2 is only active during 1 clock cycle (0,28 μs at 3,58 MHz).

Option 2- OPEN DRAIN; quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig. 12). When an open drain port is unused it must be connected to V_{SS}

Option 3- PUSH-PULL OUTPUT; drive capability of the output will be 1,5 mA (typ.) at V_{DD} = 3 V in both polarities. To avoid a large current flowing through the output transistors during the input mode, these push-pull pins must only be used as outputs (Fig. 13).

Also, individual mask selection of the RESET state of these port pins can be achieved by appending the following options S and R to options 1, 2 or 3.

Option S-SET; after RESET this pin will be initialized to HIGH.

Option R-RESET; after RESET this pin will be initialized to LOW.

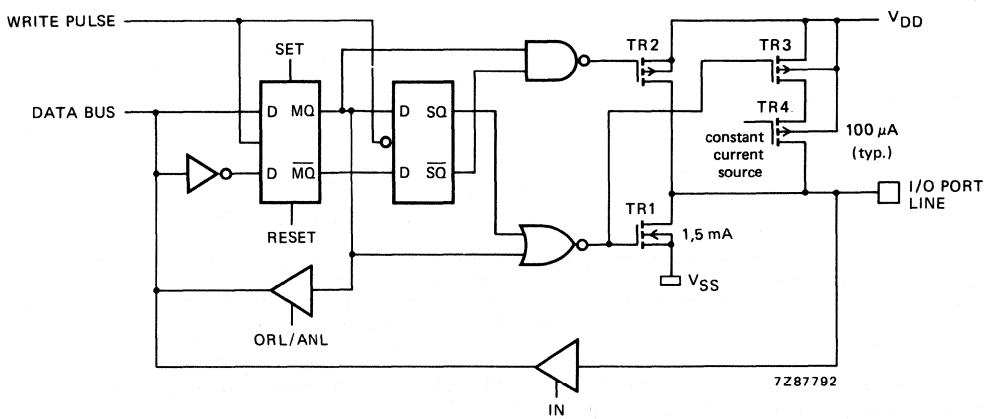


Fig. 11 Standard output with switched pull-up current source.

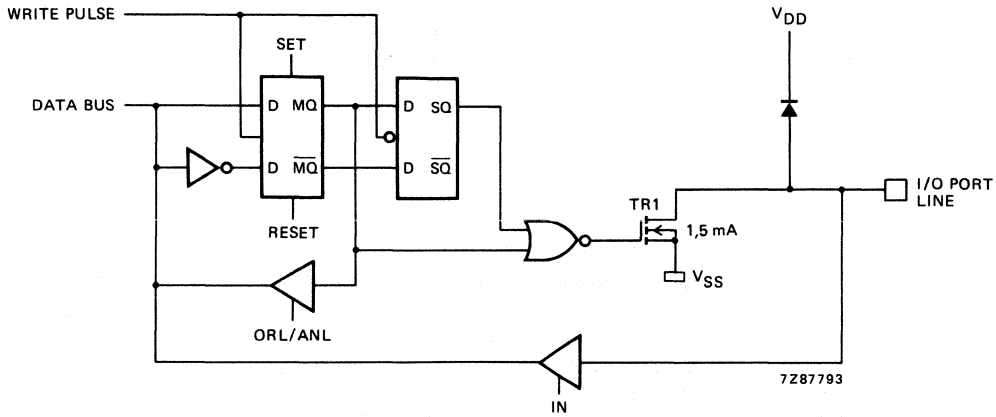


Fig. 12 Open drain output.

DEVELOPMENT DATA

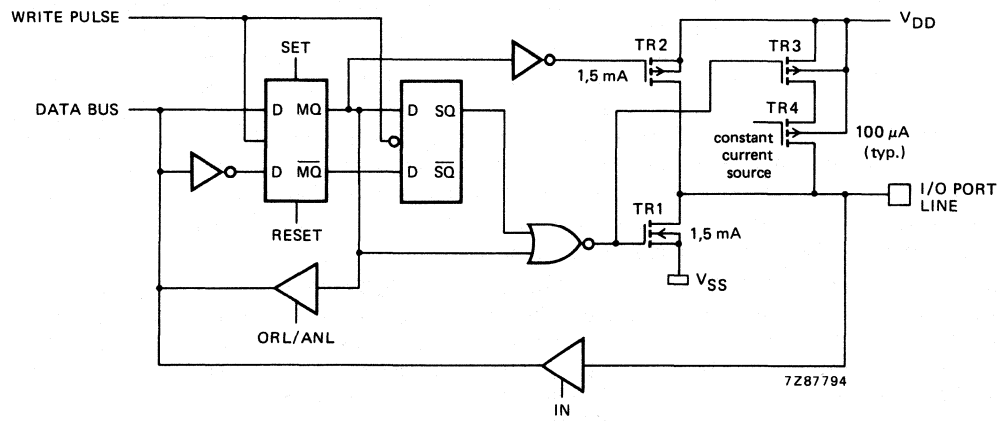


Fig. 13 Push-pull output.

FUNCTIONAL DESCRIPTION (continued)

Serial I/O (SIO)

The PCD3343 has an on-chip serial I/O interface. This SIO interface is a versatile feature in an intelligent telephone set, as shown in application diagram Fig. 32.

In this application the SIO is used to communicate with the different peripherals, such as:

- DTMF generator (PCD3312)
- LCD drivers (PCF8577)
- External RAM (PCD8571)
- Clock calendar (PCB8573)

No extra hardware is required for decoding, addressing and data processing.

Whereas a normal microcontroller must regularly monitor the serial data bus for the presence of data, the serial I/O interface detects, receives and converts the serial data stream into parallel format without interrupting the execution of the current program. An interrupt is sent to the PCD3343 only when a complete byte is received. It then reads the data byte in one instruction. Likewise during transmission the serial I/O interface performs parallel to serial conversion and subsequent serial output of the data. The microcontroller is only interrupted in the execution of its programmed tasks when a complete byte has been transmitted.

The design of the PCD3343 serial I/O system allows any number of devices from PCF8500 family (clips) to be connected via the two-line serial bus. The ability of any devices to communicate, without interrupting the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to a message prefixed with its own address or the 'general CALL' address. Address recognition is performed by the interface hardware so that operation of the microcontroller need only be interrupted when a valid address has been received. This saves significant processing time and memory space compared with a conventional microcontroller employing a software serial interface. When the addressing facility is not required, for instance in a system with only two microcontrollers, direct data transfer without addressing can be performed. In multi-master systems, an automatically invoked arbitration procedure prevents two or more devices from continuing simultaneous transmission.

In NORMAL (running) and IDLE mode, the serial I/O logic remains active; its internal system clock will be switched off when there is no activity on the serial bus.

After execution of the STOP instruction, the oscillator of the PCD3343 is switched off. This means that the serial I/O logic will remain in the state it was at the occurance of the STOP instruction. To avoid "bus block" problems and to assure correct start-up of the bus after exit from the STOP mode, the user should disable the serial logic (ESO = 0) prior to the execution of the STOP instruction. This must be carried out only when the PCD3343 has finished a serial data transfer.
After a negative RESET signal the first 30 clock pulses of the 1866 pulse initialization phase set P23/SDA and SCLK HIGH. When P23/SDA or SCLK are not used, they must be connected to V_{SS}.

Serial I/O interface

Figure 14 shows the serial I/O interface. The clock line of the serial bus has exclusive use of pin 3 (SCLK) while the data line shares pin 2 (serial data) with the I/O line P23 of port 2. When the serial I/O is enabled, P23 is disabled as a parallel port line; (P23 and SCLK only open drain).

The microcontroller and interface communicate via the internal microcontroller bus and the Serial Interrupt Request line. Data and information controlling the operation of the interface are stored in four registers:

- Data shift register (S0)
- Serial I/O interface status word (S1)
- Serial clock control word (S2)
- Address register

Data shift register (S0)

Register S0 converts serial data to parallel format and vice versa. A pending interrupt is generated only after a complete byte has been transmitted, or after a complete data byte, specific address or 'general CALL' address has been received. The most significant bit is transmitted first.

Serial I/O interface status word (S1)

Register S1 provides information concerning the state of the interface and stores information from the microcontroller. Bits 0 to 3 are duplicated: control bits in these positions can only be written by the microcontroller, while interface bits can only be read.

MST and TRX (see Table 1)

These bits determine the operating mode of the serial I/O interface.

Table 1 Operating modes of the serial I/O interface

MST	TRX	operating mode
0	0	slave receiver
1	0	master receiver
0	1	slave transmitter
1	1	master transmitter

BB: Bus Busy.

This is the flag which indicates the status of the bus.

PIN: Pending Interrupt Not

PIN = '0' indicates the presence of a pending interrupt, which will cause a Serial Interrupt Request when the serial interrupt mechanism is enabled.

ESO: Enable Serial output

The ESO flag enables/disables the serial I/O interface: ESO = '1' enables, ESO = '0' disables. ESO can only be written by software.

BC0, BC1 and BC2

Bits BC0, BC1 and BC2 indicate the number of bits received or transmitted in a data stream. These bits can only be written by software.

AL: Arbitration Lost

The arbitration lost flag is set by hardware when the serial I/O interface, as master transmitter, loses a bus arbitration procedure.

AAS: Addressed As Slave

This flag is set by hardware when the interface detects either its own specific address or the 'general CALL' address as the first byte of a transfer and the interface has been programmed to operate in the address recognition mode.

AD0: Address Zero

This flag is set by hardware after detection of the 'general CALL' address when the interface is operating in the address recognition mode.

LRB: Last Received Bit

This contains either the last data bit received or, for a transmitting device in the acknowledgement mode, the acknowledgement signal from the receiving device.

Bits AL, AAS, AD0 and LRB can only be read by software.

FUNCTIONAL DESCRIPTION (continued)

Serial clock control word (S2)

Bits 0 to 4 of the clock control register S2 are used to set the frequency of the serial clock signal. When a 3,58 MHz crystal is used, the frequency of the serial clock can be varied between 92 kHz and 580 Hz (see Table 2). An asymmetrical clock with a HIGH-to-LOW ratio of 3 : 1 can be generated using bit 5. The asymmetrical clock allows a microcontroller more time per clock period for sampling the data line, making the timing of this action less critical. Bit 6 can be used to activate the acknowledge mode of the serial I/O. S2 is a write only register.

Address register

The address register contains the 7-bit address back-up latches and the bit (ALS) used to enable/disable the address recognition mode. The address register can be written using the MOV S0, A and MOV S0, # data instructions, but only when ES0 = '0'.

Serial I/O interrupt logic

An EN SI instruction enables and a DIS SI instruction disables the interrupt logic. When the logic is enabled, a pending interrupt results in a serial I/O interrupt to the processor, causing a CALL to location 5 in the ROM. When disabled, the presence of an interrupt is still indicated by PIN in S1, allowing the interrupt to be serviced. However, vectored interrupt will not occur.

DEVELOPMENT DATA

Table 2 SIO clock pulse frequency control when using a 3,58 MHz crystal

hexadecimal S20-S24 code	divisor	f_{SCLK} (kHz) (approximate)
0	not allowed	
1	39	92
2	45	80
3	51	70
4	63	57
5	75	48
6	87	41
7	99	36
8	123	29
9	147	24
A	171	21
B	195	18
C	243	15
D	291	12
E	339	11
F	387	9,2
10	483	7,4
11	579	6,2
12	675	5,3
13	771	4,6
14	963	3,7
15	1155	3,1
16	1347	2,7
17	1539	2,3
18	1923	1,9
19	2307	1,6
1A	2691	1,3
1B	3075	1,2
1C	3843	0,93
1D	4611	0,78
1E	5379	0,67
1F	6147	0,58

FUNCTIONAL DESCRIPTION (continued)

Table 3 Serial I/O addresses for telephony peripherals

type	address 7	6	5	4	3	2	1	0	description
PCF8570A	1	0	1	0	A2	A1	X	R/$\overline{W}$	2 K RAM
PCF8570	1	0	1	0	A2	A1	A0	R/$\overline{W}$	2 K RAM
PCD8571	1	0	1	0	A2	A1	A0	R/$\overline{W}$	1 K RAM
PCD3311	0	1	0	0	1	0	A0	R/$\overline{W}$	DTMF dialler
PCD3312	0	1	0	0	1	0	A0	R/$\overline{W}$	DTMF dialler
PCE2111	0	0	0	0	0	0	1	0	LCD driver *
PCD8573	1	1	0	1	0	A1	A0	R/$\overline{W}$	clock calendar
PCF8574	0	0	1	1	A2	A1	A0	R/$\overline{W}$	8-bit I/O expander
PCF8576	0	1	1	1	0	0	SA0	R/$\overline{W}$	1 : 4 LCD driver
PCF8577	0	1	1	1	0	1	0	R/$\overline{W}$	1 : 2 LCD driver

* LCD driver requires an additional enable line.

DEVELOPMENT DATA

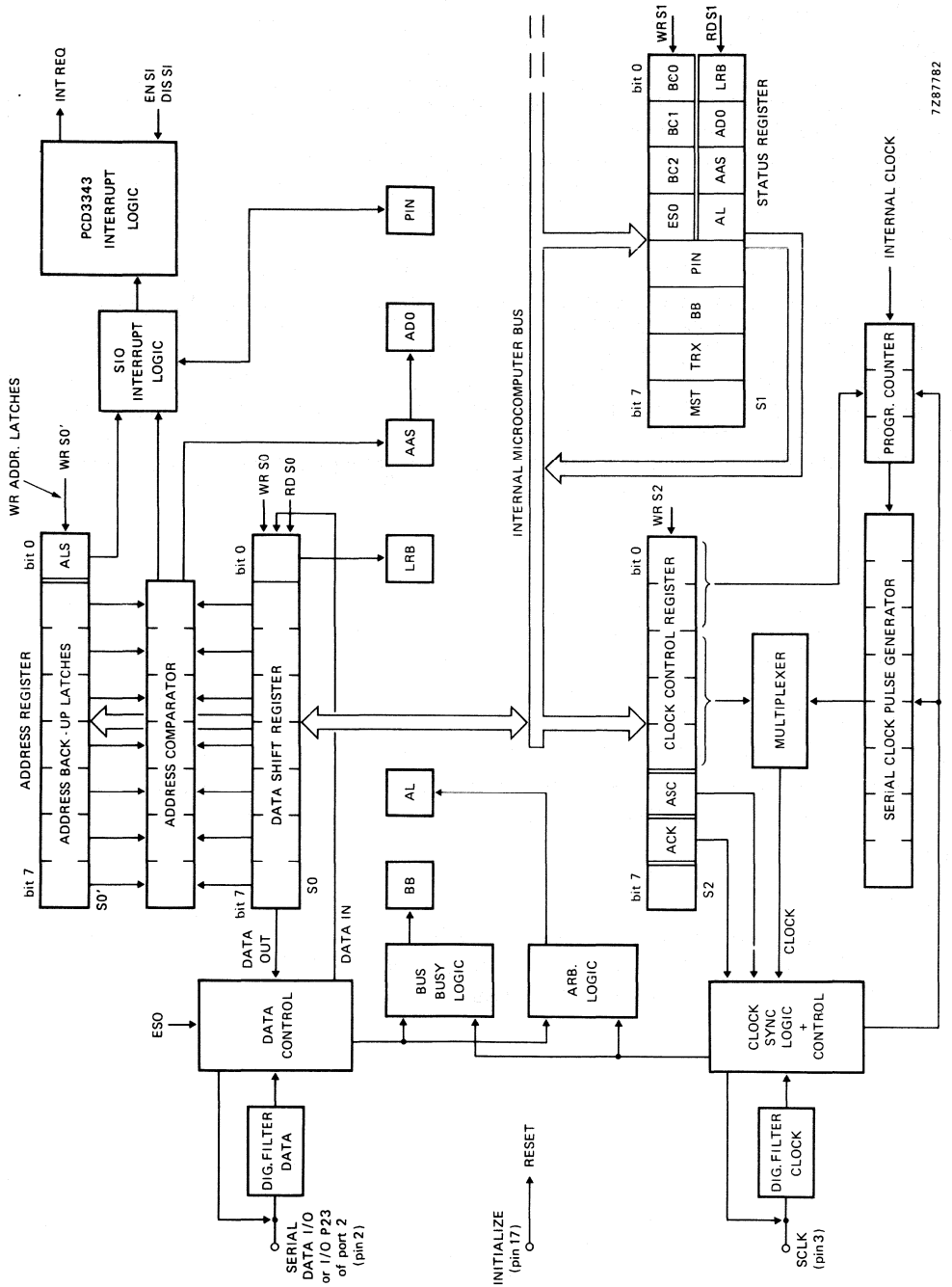


Fig. 14 Serial I/O interface.

FUNCTIONAL DESCRIPTION (continued)

Interrupts (see Fig. 15)

When the external interrupt is enabled, a LOW-to-HIGH transition on the CE/$\overline{T0}$ input initiates an external interrupt subroutine which causes a CALL to program memory location 3 following completion of the current instruction.
The interrupt must remain enabled until the interrupt instruction is completed, otherwise the next instruction of the main program will be executed. Serial I/O interrupt, when enabled, causes a CALL to location 5, and a timer/event counter overflow forces a CALL to location 7 when the timer interrupt is enabled.

When an interrupt subroutine starts, the contents of the program counter and bits 4, 6 and 7 of the PSW have been saved in the program counter stack. Accumulator contents have to be saved by software. Interrupt acknowledgement can be carried out by software via port pins. All interrupt subroutines must reside in memory bank 0.

Since the interrupt system is single level, once an interrupt is detected, all further interrupt requests are latched, but ignored, pending a RETR instruction to re-enable the interrupt input logic. After executing RETR, the program continues in the main part; this is independent of the occurance of a second interrupt during the running of the first routine. If 2 or 3 interrupts occur simultaneously, their priority is:

- (1) external
- (2) serial I/O
- (3) timer/event counter

An external interrupt can be generated by using the timer/counter in the event counter mode. The counter is first preset to (H'FF'), then EN TCNTI instruction is executed. A LOW-to-HIGH transition of the T1 input will then initiate an interrupt subroutine and cause a CALL to location 7.

On execution of a DIS I instruction, the PCD3343 always clears the digital filter/latch and the External Interrupt Flag.

The Timer Flag (TF) is reset only when the JTF or JNTF instruction is executed or after RESET.

The Timer Interrupt Flag is set when timer overflow occurs, only if the timer interrupt is enabled.

The microcontroller will exit the IDLE mode when any one of the following three interrupts is enabled:

- External
- Serial I/O
- Timer/event counter

There is no internal pull-up or pull-down device connected to the external interrupt input (pin 12). If required pin 12 must be externally connected to a resistor ($R \leqslant 100\ k\Omega$). When the external interrupt is not used pin 12 must be connected to V_{SS}.

DEVELOPMENT DATA

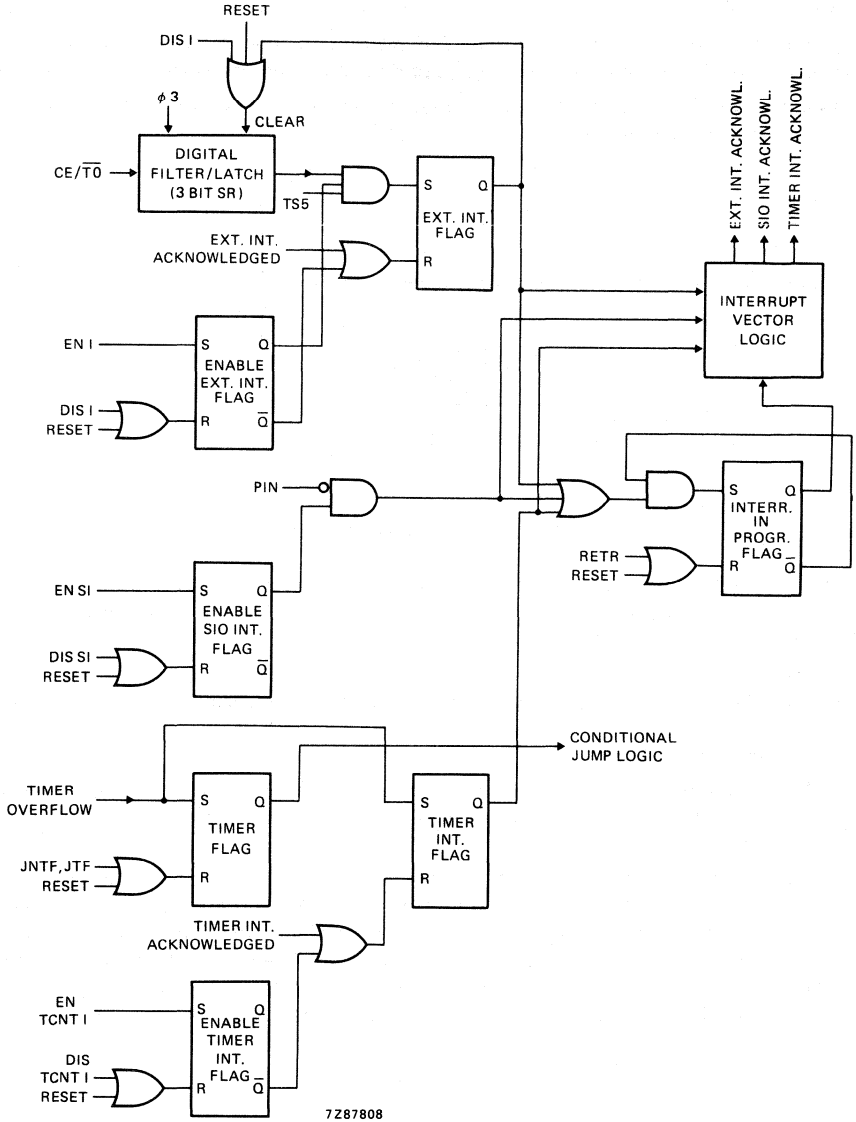


Fig. 15 Interrupt logic.

Notes to figure 15

1. CE/$\overline{T0}$ positive edge is always latched in the digital filter/latch.
2. Correct interrupt timing in ensured when CE/$\overline{T0}$ is LOW for >4 CP followed by a HIGH for >7 CP.
3. When the interrupt in progress flag is set, further interrupts are latched but ignored, until RETR is executed.
4. A DIS I instruction always clears a pending external interrupt.

FUNCTIONAL DESCRIPTION (continued)

Oscillator (see Fig. 16)

The 3,58 MHz oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-voltage condition is present to prevent discharge of a weak back-up battery.

Provided the supply voltage is within the operating range, the oscillator will be restarted after a STOP instruction by a HIGH level at either the CE/$\overline{T0}$ or RESET pin.

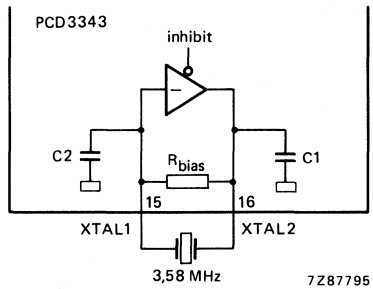


Fig. 16 Oscillator with integrated elements.

The oscillator has the output drive capability for the DTMF generator (PCD3311/3312) via pin 16 (XTAL 2). An external clock can be applied to pin 15 (XTAL 1). A machine cycle consists of 10 time slots, each time slot being 3 oscillator periods.

In telephony applications the 3,58 MHz crystal provides a 8,4 μs machine cycle. The range of the clock frequency is from 100 kHz up to a maximum which is a function of the supply voltage (see Fig. 23).

Timer/event counter (see Fig. 17)

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 4 gives the instructions that control the counter and the prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW-to-HIGH transitions on pin 13 (T1) are counted. The maximum rate at which the counter may be incremented is once every machine cycle (182,6 kHz for a 8,4 μs machine cycle). When the counter overflows, the timer flag is set. The flag can be tested and reset using the JTF (jump if timer flag = 1) or JNTF instruction. Overflow also generates an interrupt to the processor via setting of the Timer Interrpt Flag when the timer/event counter interrupt is enabled.

Table 4 Timer/event counter control

function	timer mode modulo-1, modulo-32*	counter mode
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ**	MOV A,T	MOV A,T

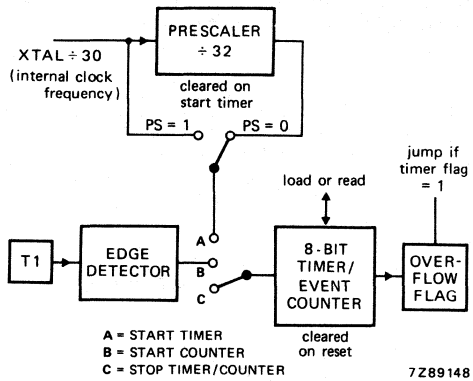


Fig. 17 Timer/event counter.

DEVELOPMENT DATA

Program status word (see Fig. 18)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.
The PSW bits are:

- Bits 0 to 2 — stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 — prescaler select (PS);
  0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 — working register bank select (RBS);
  0 = register bank 0; 1 = register bank 1
- Bit 5 — not used (1)
- Bit 6 — auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 — carry (CY); the carry flag indicates that previous operation has resulted in an overflow of the accumulator.

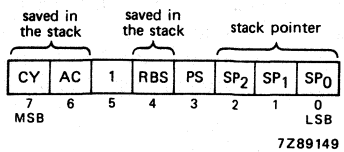


Fig. 18 Program status word.

* With prescaler select, PS = 0, the timer counts modulo-32 machine cycles, with PS = 1 it counts modulo-1 cycles (prescaler not used); prescaler cleared with STRT T, prescaler not readable.

** READ does not disturb the counting process.

FUNCTIONAL DESCRIPTION (continued)

Program status word (continued)

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by a SEL RB instruction, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions and in the event of an interrupt. Bits 7, 6 and 4 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt and can be used at the end of a normal subroutine. The RET instruction has no restore feature and cannot be used at the end of an interrupt.

Program counter (see Fig. 19)

A 13-bit program counter is used to facilitate 8 K bytes of ROM being addressed. The arrangement of the bits is shown in figure 19. During an interrupt subroutine PC_{11} and PC_{12} are forced to logic 0. All 13 bits are saved in the stack during CALL and interrupt routines.

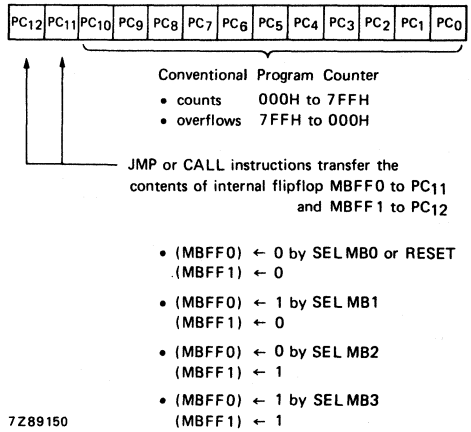


Fig. 19 Program counter.

Central processing unit

The PCD3343 has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the current ROM page.

Conditional branch logic

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program. Table 5 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Table 5 Conditional branches

test	jump condition	jump instruction
accumulator	all bits zero	JZ
	any bit non-zero	JNZ
accumulator bit test	1	JB0 to JB7
carry flag	1	JC
	0	JNC
timer overflow flag	1	JTF
	0	JNTF
test input T0	1	JNT0
	0	JT0*
test input T1	1	JT1
	0	JNT1
register	non-zero	DJNZ

Test input T1 (pin 13)

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for $>$ 4 CP, followed by a HIGH for $>$ 4 CP. The transition can be recognized with a repetition rate of once per 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. If required it must be externally connected to a resistor ($R = \leqslant 100\ k\Omega$). When T1 is not used pin 13 must be connected to V_{DD} or V_{SS}.

Reset (pin 17)

A positive-going signal on the RESET input/output:

- Sets the program counter to zero
- Selects location 0 of memory band 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external, timer and serial I/O)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to modulo-32
- Resets the timer flag
- Sets all ports according to reset states
- Sets all ports except P23 to reset state *(see Serial I/O)*
- Cancels IDLE and STOP mode

A negative-going signal on the RESET input/output:

- Sets P23/SDA and SCLK to HIGH after a maximum of 30 clock pulses
- Sets the serial I/O to slave receiver mode and disables the serial I/O after 1866 clock pulses
- Starts an internal delay of 1866 clock pulses after which the microcontroller commences operation.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Power-on-reset and low-voltage detection (see Fig. 20)

In telephony applications, correct operation of the PCD3343 during moments of slowly changing supply voltages and low-voltage conditions is essential. This is achieved by the addition of an internal power-on-reset and low-voltage detection circuit.
To allow an external RESET signal being fed into the PCD3343, the reset pin (pin 17) has been configured as an input/output.

While a reset condition exists in the detection circuit, pin 17 is pulled HIGH by TR1 controlled by the reset circuit.
When the reset condition is not present a pull-down current source (TR2) will be activated. TR2 forces pin 17 LOW thus removing the RESET signal from the microcontroller.

Since the level at pin 17 is recognized by the microcontroller, the reset time constant can be stretched by connecting an external capacitor between V_{DD} and pin 17 (see Fig. 22).

The signal at pin 17 can also be used as an output to reset other devices in the system.

The internal reset circuit monitors the PCD3343 supply voltage. If the voltage drops below the switching level (typ. 1,3 V), a reset (HIGH) is applied to pin 17. This reset is removed (pin 17 goes LOW), after a fixed delay (t_d), when the supply voltage rises above the switching level again. The delay ensures a complete reset even when the supply voltage quickly rises above switching level after initial switch-on.

During a low-voltage condition the oscillator is inhibited to prevent complete discharge of a weak battery. The timing of the power-on-reset and low-voltage detection circuit is shown in figure 21.

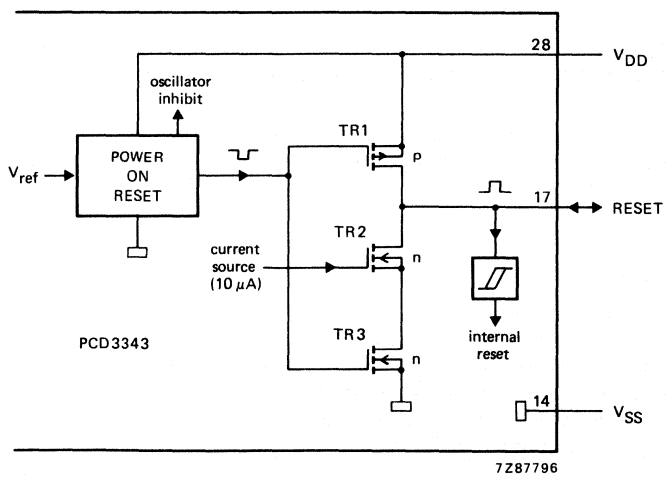
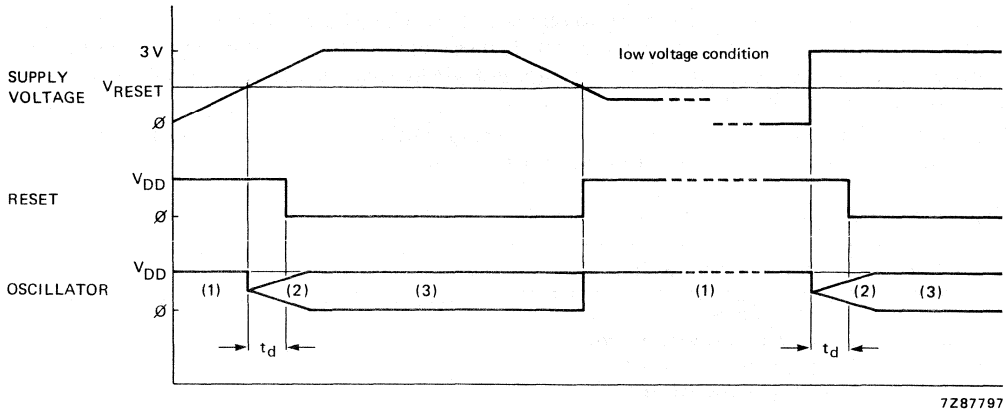


Fig. 20 Power-on-reset configuration.



Where: (1) Oscillator inhibited
(2) Oscillator starting
(3) Oscillator running, but may be stopped with a STOP condition

Fig. 21 Timing of power-on-reset and low-voltage detection.

DEVELOPMENT DATA

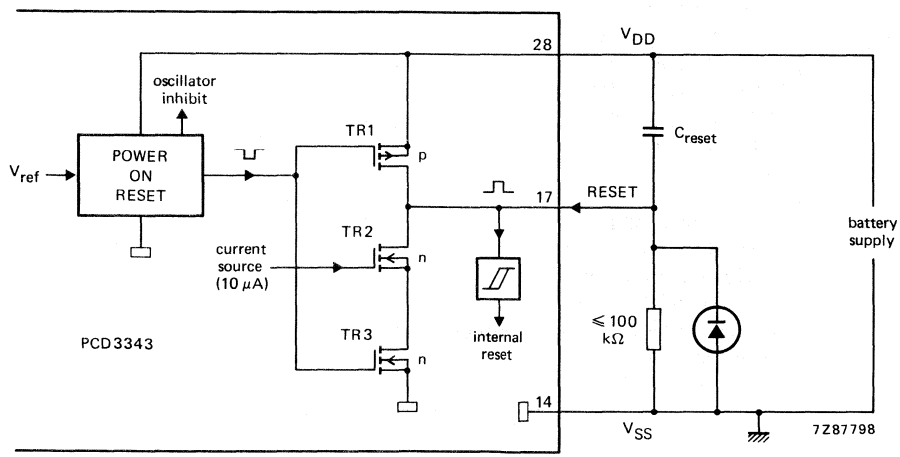


Fig. 22 Stretched power-on-reset with external capacitor.

INSTRUCTION SET

The PCD3343 instruction set consists of over 80 one and two byte instructions and is based on the MAB8048 instruction set. New instructions include those for serial I/O operation and memory bank selection. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 8 gives the instruction set of the PCD3343. Table 7 shows the instruction map and Table 6 details the symbols and definition descriptions that are used.

Table 6 Symbols and definitions used in Table 8

symbol	definition description
A	accumulator
addr	program memory address
Bb	bit designation (b = 0-7)
RBS	register bank select
C	carry bit (bit CY)
CNT	event counter
D	mnemonic for 4-bit digit (nibble)
data	8-bit number or expression
I	interrupt
MB	memory bank
MBFF	memory bank flip-flop
P	mnemonic for 'in-page' operation
PC	program counter
Pp	port designation (p = 0, 1 or 2)
PSW	program status word
RB	register bank
Rr	register designation (r = 0-7)
Sn	serial I/O register
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with

Table 7 PCD3343 instruction map

first hexadecimal character of opcode ↓ / second hexadecimal character of opcode →	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A,#data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0 1 2				MOV A,Sn 0 1			
1	INC @Rr 0 1		JBO addr	ADDC A,#data	CALL page 0	DIS I	JTF addr	INC A	INC Rr 0 1 2 3 4 5 6 7							
2	XCH A,@Rr 0 1		STOP	MOV A,#data	JMP page 1	EN TCNTI	JNTO addr	CLR A	XCH A,Rr 0 1 2 3 4 5 6 7							
3	XCHD A,@Rr 0 1		JB1 addr		CALL page 1	DIS TCNTI	JTO addr	CPL A	OUTL Pp,A 0 1 2				MOV Sn,A 0 1 2			
4	ORL A,@Rr 0 1		MOV A,T	ORL A,#data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr 0 1 2 3 4 5 6 7							
5	ANL A,@Rr 0 1		JB2 addr	ANL A,#data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr 0 1 2 3 4 5 6 7							
6	ADD A,@Rr 0 1		MOV T,A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr 0 1 2 3 4 5 6 7							
7	ADDC A,@Rr 0 1		JB3 addr		CALL page 3			RR A	ADDC A,Rr 0 1 2 3 4 5 6 7							
8				RET	JMP page 4	EN SI			ORL Pp,#data 0 1 2							
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,#data 0 1 2				MOV Sn,#data 0 1 2			
A	MOV @Rr,A 0 1			MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A 0 1 2 3 4 5 6 7							
B	MOV @Rr,#data 0 1		JB5 addr	JMPP @A	CALL page 5	SEL MB3			MOV Rr,#data 0 1 2 3 4 5 6 7							
C	DEC @Rr 0 1				JMP page 6	SEL RB0	JZ addr	MOV A,PSW	DEC Rr 0 1 2 3 4 5 6 7							
D	XRL A,@Rr 0 1		JB6 addr	XRL A,#data	CALL page 6	SEL RB1		MOV PSW,A	XRL A,Rr 0 1 2 3 4 5 6 7							
E	DJNZ @Rr,addr 0 1				JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr 0 1 2 3 4 5 6 7							
F	MOV A,@Rr 0 1		JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr 0 1 2 3 4 5 6 7							

INSTRUCTION SET (continued)

Table 8 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) −1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

DEVELOPMENT DATA

ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1}) \leftarrow A_n$ $(A_0) \leftarrow (C), (C) \leftarrow (A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (C), (C) \leftarrow (A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7}) \leftrightarrow (A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data		
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3}) \leftrightarrow ((R0_{0-3}))$ $(A_{0-3}) \leftrightarrow ((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3) \leftarrow (A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7}) \leftarrow (A), (A) \leftarrow ((PC))$		
FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1 r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1	
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1 r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1	
BRANCH	JMP addr	• 4 address	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))	
	DJNZ Rr, addr	E* address	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 r = 0–7 if (Rr) not zero (PC_{0-7})←addr	
	DJNZ @Rr, addr	E0	2/2	decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr	
		E1			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr	
	JBb addr	▲ 2 address	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr b = 0–7	
	JC addr	F6 address	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr	
	JNC addr	E6 address	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr	
	JZ addr	C6 address	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr	
	JNZ addr	96 address	2/2	jump to addr if A is NOT zero	if A≠0 : (PC_{0-7})←addr	
	JT0 addr	36 address	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr	
	JNT0 addr	26 address	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr	
	JT1 addr	56 address	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr	
	JNT1 addr	46 address	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr	
	JTF addr	16 address	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr	4
	JNTF addr	06 address	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr	

TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
	STOP	22	1/1	enter STOP mode		
	IDLE	01	1/1	enter IDLE mode		
SUBROUTINE	CALL addr	▲ 4 address	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4,6,7}$) 6 (SP)←(SP) + 1 (PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) – 1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) – 1 ($PSW_{4,6,7}$) + (PC)←((SP))	6

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 99 9A	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 89 8A	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
SERIAL INPUT/OUTPUT	MOV A, S_n	0C 0D	1/2	move serial I/O register contents to accumulator	(A)←(S0) (A)←(S1)	8
	MOV S_n, A	3C 3D 3E	1/2	move accumulator contents to serial I/O register	(S0)←(A) (S1)←(A) (S2)←(A)	9
	MOV S_n, #data	9C 9D 9E	2/2	move immediate data to serial I/O register	(S0)←data (S1)←data (S2)←data	
	EN SI	85	1/1	enable serial I/O interrupt		
	DIS SI	95	1/1	disable serial I/O interrupt		
	NOP	00	1/1	no operation		

Notes to Table 8

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF).

* : 8, 9, A, B, C, D, E, F
● : 0, 2, 4, 6, 8, A, C, E
▲ : 1, 3, 5, 7, 9, B, D, F

5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 1111 P23, P22, P21, P20.
8. (S1) has a different meaning for read and write operation, see serial I/O interface.
9. (S2) is a write only register. Reading S2 will give value FFH.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 28)	V_{DD}		−0,8 to + 8	V
All input voltages	V_I	0,8 to V_{DD} + 0,8		V
D.C. current into any input or output	$\pm I_I, \pm I_O$	max.	10	mA
Total power dissipation (see note)	P_{tot}	max.	500	mW
Power dissipation per output				
except P23, SCLK	P_O	max.	50	mW
P23, SCLK	P_O	max.	180	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 70	°C
Operating junction temperature	T_j	max.	125	°C

Note

Thermal resistance (junction to ambient)				
for SOT-117	$R_{th\ j\text{-}a}$	max.	120	K/W
for SOT-135A	$R_{th\ j\text{-}a}$	max.	60	K/W
for SOT-136A	$R_{th\ j\text{-}a}$	max.	150	K/W

DEVELOPMENT DATA

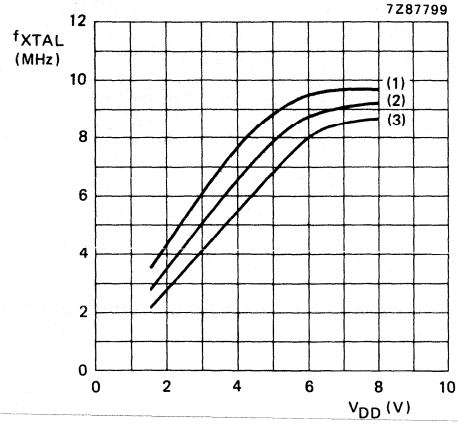
D.C. CHARACTERISTICS

V_{DD} = 2,75 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; f = 3,58 MHz with R_S = 50 Ω; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating (see Fig. 23)	V_{DD}	1,8	–	6	V
STOP mode for RAM retention	V_{DD}	1,0	–	6	V
Supply current					
operating					
at V_{DD} = 3 V (see Fig. 24)	I_{DD}	–	600	–	μA
IDLE mode					
at V_{DD} = 3 V (see Fig. 25)	I_{DD}	–	300	–	μA
STOP mode (see Fig. 26 and note 1)					
at V_{DD} = 1,8 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 1,8 V; T_{amb} = 55 °C	I_{DD}	–	–	5	μA
at V_{DD} = 1,8 V; T_{amb} = 70 °C	I_{DD}	–	–	10	μA
RESET I/O					
Switching level	V_{RESET}	–	1,3	–	V
Sink current					
at $V_{DD} > V_{RESET}$	I_{OL}	–	7	–	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current					
at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at $V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 3 V; V_O = 0,4 V					
except P23/SDA, SCLK (see Fig. 27)	I_{OL}	0,75	1,5	–	mA
P23/SDA, SCLK (see Fig. 28)	I_{OL}	1,5	–	–	mA
Pull-up output source current HIGH (see Fig. 29)					
at V_{DD} = 3 V; $V_O = 0{,}9V_{DD}$	$-I_{OH}$	25	–	–	μA
at V_{DD} = 3 V; $V_O = V_{SS}$	$-I_{OH}$	–	–	200	μA
Push-pull output source current HIGH					
at V_{DD} = 3 V; $V_O = V_{DD}-0{,}4$ V	$-I_{OH}$	0,75	1,5	–	mA

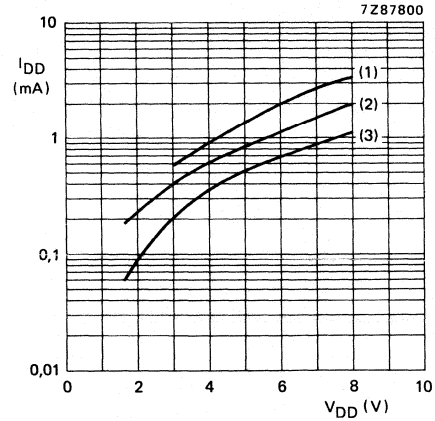
Note 1

Crystal connected between XTAL 1 and XTAL 2; SCL and SDA pulled to V_{DD} via 5,6 kΩ resistor; CE and T1 at V_{SS}.



(1) $T_{amb} = -25\ ^{o}C$
(2) $T_{amb} = 25\ ^{o}C$
(3) $T_{amb} = 70\ ^{o}C$

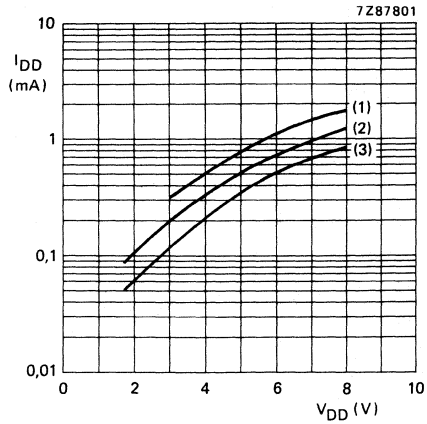
Fig. 23 Maximum clock frequency (f_{XTAL}) as a function of the supply voltage (V_{DD}).



(1) clock frequency = 4 MHz
(2) clock frequency = 2 MHz
(3) clock frequency = 500 kHz

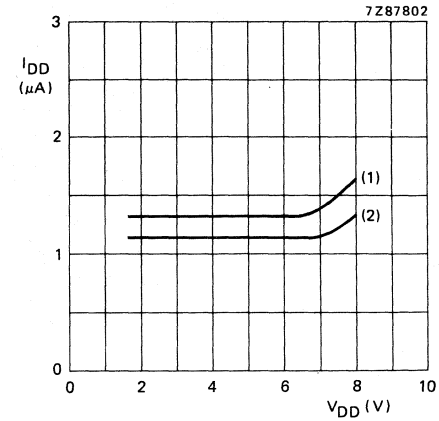
Fig. 24 Typical supply current (I_{DD}) in operating mode as a function of the supply voltage (V_{DD}); $T_{amb} = 25\ ^{o}C$.

DEVELOPMENT DATA



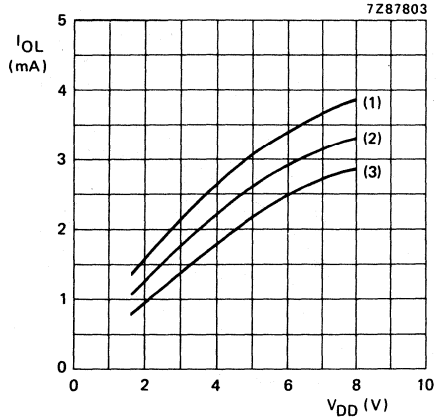
(1) clock frequency = 4 MHz
(2) clock frequency = 2 MHz
(3) clock frequency = 500 kHz

Fig. 25 Typical supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}); $T_{amb} = 25\ ^{o}C$.



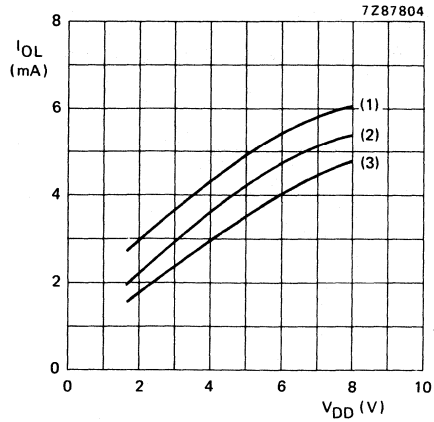
(1) $T_{amb} = 70\ ^{o}C$
(2) $T_{amb} = 25\ ^{o}C$

Fig. 26 Typical supply current (I_{DD}) in STOP mode as a function of the supply voltage (V_{DD}).



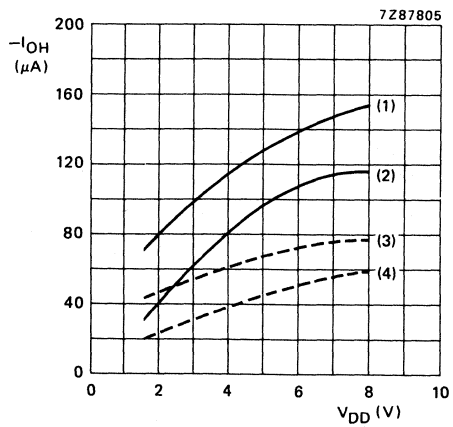
(1) $T_{amb} = -25\ ^{o}C$
(2) $T_{amb} = 25\ ^{o}C$
(3) $T_{amb} = 70\ ^{o}C$

Fig. 27 Output sink current LOW (I_{OL}), except outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); V_O = 0,4 V.



(1) $T_{amb} = -25\ ^{o}C$
(2) $T_{amb} = +25\ ^{o}C$
(3) $T_{amb} = +70\ ^{o}C$

Fig. 28 Output current LOW (I_{OL}), outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); V_O = 0,4 V.



(1) $T_{amb} = 25\ ^{o}C$; $V_O = V_{SS}$
(2) $T_{amb} = 25\ ^{o}C$; $V_O = 0{,}9V_{DD}$
(3) $T_{amb} = 70\ ^{o}C$; $V_O = V_{SS}$
(4) $T_{amb} = 70\ ^{o}C$; $V_O = 0{,}9V_{DD}$

Fig. 29 Output source current HIGH ($-I_{OH}$) as a function of supply voltage (V_{DD}).

A.C. CHARACTERISTICS

Rise and fall times between 10 and 90% levels; C_L = 50 pF

parameter	symbol	at 70 °C max. value			unit
	V_{DD}	1,8	3,0	6,0	V
Fall time	t_f	200	100	70	ns
Rise time	t_r	200	100	80	ns

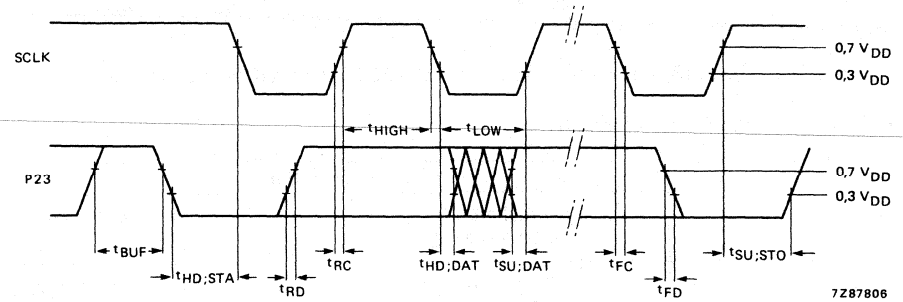


Fig. 30 PCD3343 timing requirements for the P23 and SCLK *input* signals.

Table 9 Input timing shown in figure 30

symbol	timing
t_{BUF}	$\geqslant 14t_{XTAL}$
$t_{HD;STA}$	$\geqslant 14t_{XTAL}$
t_{HIGH}	$\geqslant 17t_{XTAL}$
t_{LOW}	$\geqslant 17t_{XTAL}$
$t_{SY;STO}$	$\geqslant 14t_{XTAL}$
$t_{HD;DAT}$	> 0
$t_{SU;DAT}$	$\geqslant 250$ ns
t_{RD}	$\leqslant 1\ \mu s$
t_{RC}	$\leqslant 1\ \mu s$
t_{FD}	$\leqslant 1\ \mu s$
t_{FC}	$\leqslant 0{,}3\ \mu s$

Notes to Table 9

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 280 ns for f_{XTAL} = 3,58 MHz.
These figures apply to all modes.

DEVELOPMENT DATA

A.C. CHARACTERISTICS (continued)

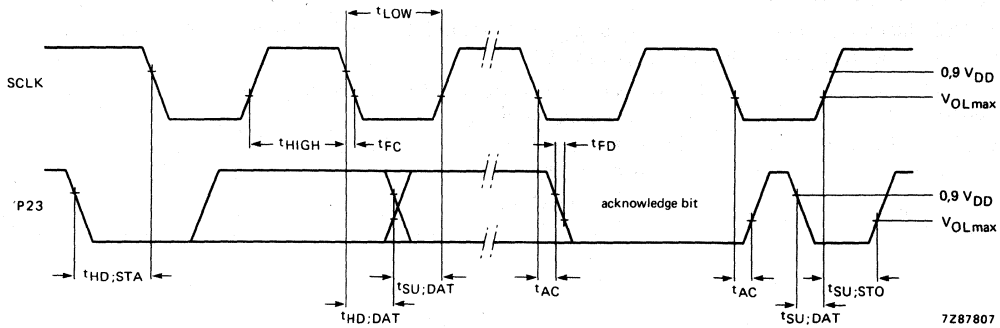


Fig. 31 PCD3343 timing requirements for the P23 and SCLK *output* signals.

Table 10 Output timing shown in figure 31

symbol	timing	
	normal mode (ASC in S2 = 0)	low-speed mode (ASC in S2 = 1)
$t_{HD;STA}$	½ (DF + 9) t_{XTAL}	¾ (DF + 9) t_{XTAL}
t_{HIGH}	½ (DF) t_{XTAL}	¾ (DF) t_{XTAL}
t_{LOW}	½ (DF) t_{XTAL}	¼ (DF) t_{XTAL}
$t_{SU;STO}$	½ (DF − 3) t_{XTAL}	¼ (DF − 3) t_{XTAL}
$t_{HD;DAT}$ (slave transmitter)		
any DF	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{HD;DAT}$ (master transmitter)		
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	– –
for DF $\leqslant$ 99	– –	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{SU;DAT}$ (master transmitter)		
for DF > 51	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$	– –
for DF > 99	–	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$	$\geqslant 9t_{XTAL}$
for DF $\leqslant$ 99	–	$\geqslant 9t_{XTAL}$
t_{AC}	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$ $\leqslant$ 100 ns at C_b = 400 pF	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$ $\leqslant$ 100 ns at C_b = 400 pF
t_{FD}, t_{FC}		

Notes to Table 10

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 280 ns for f_{XTAL} = 3,58 MHz.
DF = divisor (see Table 2 Serial I/O section).
C_b = the maximum bus capacitance for each line.

APPLICATION INFORMATION

A block diagram of an electronic featurephone built around the PCD3343 is shown in figure 32. It comprises the following dedicated telephony IC's:

- TEA1060/1061 — transmission circuit for telephony
- PCD3312 — DTMF generator with Serial I/O
- PCE2111 or PCF8577 — 2 LCD drivers in LCD module MB7020160
- PCD8571 — 1 K RAM's with Serial I/O; the number of RAM's depends on the required amount of stored telephone numbers
- PCD3360/3361 — programmable multi-tone ringer

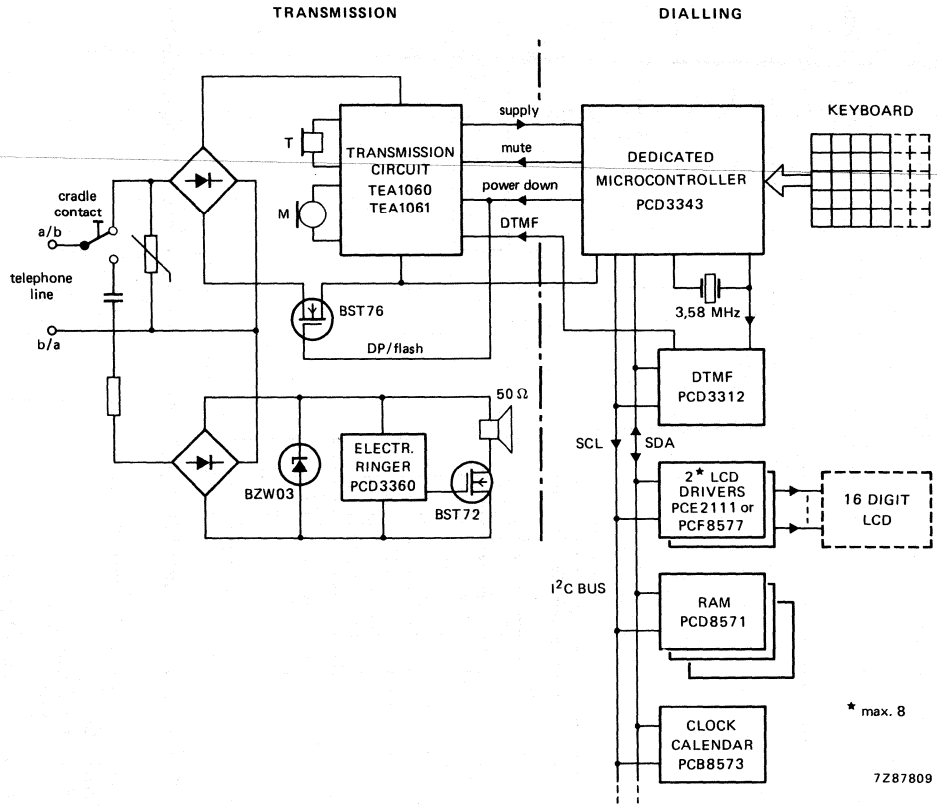


Fig. 32 Block diagram of electronic featurephone with common line interface.

A detailed application diagram of the PCD3343 with PCD3312 (DTMF), two PCD8571 (RAM) and two PCE2111 (LCD display drivers) is shown in figure 33.

Row 5 of the keyboard contains the following special keys:

- P — program and autodial
- FL — flash or register recall
- R — redial or extended redial
- AP — access pause

Row 6 contains the different diode options.

Columns 5 and 6 contain the button keys M0 to M9; single name keys for repertory telephone numbers.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

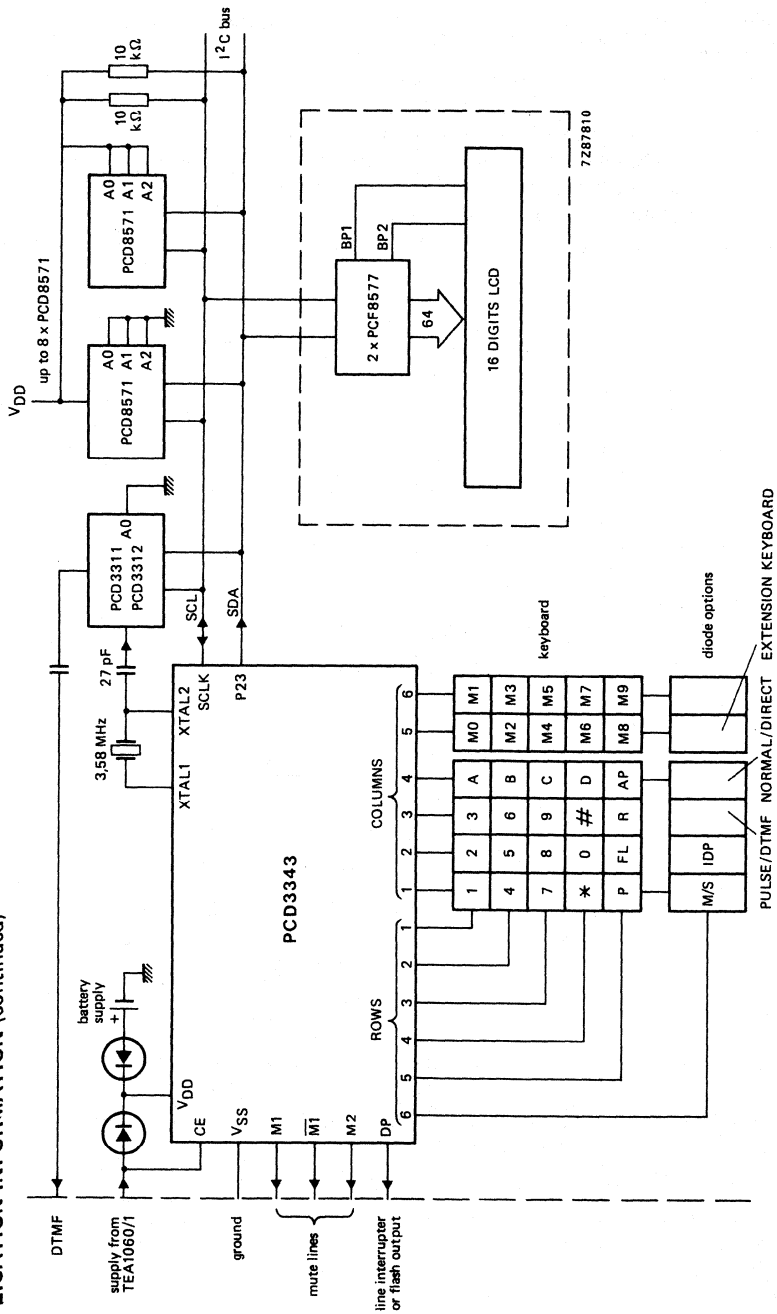


Fig. 33 Application diagram of PCD3343 for electronic featurephone with associated keyboard.

Additional information is available on request for the following:

- Serial I/O
- I^2C bus specification
- Interrupt logic
- Instruction set descriptions
- Software routines for an intelligent telephone set

VOICE SYNTHESIZER

GENERAL DESCRIPTION

The PCF8200 is a CMOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately.
Applications include automotive, telephony, personal computers, annunciators, aids for the handicapped, and general industrial devices.

Features

- Male and female speech with good quality
- Speech-band from 0 to 5 kHz
- Bit-rate between 455 bits/second and 4545 bits/second
- Programmable frame duration
- Programmable speaking speed
- CMOS technology
- Operating temperature range −40 to + 85 °C
- Single 5 V supply with low power consumption and power-down stand-by mode
- Interfaces easily with most popular microcomputers and microprocessors through 8 bit parallel bus or I^2C bus
- Software readable status word (parallel bus or I^2C bus)
- BUSY-signal and $\overline{REQ}$-signal hardware readable
- Internal low-pass filter and 11-bit D/A converter

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	–	5	–	V
Supply current	I_{DD}	–	12	#	mA
Supply current (stand-by)	$I_{DD(SB)}$	–	1	–	μA
Inputs					
Input voltage	V_{IH}	2,0	–	V_{DD}	V
Input voltage	V_{IL}	0	–	0,8	V
Input capacitance	C_I	–	7	–	pF
Outputs (D5 to D7)					
Output voltage high	V_{OH}	3,5	–	V_{DD}	V
Output voltage low	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

Value not yet available.

PACKAGE OUTLINE

24-lead DIL; plastic (SOT101A).

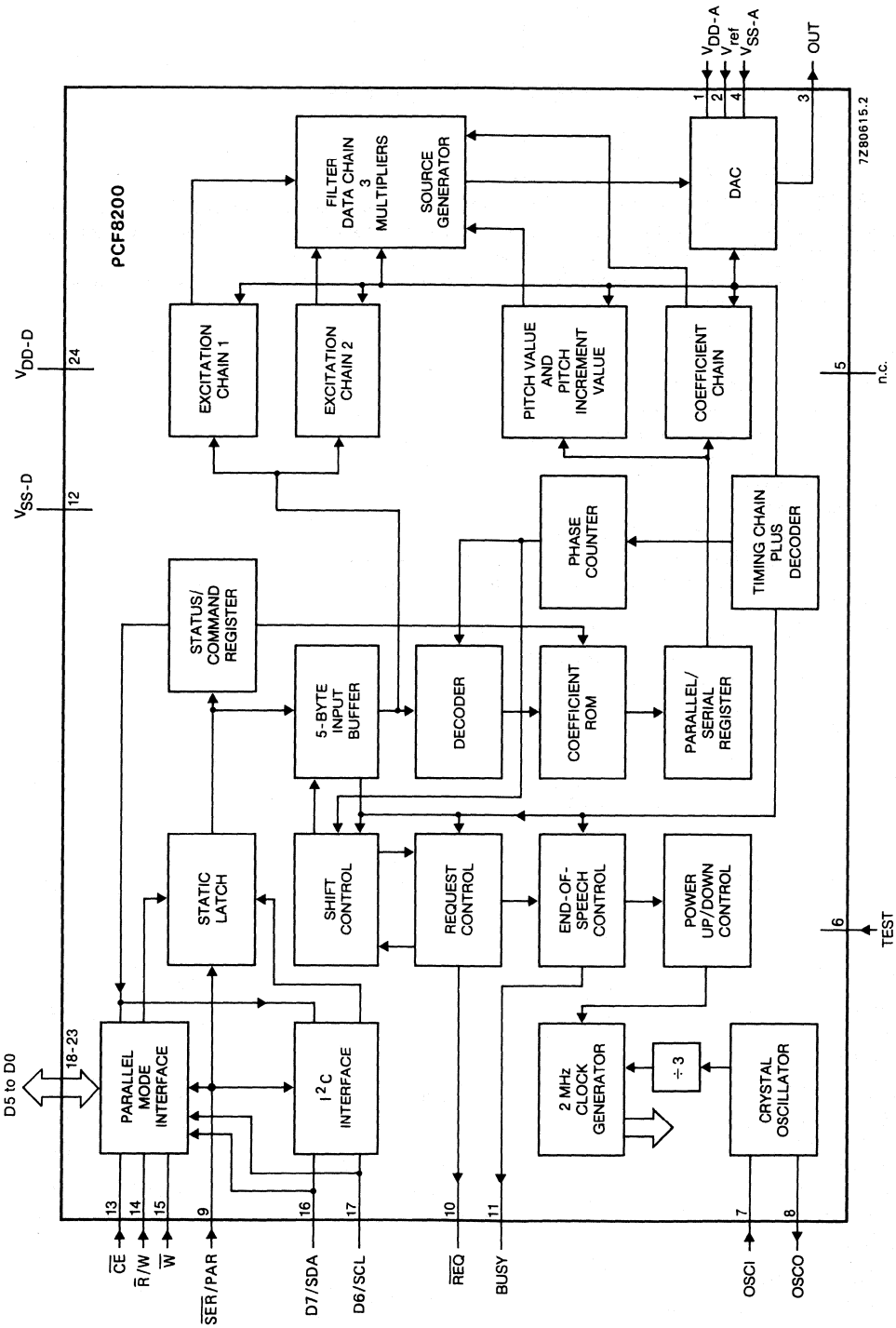


Fig. 1 Block diagram.

PINNING

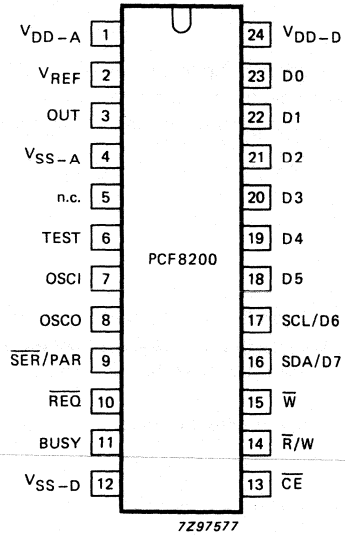


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

1	V_{DD-A}	positive supply voltage for DAC output stage
2	V_{REF}	DAC reference voltage input
3	OUT	speech output
4	V_{SS-A}	negative supply voltage for DAC stage
5	n.c.	not connected
6	TEST	for normal operation this pin must be grounded (V_{SS})
7	OSCI	oscillator input
8	OSCO	oscillator output
9	$\overline{SER}$/PAR	for parallel data bus operation this pin is hard-wired to V_{DD}, or to V_{SS} to enable the I^2C bus
10	$\overline{REQ}$	status bit indicating request for data
11	BUSY	status indicating synthesizer busy
12	V_{SS-D}	negative supply voltage for digital circuits
13	$\overline{CE}$	chip-enable input
14	R/$\overline{W}$	read/write control input
15	$\overline{W}$	write input
16	SDA/D7	I^2C bus serial data input/output (serial mode) or parallel data input/output D7 (parallel mode)
17	SCL/D6	I^2C bus serial clock input/output (serial mode) or parallel data input/output D6 (parallel mode)
18	D5	parallel data input/outputs
19	D4	
20	D3	
21	D2	
22	D1	
23	D0	
24	V_{DD-D}	positive supply voltage for digital circuits

FUNCTIONAL DESCRIPTION

The synthesizer has been designed for a vocal tract modelling technique of voice synthesis. An excitation signal is fed to a series of resonators. Each resonator simulates one of the formants in the original speech. It is controlled by two parameters, one for the resonant frequency and one for the bandwidth. Five formants are needed for male speech and four for female speech. The output of this system is defined by the excitation signal, the amplitude values and the resonator settings. By periodic updating of all parameters very high quality speech can be produced.

OPERATION

Speech characteristics change quite slowly, therefore the control parameters for the speech synthesizer can be adequately updated every few tens of milliseconds with interpolation during the interval to ensure a smooth changeover from one parameter value to the next. In the PCF8200 the standard-frame duration can be set to 8,8 , 10,4, 12,8 or 17,6 milliseconds with the speed-option, speaking speed, in the command-register.
The duration of each individual speech frame is programmable to be 1, 2, 3 or 5 times the standard-frame duration.

FD1, FD0	10	01	00	11	FS0, FS1
00	8,8	10,4	12,8	17,6	ms
01	17,6	20,8	25,6	35,2	ms
10	26,4	31,2	38,4	52,8	ms
11	44,0	52,0	64,0	88,0	ms

Table 1. Frame duration as a function of speed-option (FS1, FS0) and frame-duration (FD1, FD0).

The excitation signal is a random noise source for unvoiced sounds and a programmable pulse generator for voiced sounds. Both sources have an amplitude modulator which is updated 8 times in one speech-frame by linear interpolation. The pitch is updated every 1/8 of a standard frame.

The excitation signal is filtered with a five formant filter for male speech and a four formant filter for female speech. The formant filter is a cascade of all second-order sections. The control parameters, formant-frequency and formant-bandwidth, are updated eight times per speech frame by linear interpolation.
A block diagram of the formant synthesizer is shown in Fig. 3.

The filter output is upsampled to 80 kHz and filtered with a digital low-pass filter. Before the signal is digital to analogue converted (DAC), with an 11-bit switched capacitor DAC, the signal is multiplied with a DAC-amplitude factor. The use of a digital filter means that no external audio filtering is required for low-medium applications and minimal filtering is required for those applications requiring very high quality speech.

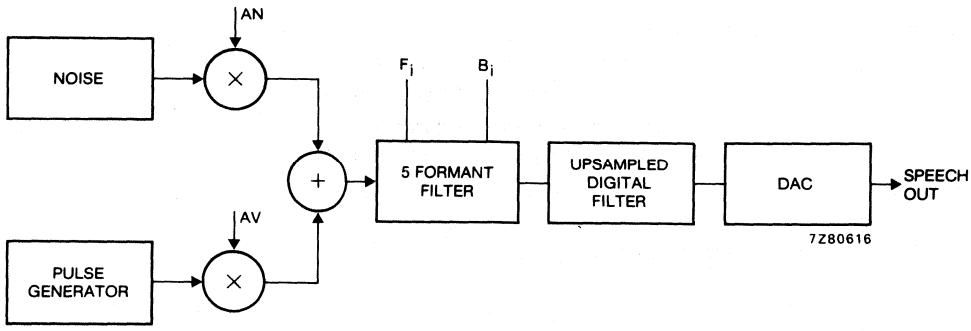


Fig. 3 Block diagram of formant synthesizer.

DATA FORMAT

Three types of format are used for data transfer to the synthesizer.

DAC-amplitude factor

The DAC-amplitude factor is one byte, which is used to optimize the digital speech signal to the 11-bit DAC. It is the first byte after a STOP or a BADSTOP or V_{DD} on. Table 2 indicates the amplitude factor.

byte	factor	dB
01110000	3,5	10,88
10110000	3,25	10,24
00110000	3,0	9,54
11010000	2,75	8,97
01010000	2,5	7,96
10010000	2,25	7,04
00010000	2,0	6,02
11100000	1,75	4,86
01100000	1,5	3,52
10100000	1,25	1,94
00100000	1,0	0,00
11000000	0,75	−2,50
01000000	0,5	−6,02
10000000	0,25	−12,04
00000000	0,0	
11110000	HEX code F0 is not allowed as a DAC amplitude	

Table 2 DAC amplitude factor.

Start pitch

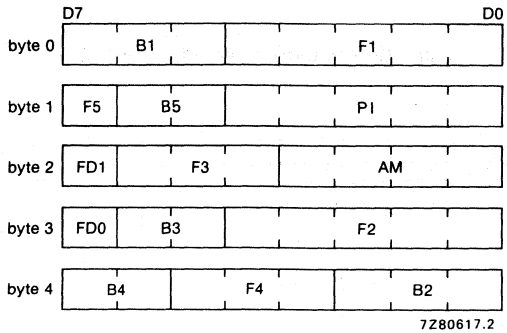
The second byte after a STOP or BADSTOP, or V_{DD} on is the start pitch. It is a one byte start value for the on-chip pitch-period generator.

Frame Data

The frame data is a five byte block which contains the filter and source information:

pitch increment/decrement value	5 bits
amplitude	4 bits
frame duration	2 bits
frequency of 1st formant	5 bits
frequency of 2nd formant	5 bits
frequency of 3rd formant	3 bits
frequency of 4th formant	3 bits
frequency of 5th formant	1 bit
bandwidth of 1st formant	3 bits
bandwidth of 2nd formant	3 bits
bandwidth of 3rd formant	2 bits
bandwidth of 4th formant	2 bits
bandwidth of 5th formant	2 bits
	40 bits = 5 bytes

The frame-data bits are organized as shown in Fig. 4.



It is not allowed to set byte 0 to the hexadecimal value 00.

Fig. 4 Format of frame-date.

CONTROL FORMAT

Command Write

A command write consists of two bytes, and it may occur before a data block. The four bits which can be written are shown in Fig. 5.

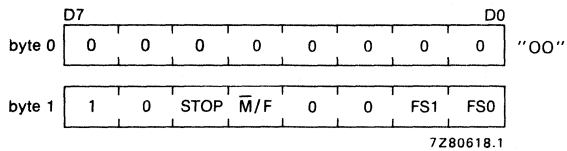


Fig. 5 Control write: first byte fixed, second byte control.

FS0, FS1 speed option

FS1	FS0	speech speed	standard-frame duration
0	0	100%	12,8 ms
0	1	145%	8,8 ms
1	0	123%	10,4 ms
1	1	73%	17,6 ms

$\overline{M}$/F, male/female option

$\overline{M}$/F = 0 male quantization table
= 1 female quantization table

STOP

STOP = 1 stop; repeat last complete frame with amplitude = 0 (no excitation signal)
= 0 if the frame data is not sent within the duration of a half frame, there will be a BADSTOP:

1. $\overline{REQ}$ = 1 STOP = 0
2. Repeat last frame with amplitude = 0
3. BUSY = 0

Status Read

Three status bits can be read out at any time without a preceding byte (00).
This is shown in Fig. 6.

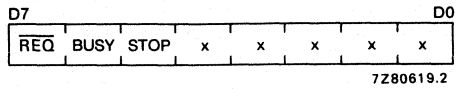


Fig. 6 Status read.

$\overline{REQ}$ = 1 No data required
= 0 Synthesizer requesting for new data
BUSY = 1 Busy (an utterance is pronounced)
= 0 Idle, $\overline{REQ}$ will set to 1; the synthesizer is in STOP or BADSTOP mode
STOP The STOP bit is the same as the stop bit written to the synthesizer during a command write.
STOP = 1, BUSY = 0 stopped by the user.
STOP = 0, BUSY = 0 BADSTOP because the data was not sent in time.

DEVELOPMENT DATA

After initial power-up the status/command register is set to the following status:

FS0, FS1 = 0 Standard-frame duration of 12,8 ms
$\overline{M}$/F = 0 Male quantization table
STOP = 0
BUSY = 0 Idle
$\overline{REQ}$ = 1 No data required

INTERFACE PROTOCOL

Data can be written to the synthesizer when $\overline{REQ}$ = 0 or, when $\overline{REQ}$ = 1 and BUSY = 0. Figure 7 shows the interface protocol of the synthesizer.

In parallel mode the synthesizer is activated by sending the DAC-amplitude factor. In serial mode the DAC-amplitude factor can be sent as soon as the synthesizer is powered-up.

The I²C transmitter/receiver will then acknowledge. When the request for the pitch-byte occurs the byte must be provided within the duration of a half standard frame. If the byte is not provided in time a BADSTOP will be generated.

During each data write operation, the status bit $\overline{REQ}$ will be set to '1'.
Within a frame data block, it disappears within a few microseconds, asking for the next byte of that block. If the bytes of frame data are not provided within the time-duration of a half frame, a BADSTOP will be generated.

I²C ADDRESS

On chip there is a I²C slave receiver/transmitter with the address:

7 6 5 4 3 2 1 0
0 0 1 0 0 0 0 R/W

POWER UP

The synthesizer will be set to power-up on a parallel-write sequence.

PAR-mode: The input-latches are active so they can receive the first byte

SER-mode: The I^2C transmitter/receiver will not acknowledge until the synthesizer has powered-up. To power up the synthesizer a parallel write sequence (Fig. 9) must be made to the synthesizer by using external logic for the control lines; at least one line must be toggled, $\overline{CE}$, while $\overline{W} = 0$ and $\overline{R}/W = 1$.
The synthesizer can be set to permanent power-up by hard-wired control pins ($\overline{CE} = 0$, $\overline{R}/W = 1$, $\overline{W} = 0$).

POWER DOWN MODE

When BUSY = 0 the synthesizer will be set to power-down. In the power-down mode the status/command register will be retained.
In power-down mode the clock-oscillator is switched off. After initial V_{DD} the synthesizer is in power-down mode.

HANDLING

All inputs and outputs are protected against electrostatic charge under normal handling conditions.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	any pin with respect to V_{SS}	V_{DD}	−0,3	7,5	V
Input voltage	any pin with respect to V_{SS}	V_I	−0,3	7,5	V
Output voltage	any pin with respect to V_{SS}	V_O	−0,3	7,5	V
D.C. input diode current	$V_I < V_{SS}$	$-I_{IK}$	–	20	mA
	$V_I > V_{DD}$	I_{IK}	–	20	mA
D.C. output diode current	$V_O < V_{SS}$	$-I_{OK}$	–	20	mA
	$V_O > V_{DD}$	I_{OK}	–	20	mA
Operating ambient temperature range		T_{amb}	−40	85	°C
Storage temperature range		T_{stg}	−55	125	°C

CHARACTERISTICS

T_{amb} = −45 to + 85 °C; supply voltage (V_{DD} to V_{SS}) = 4,5 to 5,5 V with respect to V_{SS}, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	10	–	mA
Standby current	$I_{DD(SB)}$	–	200	–	μA
Inputs					
$\overline{CE}$, R/$\overline{W}$, $\overline{W}$					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current V_{in} = 0 to 5,5 V	I_{IR}	−10	–	10	μA
Rise and fall times (note 2)	t_{rf}	–	–	50	ns
Input capacitance	C_I	–	–	7	pF
OSCI					
Input voltage HIGH	V_{IH}	2,2	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current V_{in} = 0 to 5,5 V	I_{IR}	−10	–	10	μA
Rise and fall times (note 2)	t_{rf}	–	–	50	ns
Input capacitance	C_I	–	–	7	pF
PARALLEL MODE					
Input Characteristics (D0 to D7)					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current (V_{in} = 0 to 5,5 V, output off)	I_{IR}	−10	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output Characteristics (D5 to D7 only)					
Output voltage HIGH (I_{OH} = −100 μA)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (I_{OL} = 3,2 mA)	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Rise and fall times (note 3)	t_{rf}	–	–	50	ns
SERIAL MODE					
Input characteristics (SDA and SDL)					
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input leakage current (V_{in} = 0 to 5,5 V, output off)	I_{IR}	−10	–	10	μA
Input capacitance	C_I	–	–	10	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Output Characteristics (SDA only, open drain)					
Output voltage LOW (I_{OL} = 3 mA)	V_{OL}	0	–	0,4	V
OSCILLATOR					
Crystal frequency	f_{XTAL}	–	6	6,1	MHz
V_{REF}					
Reference voltage	V_{REF}	1,9	–	$\frac{V_{DD}-1,5}{1,25}$	V
Input leakage current (active)	I_{IR}	–	5	–	μA
Outputs					
$\overline{REQ}$, BUSY					
Output voltage HIGH (I_{OH} = 100 μA)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (I_{OL} = 3,2 mA)	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Rise and fall times (note 3)	t_{rf}	–	–	50	ns
OUT					
Output voltage	V_{OUT}	0,66 x V_{REF}		1,34 x V_{REF}	V
Minimum external load		600	–	–	Ω
Timing characteristics (note 1) (Figs 8 and 9)					
Write enable	t_{WR}	200	–	–	ns
Data set-up for write	t_{DS}	150	–	–	ns
Data hold for write	t_{DH}	30	–	–	ns
Read enable	t_{RD}	200	–	–	ns
Data delay for read (note 2)	t_{DD}	–	–	150	ns
Data floating for read (note 2)	t_{DF}	–	–	150	ns
Control set-up	t_{CS}	0	–	–	ns
Control hold	t_{CH}	0	–	–	ns
REQ new (new byte of the same speech frame)	t_{RN}	–	# (≈ 3)		μs
REQ Valid	t_{RV}	0	–	–	ns
REQ Hold	t_{RH}	–	250	#	ns

NOTES TO THE CHARACTERISTICS

1. Timing reference level is 1,5 V; supply 5 V ± 10%; temperature range of –40 °C to 85 °C.
2. Levels greater than 2 V for a '1' or less than 0,8 V for a '0' are reached with a load of one TTL input and 50 pF.
3. Rise and fall times between 0,6 V and 2,2 V levels.

Values not yet available.

DEVELOPMENT DATA

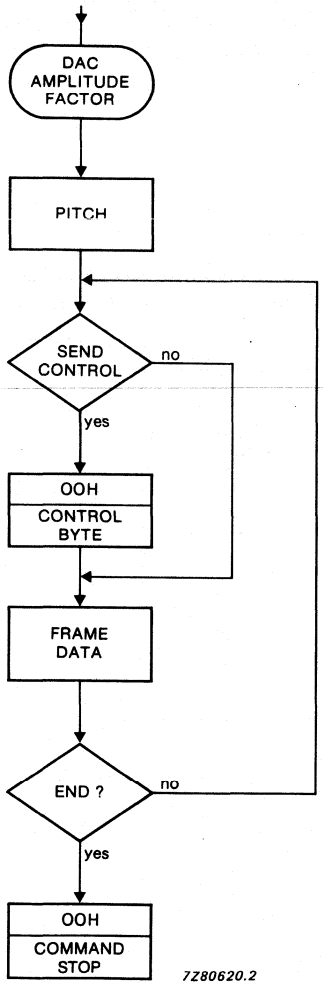
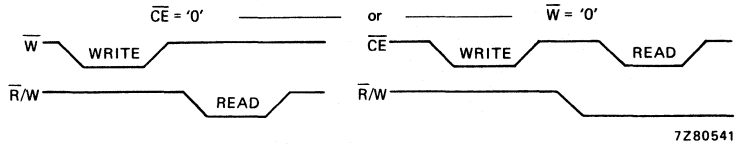


Fig. 7 Interface protocol.

Timing diagrams

The control signals $\overline{CE}$, $\overline{R}/W$ and $\overline{W}$ have been specified to enable easy interface to most microprocessors and microcomputers. For instance with connection to an MAB8048 microcomputer the $\overline{R}/W$ and $\overline{W}$ inputs can be used as the RD and WR strobe inputs.



Typical connection of control signals.

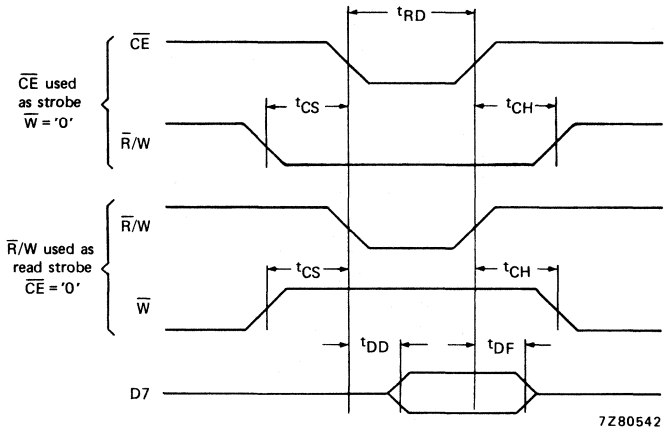


Fig. 8 Read timing.

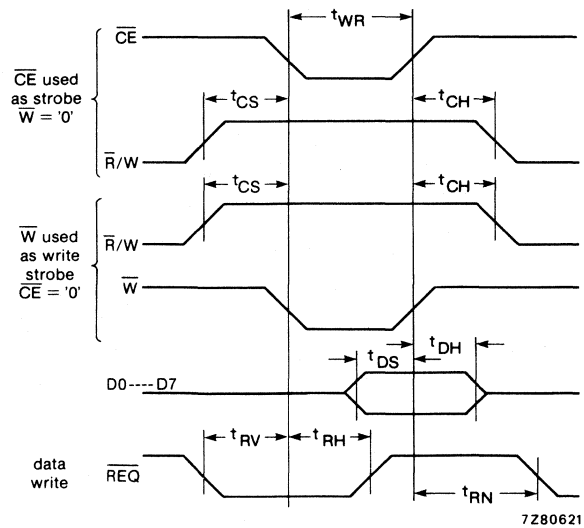


Fig. 9 Write timing.

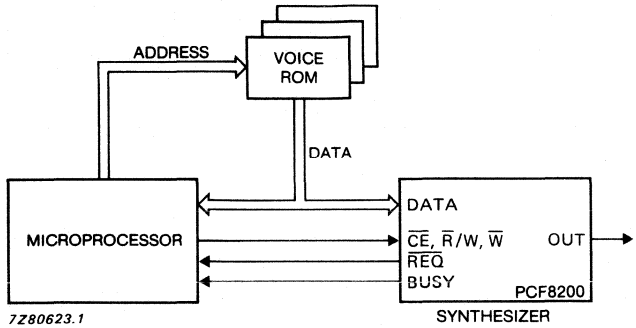


Fig. 10 Typical application configuration with parallel interface.

DEVELOPMENT DATA

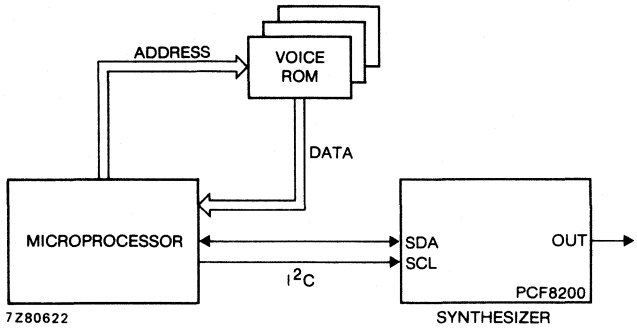


Fig. 11 Typical application configuration with series interface.

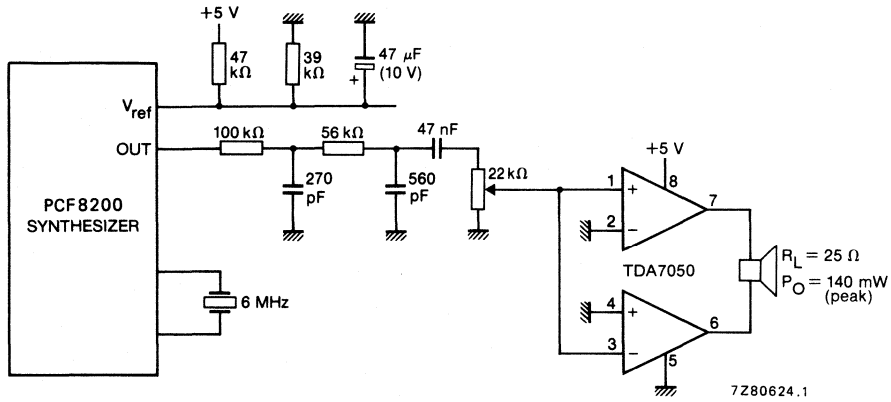


Fig. 12 An example of an output configuration.

SINGLE-CHIP 8-BIT MICROCONTROLLER FAMILY

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84CXXX microcontroller family. The family consists of the following devices:

- PCF84C00
- PCF84C21
- PCF84C41
- PCF84C81
- PCF84C12
- PCF84C22
- PCF84C42
- PCF84C85
- PCF84C121
- PCF84C230
- PCF84C270
- PCF84C271
- PCF84C430
- PCF84C470
- PCF84C640

This data sheet describes features of the PCF84CXXX microcontroller family which are common to several family members. For details on a particular device, consult the relevant data sheet.

All family members have quasi-bidirectional I/O port lines, a single-level vectored interrupt structure, an 8-bit timer/event counter and on-chip clock oscillator and clock circuits.

These efficient controllers also perform well as arithmetic processors. They have facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set is similar to that of the MAB8048 and the PCF84CXXX family is very similar to the MAB8400 family.

Features common to all family members are listed below.

Features

- 8-bit CPU, ROM, RAM, I/O in a single DIL or SO package
- 1 K, 2 K, 4 K or 8 K x 8 ROM; there is also a ROM-less device
- 64, 128 or 256 x 8 RAM
- Quasi-bidirectional I/O port lines
- Two test inputs: one of which is also an external interrupt input
- Single-level vectored interrupt structure
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2,5 V to 5,5 V)
- STOP and IDLE modes
- Power-on-reset circuit
- Operating temperature range: −40 to + 85 °C

PACKAGE OUTLINES

Consult individual data sheets.

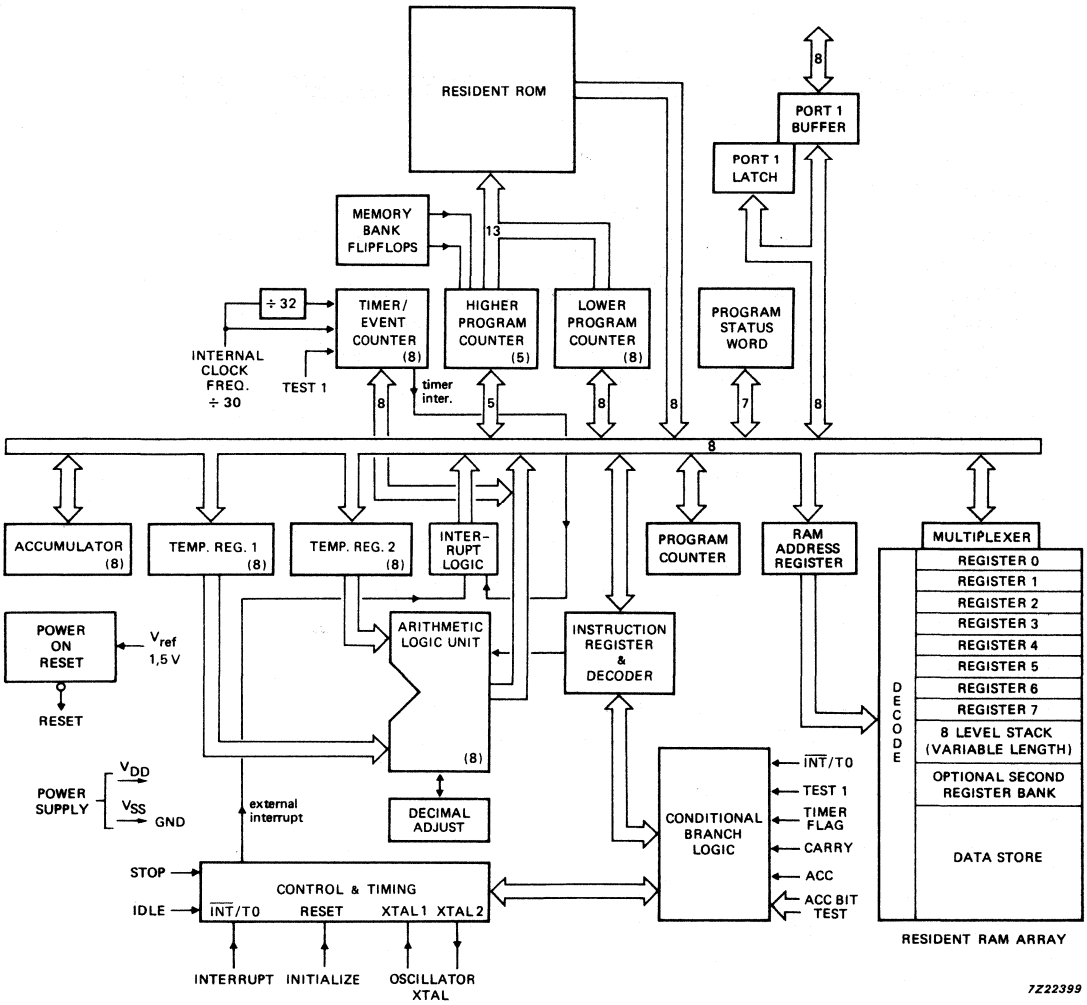


Fig. 1 PCF84CXXX block diagram.

FUNCTIONAL DESCRIPTION

Program memory

The program memory consists of 1 K, 2 K, 4 K or 8 K bytes of read-only memory (ROM). Each location is directly addressable by the program counter. The ROM is mask-programmed at the factory. Fig. 2 shows the program memory map.

Four program memory locations are of special importance:

- Location 0: contains the first instruction to be executed after the microcontroller is initialized (RESET)
- Location 3: contains the first byte of an external interrupt service routine
- Location 5: contains the first byte of a serial I/O and derivative interrupt service routine
- Location 7: contains the first byte of a timer/event counter interrupt service routine

Program memory is arranged in banks of 2 K bytes, which are selected by SEL MB instructions (family members with more than 2 K ROM only). The program memory is further divided into location 'pages', each of 256 bytes. This latter division applies only for conditional branches. Memory bank boundaries can be crossed only by using unconditional branch instructions after the appropriate memory bank has been selected. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory

Data memory consists of 64, 128 or 256 bytes of random-access memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Fig. 3 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service routines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first two locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

FUNCTIONAL DESCRIPTION (continued)

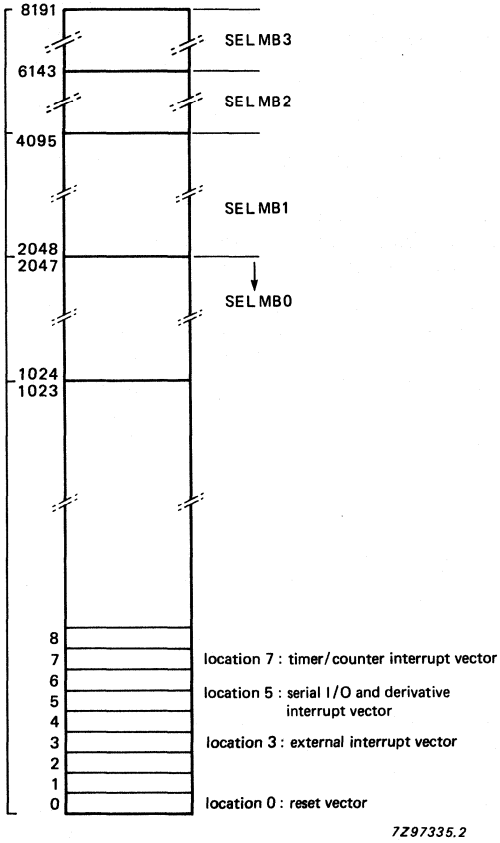


Fig. 2 Program memory map.

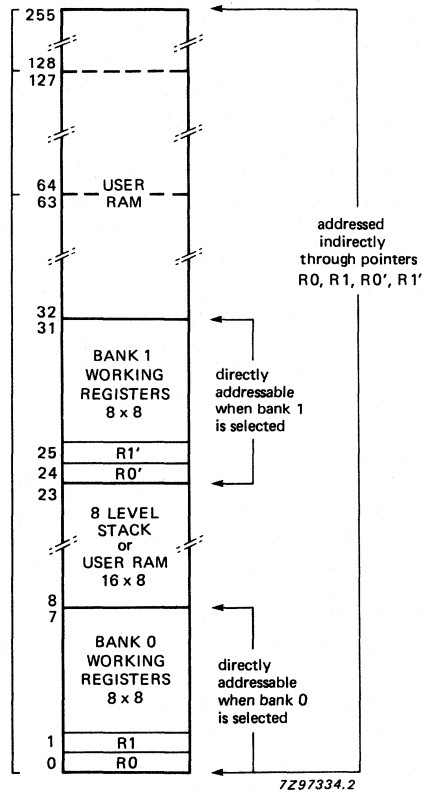


Fig. 3 Data memory map.

Program counter stack

Locations 8 to 23 may be designated as an 8-level program counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Fig. 4) enables the microcontroller to keep track of the return addresses and status prior to interrupts or CALL instructions by storing the contents of the program counter before servicing the subroutine. A 3-bit stack pointer determines which of the eight register pairs of the program counter stack will be loaded with the next return address and status.

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11, ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If all 8 levels of subroutine and interrupt nesting are not used, the unused portion of the stack may be used as any other indirectly addressable RAM locations.

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

The value of the saved contents of the program counter during an interrupt CALL is not the same as the value saved during a normal CALL to subroutine. During an interrupt CALL, the program counter return address is saved; during a subroutine CALL, the saved program counter value is one less than the program counter return address.

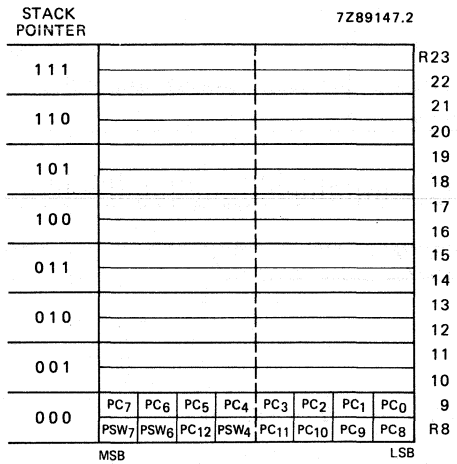


Fig. 4 Program counter stack.

IDLE and STOP modes

IDLE mode

When the microcontroller enters the IDLE mode via the IDLE instruction (01 H), the oscillator, timer/counter and serial I/O are kept running. The microcontroller exits from the IDLE mode via a RESET or one of three interrupts if they are enabled. If the interrupt is not enabled, the microcontroller will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig. 5).

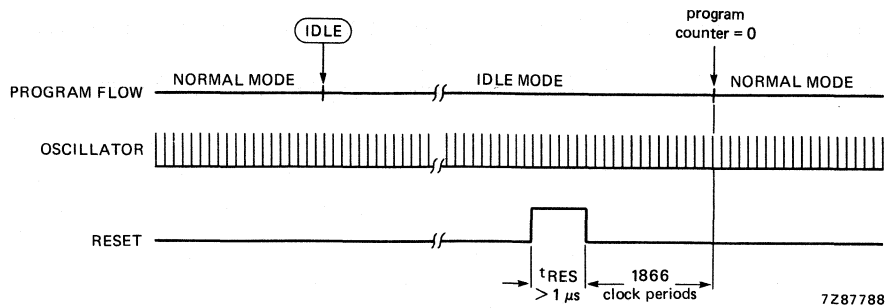


Fig. 5 Exit from IDLE mode via a RESET.

FUNCTIONAL DESCRIPTION (continued)

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A HIGH-to-LOW transition on the external interrupt pin ($\overline{INT}$/T0) reactivates the microcontroller. A LOW level applied to $\overline{INT}$/T0 will reactivate the microcontroller only in the STOP mode. Thus, if $\overline{INT}$/T0 was LOW before the microcontroller entered the IDLE mode, it must go HIGH before the microcontroller can be reactivated (see Fig. 6).

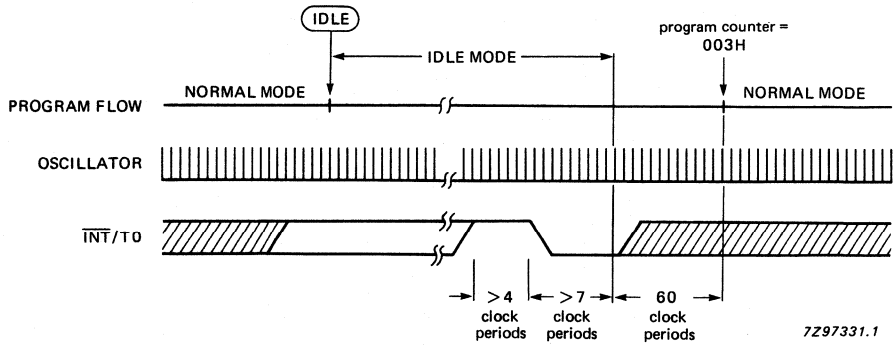


Fig. 6 Exit from IDLE mode via an interrupt.

Wake-up from the IDLE mode is ensured when $\overline{INT}$/T0 is HIGH for at least 4 CP (clock periods) and then LOW for 7 CP. After the initial forced CALL 003 H operation (60 CP), the program continues with the external interrupt service routine. During the STOP mode, the address of the instruction immediately following the instruction that caused the microcontroller to enter the IDLE mode is present on the address bus.

STOP mode

The microcontroller enters the STOP mode via the STOP instruction (22 H). The oscillator is switched off and the internal status of the CPU, RAM contents and the state of I/O ports are not affected. The microcontroller can be brought out of the STOP mode by an active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied, an internal delay of 1866 CP is provided to ensure that all internal clocks are operating correctly before restart (see Fig. 7).

Note: the start-up time of a crystal oscillator is measured in milliseconds, and the 1866 CP count begins after this start-up time.

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence is executed.

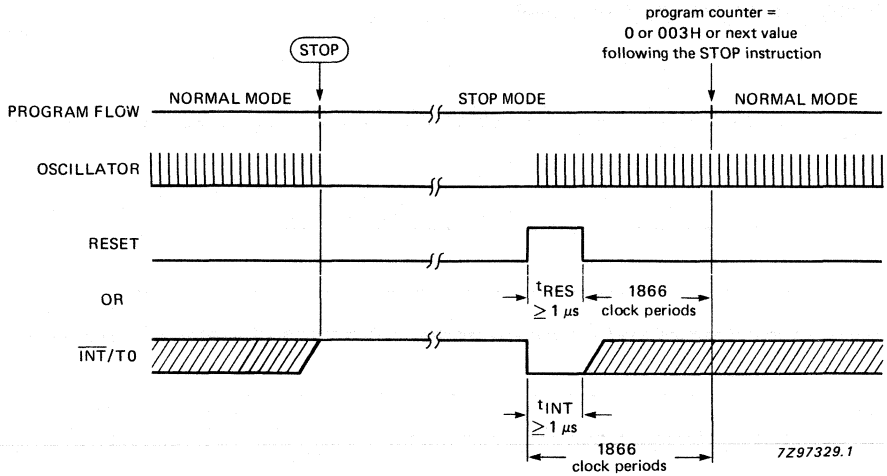


Fig. 7 Entering and exiting the STOP mode.

If the microcontroller exits the STOP mode by pulling the external interrupt input pin LOW, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller executes one instruction of the main program (the instruction following the STOP instruction) and then calls the interrupt routine. If the interrupt is not enabled, it continues the normal program sequence by executing the instruction following the STOP instruction.

The microcontroller is restarted by a LOW level applied at the $\overline{INT}$/T0 pin.

Note: When exiting the STOP mode via an interrupt, a further instruction in the main program is executed before the interrupt routine is entered.

If the $\overline{INT}$/T0 level is active (LOW) during the STOP instruction, no STOP is executed.

A LOW level on the external interrupt input of at least 1 µs will cause the microcontroller to exit the STOP mode. During the STOP mode, the address of the instruction immediately following the instruction that caused the microcontroller to enter the STOP mode is present on the address bus.

I/O facilities

Parallel ports

Parallel port lines can be individually configured as outputs or inputs; theri structure is quasi-bidirectional. Output data written to a port is latched and remains unchanged until rewritten. Input data is not latched and must be present until read by an input instruction.

Input lines are fully CMOS compatible; output lines can drive one TTL or CMOS load.

Fig. 8 shows the timing diagram for all ports using IN, OUTL, ANL, and ORL instructions. For the OUTL instruction, data changes on time slot 7 of cycle 1. For the MOV, ANL and ORL instructions, the ports change on time slot 7 of cycle 2.

FUNCTIONAL DESCRIPTION (continued)

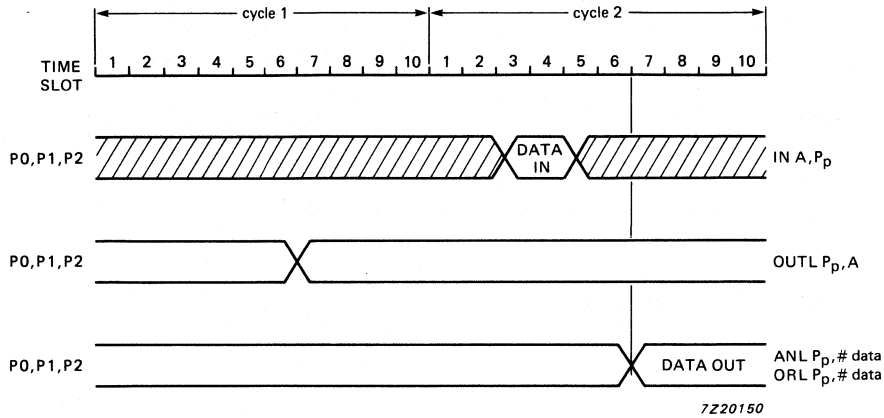


Fig. 8 Timing diagram for all ports using IN, OUTL, ANL, and ORL instructions.

Fig. 9 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source.

Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current source is sufficient for a TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output.

When a logic 1 is written to a port line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period), to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to a port line will not switch TR2 on. This ensures that the port lines can be pulled LOW when configured as inputs.

When a logic 0 is written to a port line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the port line; otherwise TR1 will remain low impedance.

PCF84CXXX mask options make it possible for each individual port line to be configured as one of the following:

1. STANDARD PORT: quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and P-channel booster transistor TR2. TR2 is only active during 1 clock cycle (Fig. 9).
2. OPEN DRAIN: Quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig. 10). When an open drain port is unused it must be connected to V_{SS}.
3. PUSH-PULL OUTPUT: the outputs can sink or source 1,6 mA (min.) at V_{DD} = 5 V. Thse pins may not be used as inputs (Fig. 11). The contents of the port latch may be read using the IN A,pp instruction.

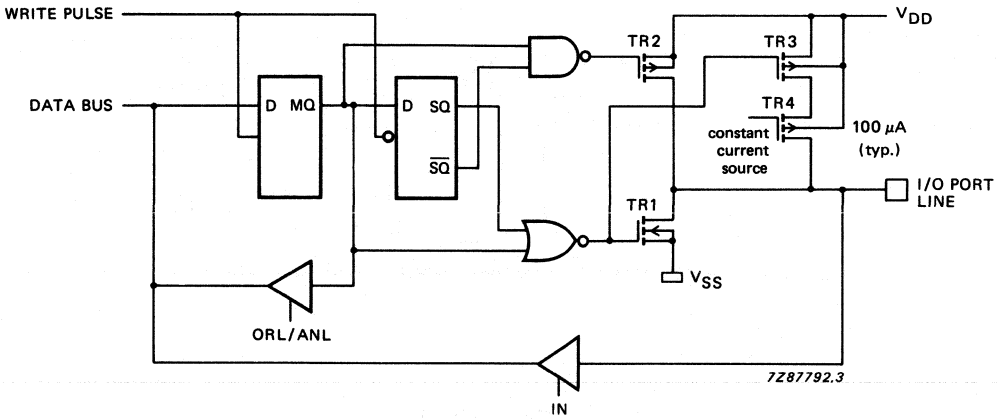


Fig. 9 Standard output with switched pull-up current source.

DEVELOPMENT DATA

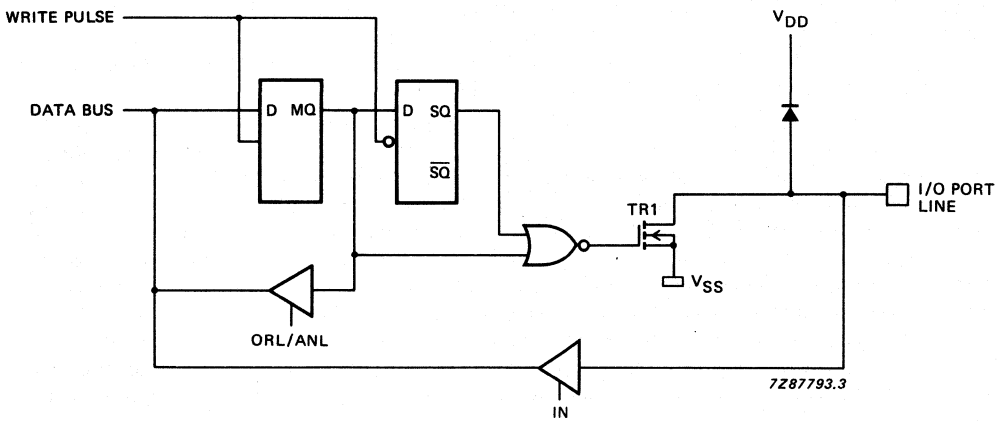


Fig. 10 Open drain output.

FUNCTIONAL DESCRIPTION (continued)

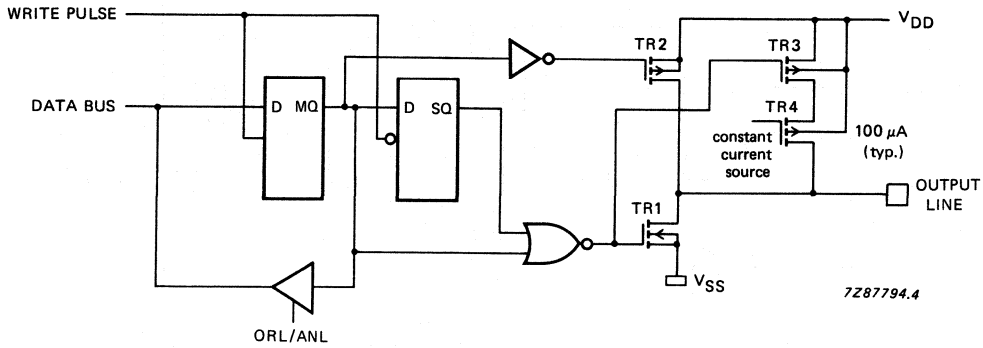


Fig. 11 Push-pull output.

Serial I/O (SIO)

The PCF84CXXX has an on-chip serial I/O interface that supports the I^2C-bus. Whereas a normal microcontroller must regularly monitor the serial data bus for the presence of data, the serial I/O interface detects, receives and converts the serial data stream into parallel format without interrupting the execution of the current program. An interrupt is sent to the PCF84CXXX only when a complete byte is received. It then reads the data byte in one instruction.

The design of the PCF84CXXX serial I/O system allows any number of devices from the PCF8500 family (clips) to be connected via the two-line serial bus. The ability of any devices to communicate, without interrupting the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to a message prefixed with its own address or the 'general CALL' address. Address recognition is performed by the interface hardware so that operation of the microcontroller need only be interrupted when a valid address has been received. This saves significant processing time and memory space compared with a conventional microcontroller employing a software serial interface. When the addressing facility is not required, for instance in a system with only two microcontrollers, direct data transfer without addressing can be performed. In multi-master systems, an automatically invoked arbitration procedure prevents two or more devices from continuing simultaneous transmission.

In NORMAL (running) and IDLE mode, the serial I/O logic remains active; its internal system clock will be switched off when there is no activity on the serial bus.

After execution of the STOP instruction, the oscillator of the PCF84CXXX is switched off. This means that the serial I/O logic will remain in the state it was in when the STOP mode was entered. To avoid "bus block" problems and to assure correct start-up of the bus after exit from the STOP mode, the user should disable the serial logic (ESO = 0) prior to the execution of the STOP instruction.

Serial I/O interface

Figure 12 shows the serial I/O interface. The clock line of the serial bus has exclusive use of the SCLK pin while the data line shares the SERIAL DATA pin with I/O line P2.3. When the serial I/O is enabled, P2.3 is disabled as a parallel port line; (P2.3 and SCLK are open drain; when unused these lines must be connected to V_{SS}).

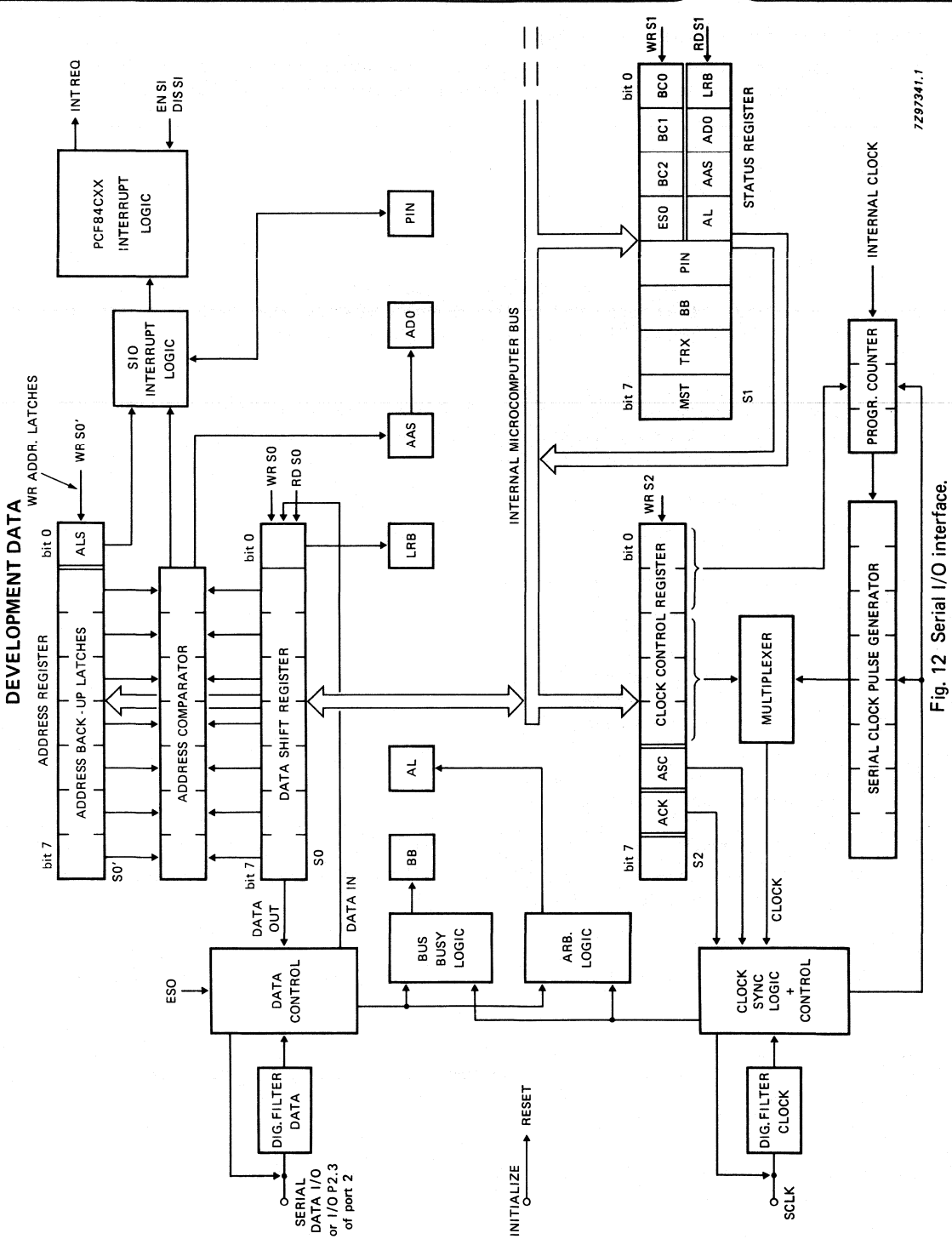


Fig. 12 Serial I/O interface.

FUNCTIONAL DESCRIPTION (continued)

The microcontroller and interface communicate via the internal microcontroller bus and the Serial Interrupt Request line. Data and information controlling the operation of the interface are stored in four registers:

- Data shift register (S0)
- Serial I/O interface status word (S1)
- Serial clock control word (S2)
- Address register (SO')

Data shift register (S0)

Register S0 converts serial data to parallel format and vice versa. An interrupt is generated only after a complete byte has been transmitted, or after a complete data byte, specific address or 'general CALL' address has been received. The most significant bit is transmitted first.

Serial I/O interface status word (S1)

Register S1 provides information concerning the state of the interface and stores information from the microcontroller. Bits 0 to 3 are duplicated: control bits in these positions can only be written by the microcontroller, while status bits can only be read.

MST and TRX (see Table 1)

These bits determine the operating mode of the serial I/O interface.

Table 1 Operating modes of the serial I/O interface

MST	TRX	operating mode
0	0	slave receiver
1	0	master receiver
0	1	slave transmitter
1	1	master transmitter

BB: Bus Busy.

This flag indicates the status of the bus.

PIN: Pending Interrupt NOT

PIN = '0' indicates the presence of a pending interrupt, which will cause a Serial Interrupt Request when the serial interrupt mechanism is enabled.

ESO: Enable Serial output

The ESO flag enables/disables the serial I/O interface: ESO = '1' enables, ESO = '0' disables. ESO can only be written by software.

BC0, BC1 and BC2

Bits BC0, BC1 and BC2 indicate the number of bits received or transmitted in a data stream. These bits can only be written by software.

AL: Arbitration Lost

The arbitration lost flag is set by hardware when the serial I/O interface, as master transmitter, loses a bus arbitration procedure.

AAS: Addressed As Slave

This flag is set by hardware when the interface detects either its own specific address or the 'general CALL' address as the first byte of a transfer and the interface has been programmed to operate in the address recognition mode.

AD0: Address Zero

This flag os set by hardware after detection of the 'general CALL' address when the interface is operating in the address recognition mode.

LRB: Last Received Bit

This contains either the last data bit received or, for a transmitting device in the acknowledgement mode, the acknowledgement signal from the receiving device.

Bits AL, AAS, AD0 and LRB can only be read by software.

Serial clock control word (S2)

Bits 0 to 4 of the clock register S2 determine the frequency of the serial clock signal. When a 6 MHz crystal is used, the frequency of the serial clock can be varied between 1 kHz and 154 kHz (see Table 2). An asymmetrical clock with a HIGH-to-LOW ratio of 3 : 1 can be generated using bit 5. The asymmetrical clock allows a microcontroller more time per clock period for sampling the data line, making the timing of this action less critical. Bit 6 can be used to activate the acknowledge mode of the serial I/O. S2 is a write only register.

Address register (S0)

The address register contains the 7-bit address back-up latches and the bit (ALS) used to enable/disable the address recognition mode. The address register can be written using the MOV S0, A and MOV S0, # data instructions, but only when ESO = logic 0.

Serial I/O interrupt logic

An EN SI instruction enables and a DIS SI instruction disables the interrupt logic. When enabled, a pending interrupt results in a serial I/O interrupt to the processor, causing a CALL to location 5 in the ROM. When disabled, the presence of an interrupt request is still indicated by PIN in S1, but the interrupt will not be serviced.

FUNCTIONAL DESCRIPTION (continued)

Table 2 SIO clock pulse frequency control when using a 6 MHz and a 10 MHz crystal

hexadecimal S20-S24 code	f_{OSC} divided by	f_{OSC} = 6 MHz f_{SCLK} (kHz)**	f_{OSC} = 10 MHz f_{SCLK} (kHz)**
0	not allowed		
1	39	*154	*256
2	45	*133	*222
3	51	*118	*196
4	63	95	*159
5	75	80	*133
6	87	69	*115
7	99	61	*101
8	123	49	81
9	147	41	68
A	171	35	58
B	195	31	51
C	243	25	41
D	291	21	34
E	339	18	29
F	387	16	26
10	483	12	21
11	579	10	17
12	675	8,9	15
13	771	7,8	13,4
14	963	6,2	10,4
15	1155	5,2	8,7
16	1347	4,5	7,4
17	1539	3,9	6,5
18	1923	3,1	5,2
19	2307	2,6	4,3
1A	2691	2,2	3,7
1B	3075	2,0	3,3
1C	3843	1,6	2,6
1D	4611	1,3	2,2
1E	5379	1,1	1,9
1F	6147	1,0	1,6

* Not permitted for I^2C operation.

** The maximum clock frequency in the I^2C systems is 100 kHz.

Interrupts

When an interrupt routine is entered, the contents of the program counter and bits 4, 6 and 7 of the PSW are saved in the program counter stack. The contents of the accumulator can only be saved by user software. Interrupt acknowledgement may be carried out by software via I/O ports. All interrupt routines must reside in memory bank 0; the SEL MB instructions may not be used within an interrupt routine. An interrupt routine can only be terminated by the RETR (return and restore) instruction. During an interrupt routine, subroutine calls must be terminated by the RET instruction. Using the RETR instruction to terminate a subroutine called in an interrupt routine would terminate the interrupt routine prematurely and result in a wrong return address.

External Interrupts

When the external interrupt is enabled and no interrupt routine is in progress, a HIGH-to-LOW transition on the $\overline{\text{INT}}$/T0 pin sets the External Interrupt Flag (EIF) and initiates the external interrupt routine by forcing a CALL to program memory location 3.* The program counter points to the external interrupt vector address (003 H) between 2,6 and 3,6 machine cycles after the transition occurs. Interrupt latency depends on the instruction that is being executed when the transition occurs. If an interrupt routine is already in progress, an external interrupt request is stored in the External Interrupt Flag (EIF). When the external interrupt has been disabled, the request is still latched into the digital filter. Execution of a DIS I instruction cancels stored interrupt requests by clearing both the digital filter latch and the external interrupt flag.

An additional external interrupt can be created by enabling the timer/counter interrupt and loading FFH into the counter (one less than overflow). If the event counter mode is enabled by executing the STRT CNT instruction, a LOW-to-HIGH transition on the T1 input will then initiate an interrupt routine by forcing a call to the timer/counter interrupt vector (location 7).

SIO Interrupt

An interrupt request from the SIO hardware will set the PIN flag to its active LOW state. This action is independent of the Enable SIO interrupt flag. When the SIO interrupt is enabled, the active LOW PIN flag will invoke the SIO interrupt routine by forcing a CALL to program memory location 5. After the SIO interrupt is initiated , the PIN flag is not automatically reset HIGH. PIN must be cleared by software during the interrupt routine.

Timer/Counter Interrupt

When no interrupt is in progress and the timer/counter is enabled, a timer/counter overflow sets the Timer Interrupt Flag (TIF). This initiates the timer interrupt routine by forcing a CALL to program memory location 7.** If an interrupt routine is in progress, the interrupt request is stored in the timer interrrupt flag only if the timer interrupt has been enabled. Execution of a DIS TCNTI instruction cancels a previously stored interrupt request. The timer flag (TF) is set every time the timer/counter overflows and is not automatically reset when the timer/counter interrupt routine is called. It can only be cleared by the JTF and JNTF instructions or by a hardware RESET.

Interrupt Priority

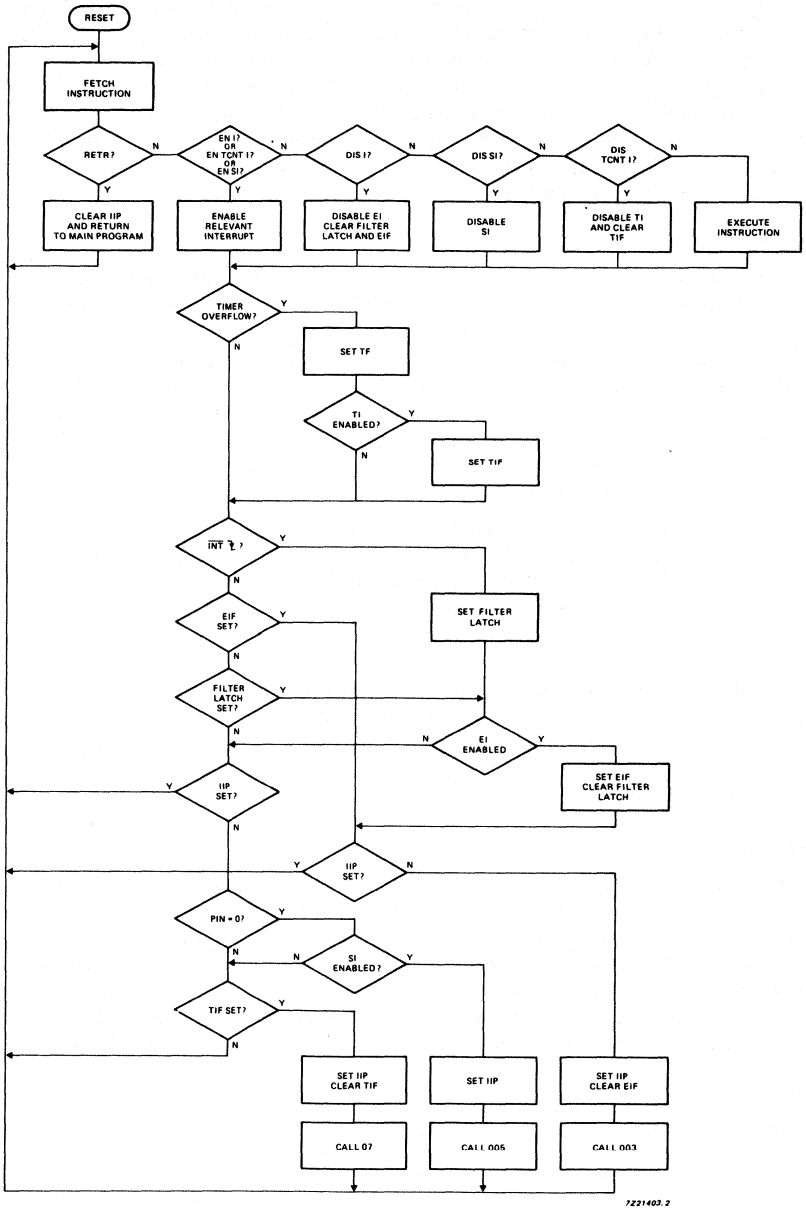
If simultaneous interrupts occur, their priority is as follows:

External (highest)
SIO
Timer/Counter (lowest)

An interrupt routine can only be interrupted by a hardware RESET and cannot be interrupted by other interrupts (which will be latched). When the interrupt routine is terminated by the RETR instruction, at least one instruction of the main program will be executed before another interrupt routine is entered.

* This CALL clears the EIF flag.
** This CALL clears the TIF flag.

FUNCTIONAL DESCRIPTION (continued)



EI	External Interrupt	TF	Timer Flag
SI	Serial Interrupt	TIF	Timer Interrupt Flag
TI	Timer/counter Interrupt	PIN	Pending Interrupt Not (SIO)
EIF	External Interrupt Flag	IIP	Interrupt In Progress Flag

Fig. 13(a) Flow chart illustrating the interrupt handling sequence.

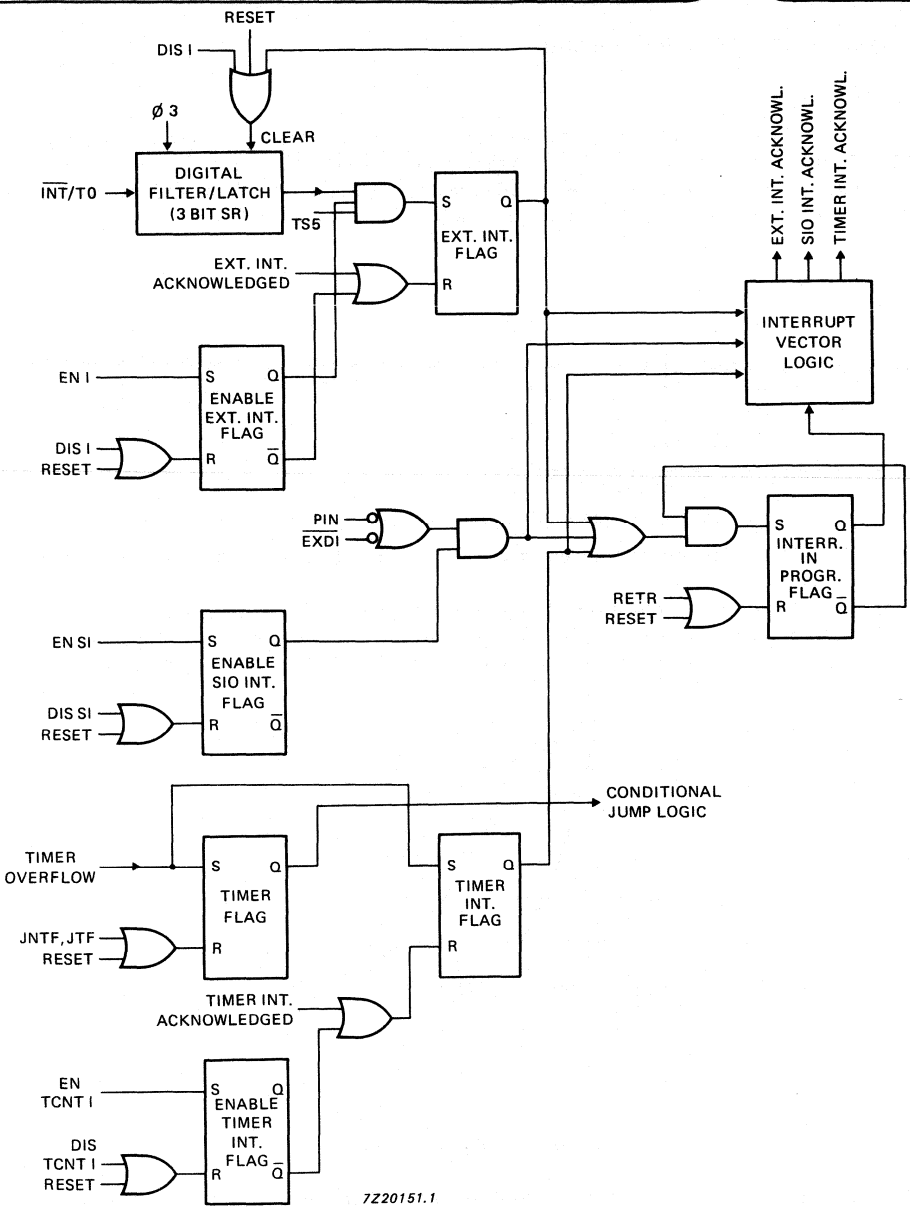


Fig. 13(b) Simplified schematic of the interrupt logic.

Notes to figure 13(b)

1. $\overline{INT}$/T0 negative edge is always latched in the digital filter/latch.
2. Correct interrupt timing is ensured when $\overline{INT}$/T0 is HIGH for $>$ 4 CP and then LOW for $>$ 7 CP.
3. When the interrupt in progress flag is set, further external and timer interrupts are latched but ignored, until RETR is executed.
4. A DIS I instruction always clears a pending external interrupt.
5. For all flip-flops, RESET overrules SET.

FUNCTIONAL DESCRIPTION (continued)

Oscillator (see Fig. 14)

The oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-supply voltage condition is present to prevent discharge of a weak back-up battery. Provided the supply voltage is within the operating range, the oscillator will be restarted after a STOP instruction by a LOW level at the $\overline{INT}$/T0 pin or a HIGH level at the RESET pin.

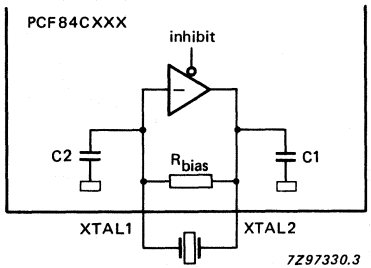


Fig. 14 Oscillator with integrated elements.

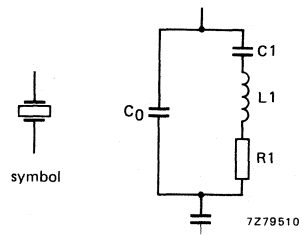


Fig. 15 Crystal unit equivalent circuit.

The values of crystal series resistance R1 and the crystal's total load capacitance C_L (C_0 + wiring + external capacitors) must not be above the curve (Fig. 16) for the corresponding frequency.
Note: if external capacitors are connected to XTAL1 and XTAL2, they must be of equal value.

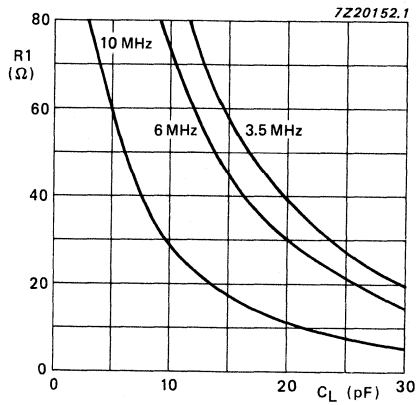


Fig. 16 Crystal circuit criteria.

XTAL2 is the output of the inverting amplifier. An external clock can be applied to XTAL1.
A machine cycle consists of 10 time slots; each time slot is 3 oscillator periods.

Timer/event counter (see Fig. 17)

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 3 shows the instructions that control the counter and the prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW-to-HIGH transitions on pin T1 are counted. The counter is incremented during a machine cycle only if the falling edge occurs during the first 7 time slots; otherwise it is incremented during the next cycle. The maximum rate at which the counter may be incremented is once every machine cycle. When the counter overflows, the Timer flag is set. The flag can be tested and reset using the JTF (jump if Timer flag = logic 1) or JNTF (jump if Timer flag = logic 0) instruction. Overflow also generates an interrupt request to the microcontroller by setting the Timer Interrupt Flag when the timer/event counter interrupt is enabled.

Table 3 Timer/event counter control

function	timer mode modulo-1, modulo-32*	counter mode
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ**	MOV A,T	MOV A,T

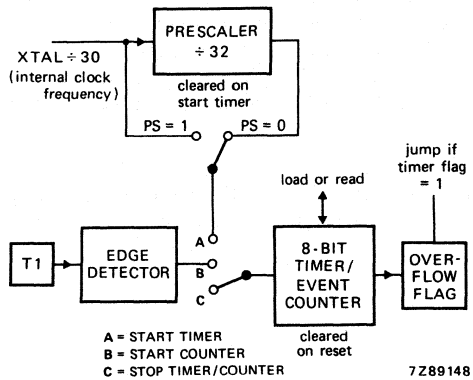


Fig. 17 Timer/event counter.

* With prescaler select (PS) = logic 0, the timer is incremented every 32 machine cycles; with PS = logic 1 the timer is incremented every machine cycle (prescaler not used), the prescaler is cleared by the STRT T instruction and is not readable.

** READ does not disturb the counting process.

FUNCTIONAL DESCRIPTION (continued)

Program status word (see Fig. 18)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.
The PSW bits are:

- Bits 0 to 2 — stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 — prescaler select (PS);
  0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 — working register bank select (RBS);
  0 = register bank 0; 1 = register bank 1
- Bit 5 — not used (1)
- Bit 6 — auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 — carry (CY); the carry flag indicates that the previous operation resulted in an overflow of the accumulator

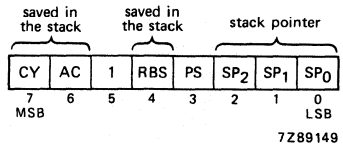


Fig. 18 Program status word.

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by the SEL RB instructions, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions and in the event of an interrupt. Bits 7, 6 and 4 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt service routine and can be used at the end of a normal subroutine. The RET instruction has no restore feature and cannot be used at the end of an interrupt service routine.

Program counter (see Fig. 19)

PCF84CXXX program counters can address up to 8 K bytes of ROM. The arrangement of the bits is shown in Fig. 17. The contents of the program counter are saved in the stack during CALL and interrupt routines.

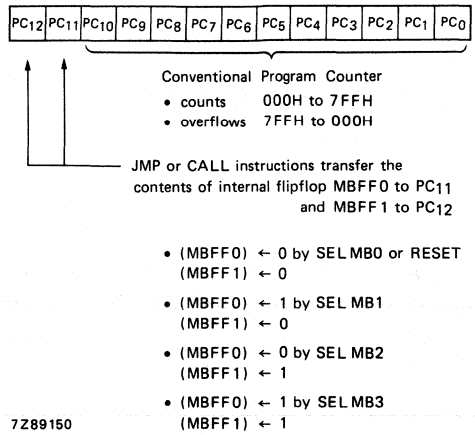


Fig. 19 Program counter.

Central processing unit

The PCF84CXXX has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the current ROM page.

Conditional branch logic

The conditional branch logic within the microcontroller enables several conditions, internal and external to the microcontroller, to be tested by the user's program. Table 4 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Table 4 Conditional branches

test	jump condition	jump instruction
accumulator	all bits zero	JZ
	any bit non-zero	JNZ
accumulator bit test	1	JB0 to JB7
carry flag	1	JC
	0	JNC
timer overflow flag	1	JTF
	0	JNTF
test input T0	1	JT0
	0	JNT0
test input T1	1	JT1
	0	JNT1
register	non-zero	DJNZ

FUNCTIONAL DESCRIPTION (continued)

Test input T1

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for $>$ 4 CP, and then HIGH for $>$ 4 CP. A transition can be recognized every 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. When T1 is not used, it must be tied to V_{DD} or V_{SS}.

Power-on-reset

The internal power-on reset circuit monitors the supply voltage V_{DD}. As long as the supply voltage remains below the internal reference level V_{ref} (typically 1,5 V), the oscillator is inhibited and RESET has an undefined level. When V_{DD} rises above the internal reference level, the oscillator is released and RESET is pulled high to V_{DD} by TR1 for a period t_D (typically 50 μs).

N.B. Because of the narrow bandwidth of the crystal, the start-up time of the oscillator is typically 10 ms.

Three cases of power-on reset are possible:

1. If V_{DD} can be switched with a fast rise time i.e. V_{DD} reaches its minimum operating value (corresponding to the selected oscillator frequency) before the RESET signal has finished (t_D), then no extra components are required (see Figs 20 and 21). Note that the first instruction is executed after the oscillator start-up time plus 1866 clock periods have elapsed.
2. If V_{DD} has a slow rise time then the RESET signal should be stretched by an external RC circuit (see Figs 22 and 23). In the event of a short drop in the supply voltage, the diode path rapidly discharges the capacitor to ensure a reliable power-on-reset. To ensure a correct reset, the RESET signal should reach at least 70% of the final value of V_{DD}. Given that the RESET voltage and V_{DD} rise exponentially, the above requirement is satisfied when the time constant τ of the RESET pulse is $>$ 8 times the time constant of V_{DD}. If V_{DD} rises linearly, then a RESET time constant $>$ 2 times the rise time of V_{DD} is required.

   When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods have elapsed (see Fig. 23). If the oscillator is started up prior to the completion of RESET, then program execution begins 1866 clock periods after RESET goes LOW.
3. Fig. 22 shows an external reset during power-on. The external reset signal must remain HIGH until V_{DD} has reached its minimum operating value corresponding to the selected oscillator frequency. When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods have elapsed (see Fig. 25). If the oscillator is started-up prior to the completion of RESET, then program execution begins 1866 clock periods after RESET goes LOW.

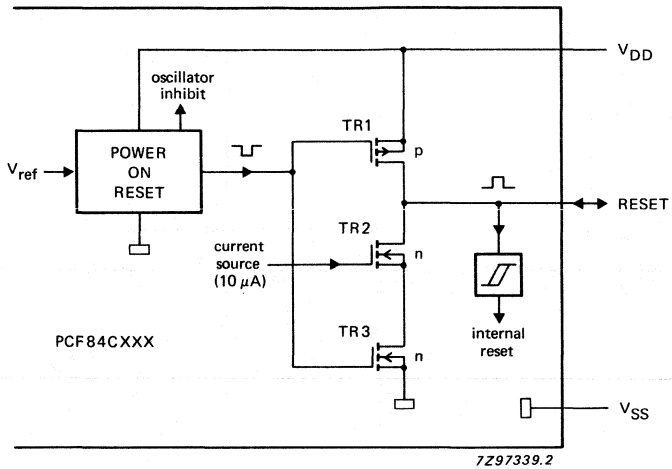


Fig. 20 Power-on-reset configuration.

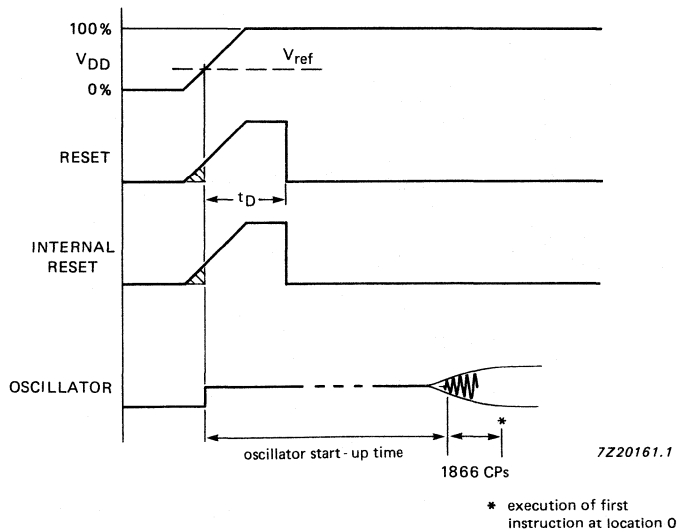


Fig. 21 Timing of power-on-reset with fast rise time.

FUNCTIONAL DESCRIPTION (continued)

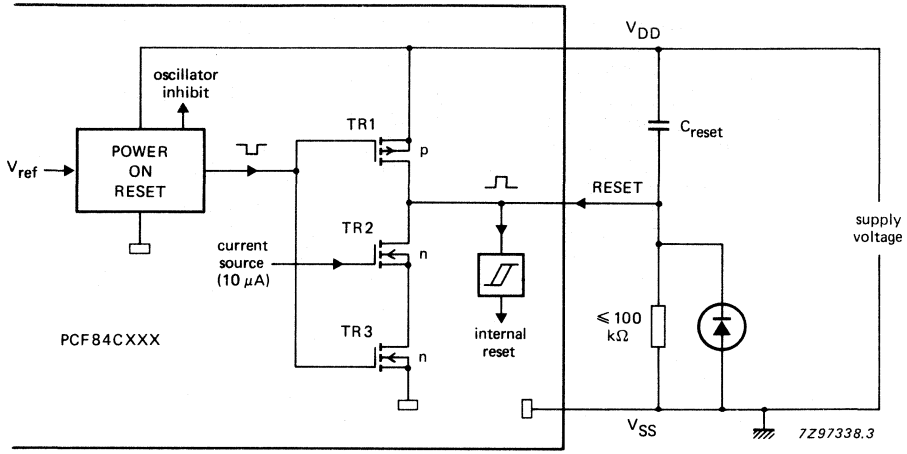


Fig. 22 Stretched power-on-reset with external components.

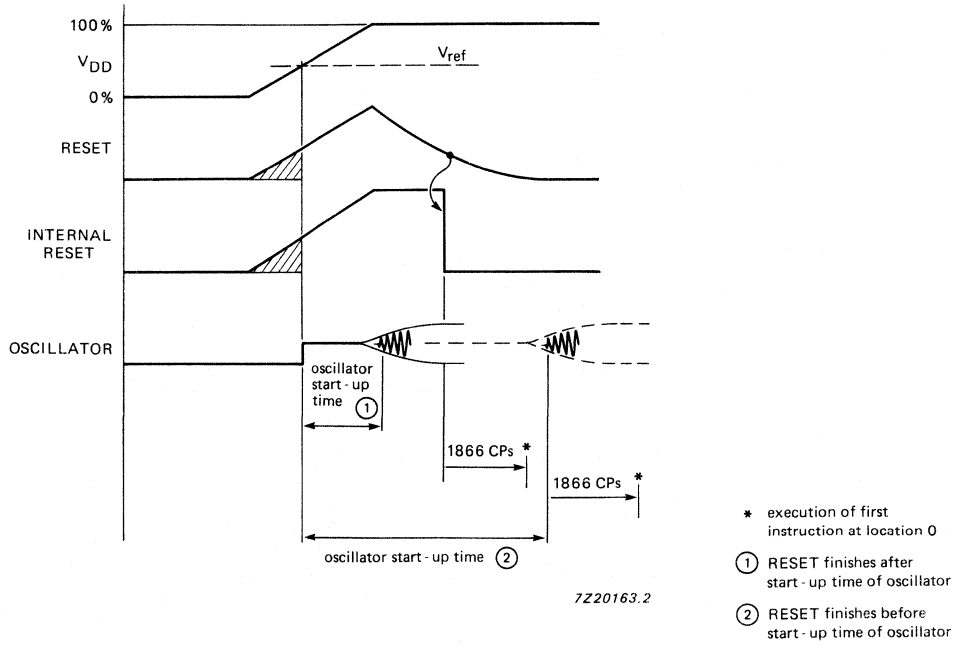


Fig. 23 Timing of power-on-reset with a slowly rising V_{DD} and a stretched RESET pulse.

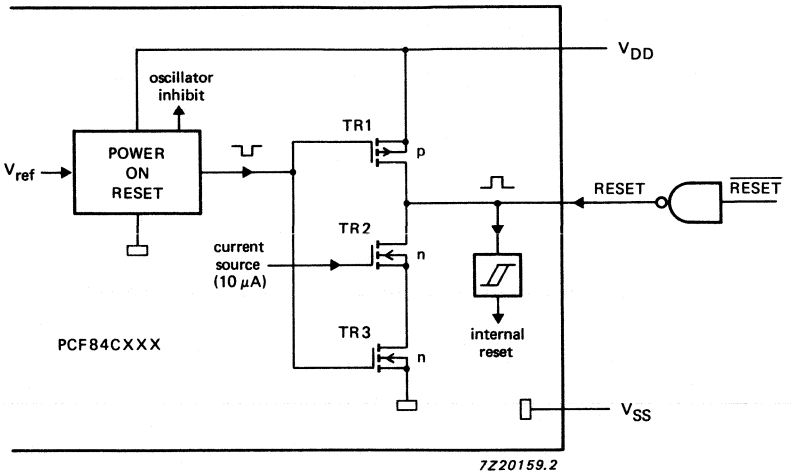


Fig. 24 External power-on-reset configuration.

DEVELOPMENT DATA

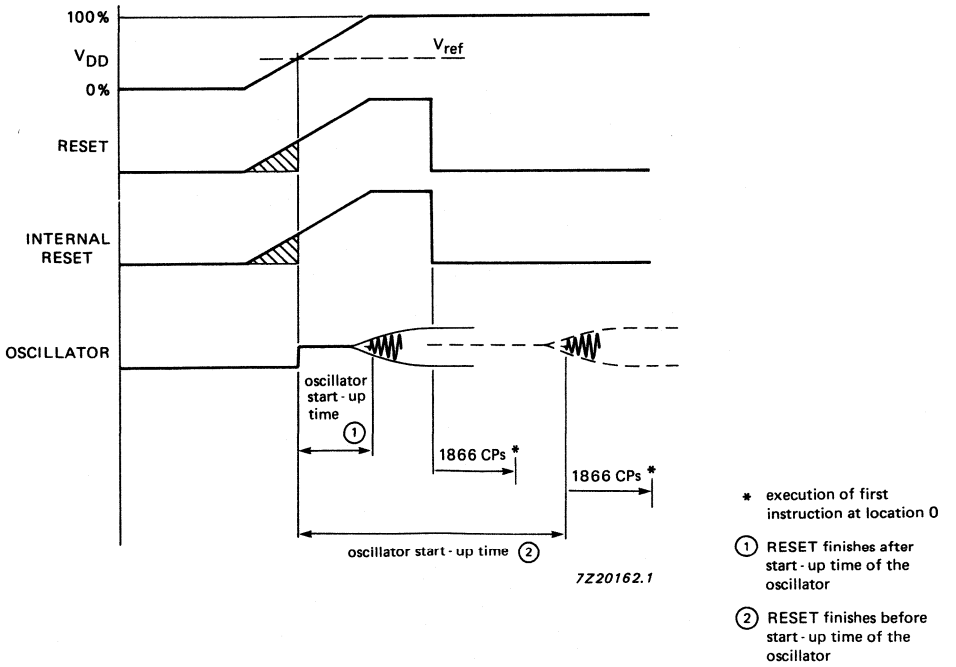


Fig. 25 Timing of external power-on-reset.

SINGLE-CHIP 8-BIT MICROCONTROLLERS WITH I²C-BUS INTERFACE

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84C00, PCF84C21/C, PCF84C41/C and PCF84C81/C microcontrollers. The PCF84C21C, PCF84C41C and PCF84C81C operate at a higher clock frequency. Each device has 20 quasi-bidirectional I/O port lines, a serial I/O interface, a single-level vectored interrupt structure, an 8-bit timer/event counter and on-chip clock oscillator and clock circuits. On-chip RAM and ROM content is as follows:

- PCF84C00 – 256 x 8 RAM, external program memory
- PCF84C21 – 64 x 8 RAM, 2 K x 8 ROM
- PCF84C41 – 128 x 8 RAM, 4 K x 8 ROM
- PCF84C81 – 256 x 8 RAM, 8 K x 8 ROM

These efficient controllers also perform well as arithmetic processors. They have facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set is similar to that of the MAB8048.

These microcontrollers are members of the PCF84CXXX family. For detailed information, consult the PCF84CXXX data sheet.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 2K, 4 K or 8 K x ROM; also a ROM-less version
- 64, 128 or 256 x 8 RAM
- 20 quasi-bidirectional I/O port lines
- Two test inputs, one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter and serial I/O
- I²C hardware interface for serial data transfer on two lines (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz ; C versions: 1 MHz to 12 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2,5 to 5,5 V)
- STOP and IDLE modes
- Power-on reset circuit
- Operating temperature range: −40 to +85 °C
- High current on Port 1: I_{OL} = 10 mA at V_{OL} = 1,2 V (all versions except the PCF84C00).

For following sections see PCF84XXX family data sheet

Program memory
Data memory
Program counter stack
IDLE and STOP modes
I/O facilities
Serial I/O
Interrupts
Oscillator
Timer/event counter
Program status word

Program counter
Central processing unit
Conditional branch logic
Test input T1

Power-on reset
Instruction set

PACKAGE OUTLINES

PCF84C21/41/81P: 28-lead DIL; plastic (SOT117).
PCF84C21/41/81T: 28-lead mini-pack; plastic (SO28; SOT136A).
PCF84C00B : 28-lead 'piggy-back' package (supports up to 28-pin EPROM).
PCF84C00T : 56-lead mini-pack; plastic (VSO56; SOT190).

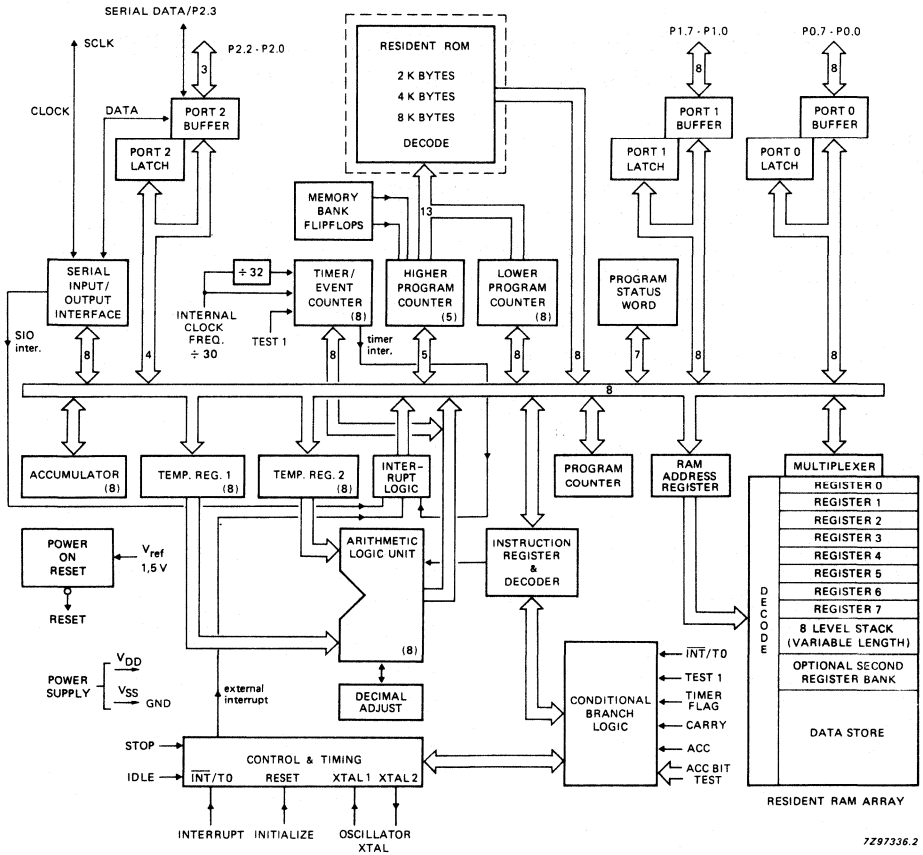


Fig. 1 Block diagram.

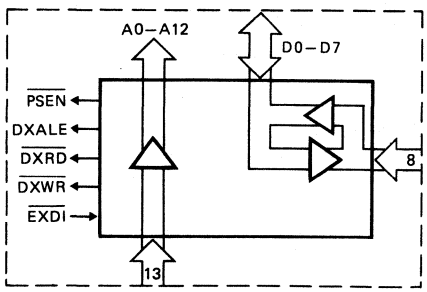


Fig. 1a Replacement of dotted section in Fig. 1, for the PCF84C00T ROM-less version.

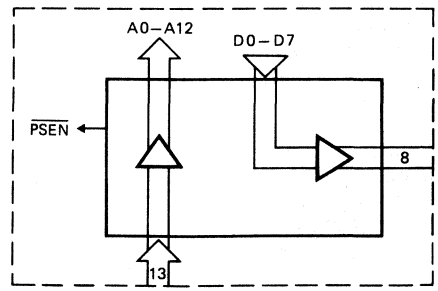


Fig. 1b Replacement of dotted section in Fig. 1, for the PCF84C00B 'piggy-back' version.

PINNING

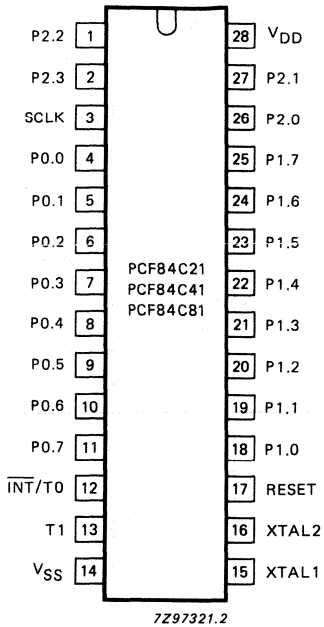


Fig. 2 Pinning diagram.

PIN DESIGNATION

Pin	*Symbol*	*Type*	*Function*
3	SCLK	I/O	**Clock:** bidirectional clock for serial I/O.
4-11	P0.0-P0.7	I/O	**Port 0:** 8-bit quasi-bidirectional I/O port.
12	$\overline{\text{INT}}$/T0	I	**Interrupt/Test 0:** external interrupt input (negative edge triggered)/ test input pin; when used as a test input, this pin is directly tested by conditional branch instructions JT0 and JNT0.
13	T1	I	**Test 1:** test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 may also be selected as an input to the 8-bit timer/event counter via the STRT CNT instruction.
14	V_{SS}	I	**Ground:** circuit earth potential.
15	XTAL 1	I	**Oscillator input:** input from a crystal which determines the internal oscillator frequency or an external clock generator.
16	XTAL 2	I/O	**Oscillator output:** output of the inverting amplifier.
17	RESET	I/O	**Reset input:** used to initialize the microcontroller (active HIGH); also output of power-on-reset circuit.
18-25	P1.0-P1.7	I/O	**Port 1:** 8-bit quasi-bidirectional I/O port.
26, 27, 1, 2	P2.0-P2.3	I/O	**Port 2:** 4-bit quasi-bidirectional I/O port. P2.3 is the serial data input/output in serial I/O mode.
28	V_{DD}	I	**Power supply:** 2,5 V to 5,5 V.

PINNING (continued)

Pin diagram of the PCF84C00B 'piggy-back' version

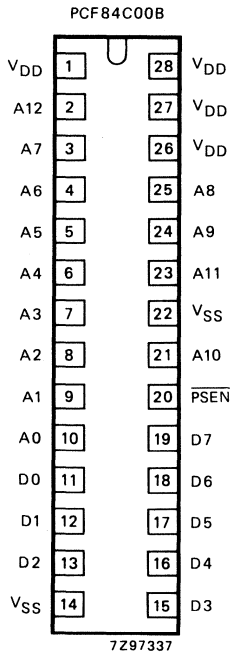


Fig. 3(a) Pinning diagram (top pins) of the PCF84C00B 'piggy-back' version.

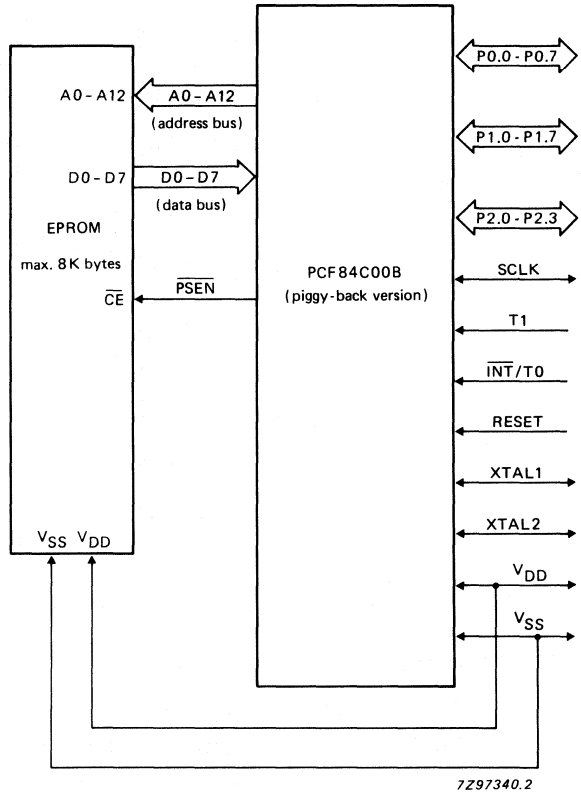


Fig. 3(b) Connection of EPROM to the PCF84C00B 'piggy-back' version.

The PCF84C00B is mainly used for prototyping and for low volume production applications. This device is packaged in a 'piggy-back' package. i.e. a 4 K or 8 K byte EPROM (2732 or 2764) may be mounted in the 24/28 pin socket on top of the package.

Notes

1. The PCF84C00B has 256 bytes of on-chip RAM.
2. Access time for ROMS/EPROMS must be less than 7 x $1/f_{XTAL}$.
3. Bottom pinning is identical to that of Fig. 2.

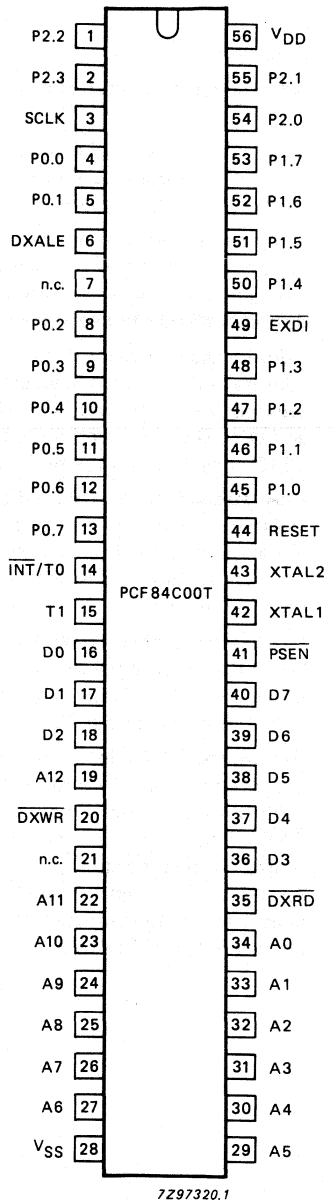


Fig. 4 Pinning diagram; ROM-less version PCF84C00T.

The PCF84C00T may be used for prototyping future derivatives of the PCF84CXX family or for low volume production applications. This device is packaged in a 56-lead VSO outline. Additional signals are available (see pinning information following) to control external program memory and derivative functions.

PIN FUNCTION (continued)

Pin	*Symbol*	*Type*	*Function*
34-29, 27-22, 19	A00-A12	O	**Address bus.** For external memory and pheripherals.
16-18, 36-40	D0-D7	I/O	**Data bus.** For external memory and pheripherals. The specified STOP mode supply current is valid only if external pull-ups are connected to all data lines.
41	$\overline{\text{PSEN}}$	O	**Program store enable** (active LOW). $\overline{\text{PSEN}}$ is used to enable external program memory and is active during TS9 and TS10 of each machine cycle and TS1 of each following cycle. $\overline{\text{PSEN}}$ is HIGH during the STOP mode.
6	DXALE	O	**Address latch enable.** On the falling edge of DXALE, the Dx address can be latched in an external latch. This signal occurs only during execution of the MOV Dx,A, MOV A,Dx, ANL Dx,A and ORL Dx,A instructions, with x = 0 to 255. It is active during TS10 of cycle 1 and the first half of TS1 of cycle 2.
35	$\overline{\text{DXRD}}$	O	**Read strobe** (active LOW). When this signal is active, external registers emulating Dx registers can be read by the data bus. This signal occurs only during execution of MOV A,Dx, ANL Dx,A and ORL Dx,A instructions, with x = 0 to 255. It is active during TS3 and TS4 of cycle 2.
20	$\overline{\text{DXWR}}$	O	**Write strobe** (active LOW). On the rising edge, data on D0-D7 may be written to external registers. This signal occurs only during MOV Dx,A, ANL Dx,A and ORL Dx,A instructions, with x = 0 to 255. It is active during TS7 of cycle 2.
49	$\overline{\text{EXDI}}$	I	**External derivative interrupt** (active LOW). $\overline{\text{EXDI}}$ is 'OR-ed' with the internal serial interrupt and can be used to initiate an interrupt from external hardware emulating derivative functions. $\overline{\text{EXDI}}$ is pulled HIGH internally. The derivative interrupt is polled during time slot TS6*, and is only accepted if an EN SI instruction has been executed and the device is not already executing an interrupt routine. Derivative interrupts are not latched in the PCF84C00.

* The interrupt signal must remain active until the vector address (05 H) is present on the address bus.

FUNCTIONAL DESCRIPTION

ROM-less version PCF84C00T

The PCF84C00T microcontroller contains no on-chip ROM, but has all address and data lines brought out to access an external ROM or EPROM. This version has more pins than the PCF84CXXX with on-chip ROM (see Fig. 1a). The PCF84C00T can address up to 8 K bytes of external program memory, and has 256 bytes of internal data RAM.

'Piggy-back' version PCF84C00B

The PCF84C00B package has standard pinning on the bottom to facilitate insertion as a mask-programmed device. An EPROM can be mounted on top in an additional socket. The total package height is greater than the height of a standard DIL package. The PCF84C00B can address up to 8 K bytes of external ROM/RAM, and has 256 bytes of internal data RAM.

Program memory

The program memory consists of 2, 4 or 8 K bytes of read-only memory (ROM). Each location is directly addressable by the program counter. The ROM is mask-programmed at the factory.

Data memory

Data memory consists of 64, 128 or 256 bytes of random-access memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer.

I/O facilities

Each device has 23 I/O lines arranged as follows:

- Port 0 — 8-bit parallel port (P0.0-P0.7)
- Port 1 — 8-bit parallel port (P1.0-P1.7)
- Port 2 — 4-bit parallel port (P2.0-P2.3)
- SCLK — serial I/O clock line
- $\overline{\text{INT}}$/T0 — external interrupt and test input. When used as a test input, it can be directly tested by conditional branch instructions JT0 and JNT0
- T1 — test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter

Reset

A positive-going signal on the RESET input/output:

- Sets the program counter to zero
- Selects location 0 of memory bank 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external, timer and serial I/O)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to divide by 32
- Resets the timer flag
- Sets all ports except P2.3 to input mode
- Sets the serial I/O to slave receiver mode and disables the serial I/O
- Cancels IDLE and STOP mode

A negative-going signal on the RESET input/output:

- Sets P2.3/SDA and SCLK to HIGH after a maximum of 30 clock pulses
- Sets the serial I/O to slave receiver mode and disables the serial I/O after a maximum of 30 clock pulses
- Starts program execution after 1866 clock pulses

INSTRUCTION SET

The instruction set consists of over 80 one and two byte instructions. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 3 contains the instruction set. Table 2 shows the instruction map and Table 1 details the symbols that are used.

Table 1 Symbols and definitions used in Table 3

symbol	description
A	accumulator
addr	program memory address
Bb	bit designation (b = 0-7)
RBS	register bank select
C	carry bit (bit CY)
CNT	event counter
Dx	mnemonic derivative register (x = 0 ... 255)
direct	8-bit derivative register address
data	8-bit number or expression
I	interrupt
MB	memory bank
MBFF	memory bank flip-flop
P	mnemonic for 'in-page' operation
PC	program counter
Pp	port designation (p = 0, 1 or 2)
PSW	program status word
RB	register bank
Rr	register designation (r = 0-7)
Sn	serial I/O register
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with

INSTRUCTION SET (continued)

Table 2 Instruction map

first hexadecimal character of opcode ↓ / second hexadecimal character of opcode →	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A, # data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0	IN A,Pp 1	IN A,Pp 2		MOV A,Sn 0	MOV A,Sn 1		
1	INC @Rr 0	INC @Rr 1	JB0 addr	ADDC A, # data	CALL page 0	DIS I	JTF addr	INC A	0	1	2	INC Rr 3	4	5	6	7
2	XCH A,@Rr 0	XCH A,@Rr 1	STOP	MOV A, # data	JMP page 1	EN TCNTI	JNT0 addr	CLR A	0	1	2	XCH A,Rr 3	4	5	6	7
3	XCHD A,@Rr 0	XCHD A,@Rr 1	JB1 addr		CALL page 1	DIS TCNTI	JT0 addr	CPL A	OUTL Pp,A 0	OUTL Pp,A 1	OUTL Pp,A 2		MOV Sn,A 0	MOV Sn,A 1	MOV Sn,A 2	
4	ORL A,@Rr 0	ORL A,@Rr 1	MOV A, T	ORL A, # data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	0	1	2	ORL A,Rr 3	4	5	6	7
5	ANL A,@Rr 0	ANL A,@Rr 1	JB2 addr	ANL A, # data	CALL page 2	STRT T	JT1 addr	DA A	0	1	2	ANL A,Rr 3	4	5	6	7
6	ADD A,@Rr 0	ADD A,@Rr 1	MOV T, A		JMP page 3	STOP TCNT		RRC A	0	1	2	ADD A,Rr 3	4	5	6	7
7	ADDC A,@Rr 0	ADDC A,@Rr 1	JB3 addr		CALL page 3			RR A	0	1	2	ADDC A,Rr 3	4	5	6	7
8				RET	JMP page 4	EN SI			ORL Pp, # data 0	ORL Pp, # data 1	ORL Pp, # data 2		MOV A, Dx	MOV Dx, A	ANL Dx, A	ORL Dx, A
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,# data 0	ANL Pp,# data 1	ANL Pp,# data 2		MOV Sn,# data 0	MOV Sn,# data 1	MOV Sn,# data 2	
A	MOV @Rr,A 0	MOV @Rr,A 1		MOVP A,@A	JMP page 5	SEL MB2		CPL C	0	1	2	MOV Rr,A 3	4	5	6	7
B	MOV @Rr, # data 0	MOV @Rr, # data 1	JB5 addr	JMPP @A	CALL page 5	SEL MB3			0	1	2	MOV Rr, # data 3	4	5	6	7
C	DEC @Rr 0	DEC @Rr 1			JMP page 6	SEL RB0	JZ addr	MOV A, PSW	0	1	2	DEC Rr 3	4	5	6	7
D	XRL A,@Rr 0	XRL A,@Rr 1	JB6 addr	XRL A,# data	CALL page 6	SEL RB1		MOV PSW, A	0	1	2	XRL A,Rr 3	4	5	6	7
E	DJNX @Rr, addr 0	DJNX @Rr, addr 1			JMP page 7	SEL MB0	JNC addr	RL A	0	1	2	DJNZ Rr, addr 3	4	5	6	7
F	MOV A,@Rr 0	MOV A,@Rr 1	JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	0	1	2	MOV A,Rr 3	4	5	6	7

Table 3 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) −1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1}) \leftarrow A_n$ $(A_0) \leftarrow (C), (C) \leftarrow (A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (C), (C) \leftarrow (A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7}) \leftrightarrow (A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data		
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3}) \leftrightarrow ((R0_{0-3}))$ $(A_{0-3}) \leftrightarrow ((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3) \leftarrow (A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7}) \leftarrow (A), (A) \leftarrow ((PC))$		
FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2

INSTRUCTION SET (continued)

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1 r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1	
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1 r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1	
BRANCH	JMP addr	● 4 addr	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))	
	DJNZ Rr, addr	E* addr	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 r = 0–7 if (Rr) not zero (PC_{0-7})←addr	
	DJNZ @Rr, addr	E0	2/2	decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr	
		E1			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr	
	JBb addr	▲ 2 addr	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr b = 0–7	
	JC addr	F6 addr	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr	
	JNC addr	E6 addr	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr	
	JZ addr	C6 addr	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr	
	JNZ addr	96 addr	2/2	jump to addr if A is NOT zero	if A ≠ 0 : (PC_{0-7})←addr	
	JT0 addr	36 addr	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr	
	JNT0 addr	26 addr	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr	
	JT1 addr	56 addr	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr	
	JNT1 addr	46 addr	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr	
	JTF addr	16 addr	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr	4
	JNTF addr	06 addr	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr	

TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	10
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	10
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	10
	STOP	22	1/1	enter STOP mode		
	IDLE	01	1/1	enter IDLE mode		
SUBROUTINE	CALL addr	▲ 4 addr	2/2	jump to subroutine	((SP))←(PC), ($PSW_{4, 6, 7}$) (SP)←(SP) + 1 (PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1	6
	RET	83	1/2	return from subroutine	(SP)←(SP) − 1 (PC)←((SP))	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	(SP)←(SP) − 1 ($PSW_{4, 6, 7}$) + (PC)←((SP))	6

INSTRUCTION SET (continued)

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	 7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 data 99 data 9A data	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 data 89 data 8A data	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
DERIVATIVE INPUT/OUTPUT	MOV A, Dx	8C direct	2/2	move derivative register contents to accumulator	(A)←(Dx) x = 0 to 255	8
	MOV Dx, A	8D direct	2/2	move accumulator contents to derivative register	(Dx)←(A) x = 0 to 255	8
	ANL Dx, A	8E direct	2/2	AND derivative register with accumulator	(Dx)←(Dx) AND (A) x = 0 to 255	8
	ORL Dx, A	8F direct	2/2	OR derivative register with accumulator	(Dx)←(Dx) OR (A) x = 0 to 255	8

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
SERIAL INPUT/OUTPUT	MOV A, S_n	0C 0D	1/2	move serial I/O register contents to accumulator	(A)←(S0) (A)←(S1)	9
	MOV S_n, A	3C 3D 3E	1/2	move accumulator contents to serial I/O register	(S0)←(A) (S1)←(A) (S2)←(A)	
	MOV S_n, #data	9C data 9D data 9E data	2/2	move immediate data to serial I/O register	(S0)←data (S1)←data (S2)←data	
	EN SI	85	1/1	enable serial I/O interrupt		
	DIS SI	95	1/1	disable serial I/O interrupt		
	NOP	00	1/1	no operation		

Notes to Table 3

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of a JTF or JNTF instruction resets the Timer Flag (TF).
5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 0000, P2.3, P2.2, P2.1, P2.0.
8. Instructions for PCF84C00T only.
9. (S1) has a different meaning for read and write operation, see serial I/O interface.
10. SEL MB1, SEL MB2 and SEL MB3 may not be used within interrupt routines.

* : 8, 9, A, B, C, D, E, F
● : 0, 2, 4, 5, 6, A, C, E
▲ : 1, 3, 5, 7, 9, B, D, F

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,8 to +8	V
All input voltages	V_I	−0,5 to V_{DD} +0,5	V
DC current into any input or output	$\pm I_I$, $\pm I_O$	max. 10	mA
Total power dissipation (see note)	P_{tot}	max. 125	mW
Storage temperature range	T_{stg}	−65 to +150	°C
Operating ambient temperature range (if P_{tot} max. = 100 mW)	T_{amb}	−40 to +70	°C
Operating ambient temperature range (if P_{tot} max. = 30 mW)	T_{amb}	−40 to +85	°C
Operating junction temperature	T_j	max. 90	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

Note

Thermal resistance (junction to ambient)

for SOT-117	$R_{th\ j\text{-}a}$	max. 120	K/W
for SOT-136A	$R_{th\ j\text{-}a}$	max. 150	K/W
for SOT-190	$R_{th\ j\text{-}a}$	max. 110	K/W

DC CHARACTERISTICS

V_{DD} = 2,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; all voltages with respect to V_{SS}; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating (see Fig. 9)	V_{DD}	2,5	–	5,5	V
Supply current					
operating (see Fig. 10; not valid for PCF84C00)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz (note 2)	I_{DD}	–	1,6	3,2	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz (note 2)	I_{DD}	–	1	2	mA
at V_{DD} = 3 V; f_{XTAL} = 3,58 MHz (note 2)	I_{DD}	–	0,3	0,6	mA
IDLE mode (see Fig. 11; not valid for PCF84C00)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz (note 2)	I_{DD}	–	0,8	1,6	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz (note 2)	I_{DD}	–	0,5	1	mA
at V_{DD} = 3 V; f_{XTAL} = 3,58 MHz (note 2)	I_{DD}	–	0,15	0,4	mA
STOP mode (see Fig. 17, note 1 and note 2)					
at V_{DD} = 2,5 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 2,5 V; T_{amb} = 85 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	V_{DD}	V
Input leakage current					
at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output sink current LOW					
at V_{DD} = 5 V ± 10%; V_O = 0,4 V					
except P2.3/SDA, SCLK (see Fig. 13) and port 1	I_{OL}	1,6	3	–	mA
P2.3/SDA, SCLK (see Fig. 14)	I_{OL}	3	–	–	mA
P1.0-P1.7 (not PCF84C00) at V_{OL} = 1,2 V	I_{OL}	10	–	–	mA
Pull-up output source current HIGH (see Fig. 15)					
at V_{DD} = 5 V ± 10%; V_O = $0,7V_{DD}$	$-I_{OH}$	40	–	–	μA
at V_{DD} = 5 V ± 10%; V_O = V_{SS}	$-I_{OH}$	–	–	400	μA
Push-pull output source current HIGH					
at V_{DD} = 5 V ± 10%; V_O = V_{DD}−0,4 V	$-I_{OH}$	1,6	3	–	mA

Note 1: Crystal connected between XTAL1 and XTAL2; T1 = V_{SS}; $\overline{INT}$ = V_{DD}.

Note 2: V_{IL} = V_{SS}; V_{IH} = V_{DD}; all outputs unloaded; all open drain outputs connected to V_{SS}.

AC CHARACTERISTICS

V_{DD} = 2,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C. All voltages with respect to V_{SS} unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Rise time all outputs (note 1)	t_R	–	30	–	ns
Fall time all outputs (note 1)	t_F	–	30	–	ns
Cycle time (= 30 CP; note 2)	t_{CY}	3	–	30	μs
PCF84C00/non-standard pins:					
Control pulse width	t_{CC}	–	9	–	CP
Address to $\overline{PSEN}$ set-up	t_{AS}	–	1,5	–	CP
Data to $\overline{PSEN}$ set-up	t_{DS}	–	2	–	CP
Data hold time	t_{DR}	0	–	–	ns
Data out to $\overline{DWXR}$ set-up	t_{SDO}	–	2	–	CP
Data out to $\overline{DXWR}$ hold	t_{HDO}	–	1	–	CP
Time from DXALE to $\overline{PSEN}$	t_{SLPH}	–	1,5	–	CP
Data-in to $\overline{DXRD}$ set-up	t_{DS1}	–	2,5	–	CP
Data-in to $\overline{DXRD}$ hold	t_{DR1}	0	–	–	ns
HIGH time of DXALE	t_{DXALE}	–	4,5	–	CP
LOW time of $\overline{DXRD}$	t_{DXRD}	–	6	–	CP
LOW time of $\overline{DXWR}$	t_{DXWR}	–	3	–	CP

Notes:

1. At V_{DD} = 5 V; T_{amb} = + 25 °C; C_L = 50 pF.
2. 1 Time slot (TS) = 3 CP, 1 clock pulse (CP) = $1/f_{XTAL}$.

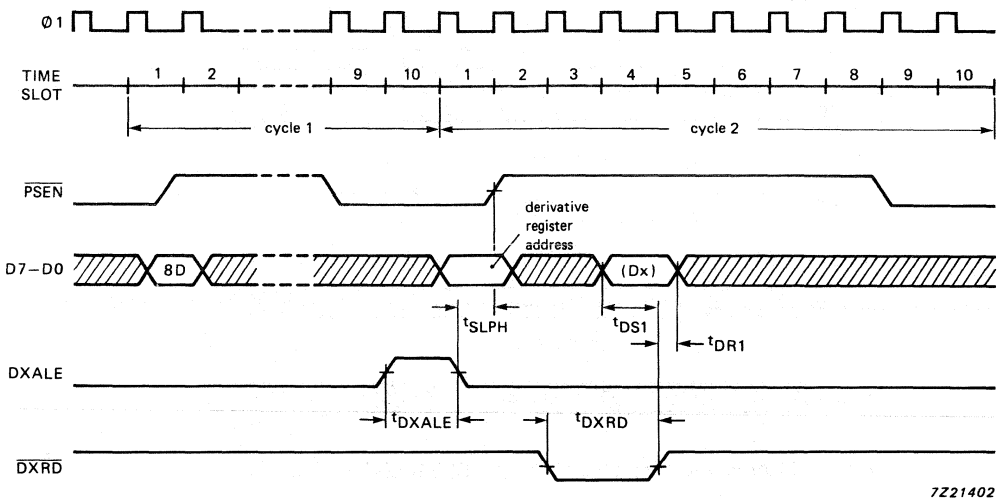


Fig. 5 MOV A,Dx timing (PCF84C00T only).

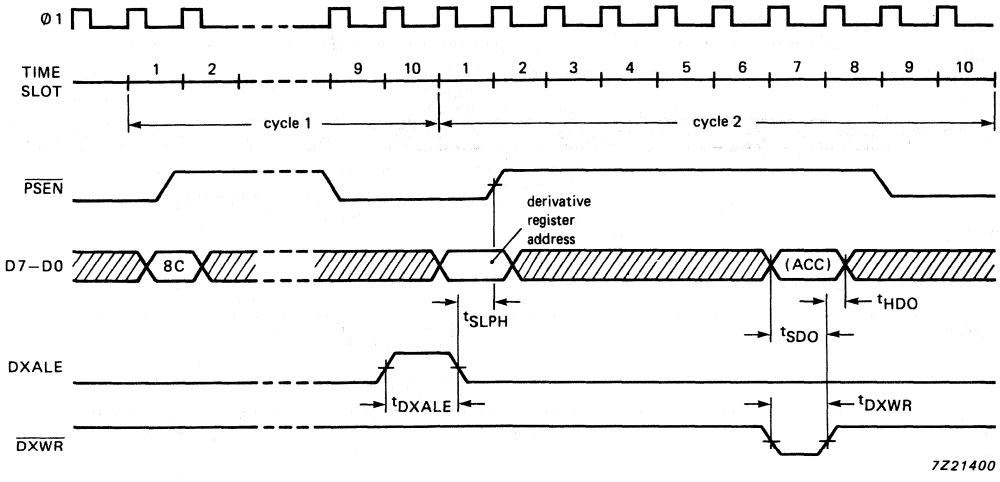


Fig. 6 MOV Dx,A timing (PCF84C00T only).

AC CHARACTERISTICS (continued)

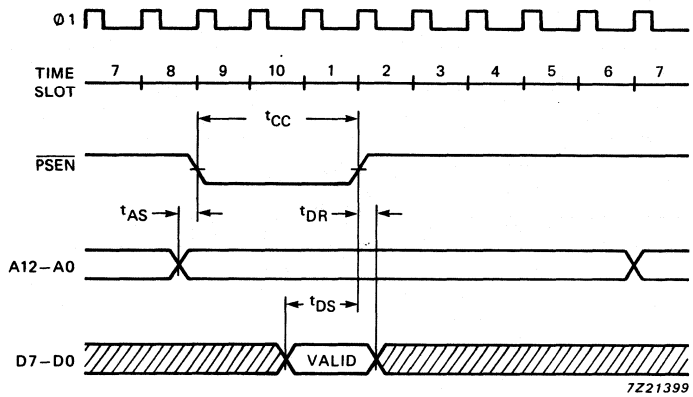


Fig. 7 External memory access timing (PCF84C00T and PCF8400B).

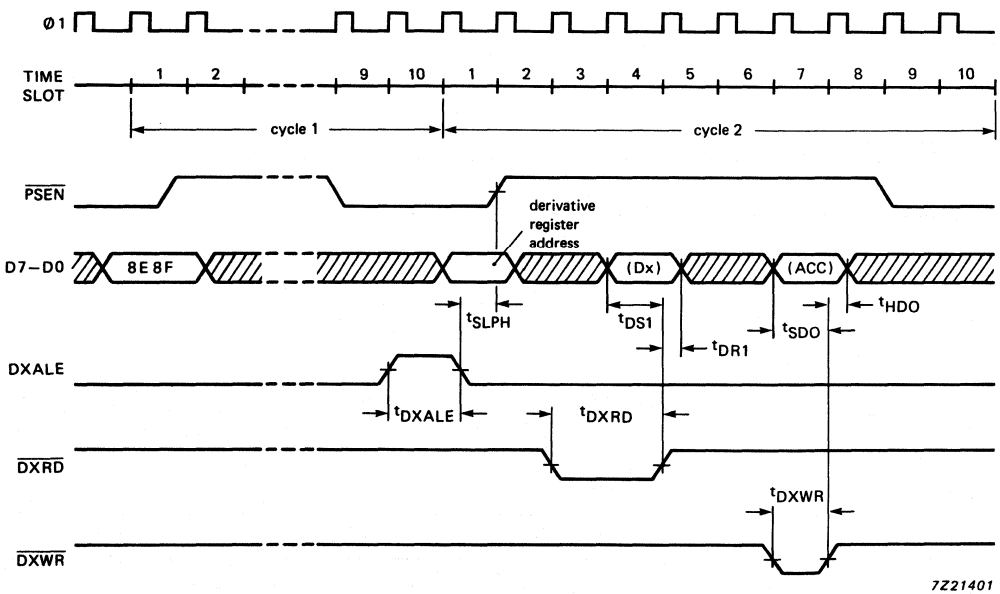


Fig. 8 ANL/ORL derivative interface timing (PCF84C00T only).

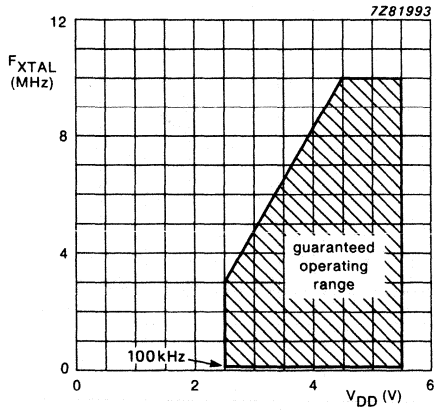


Fig. 9(a) Maximum clock frequency (f_{XTAL}) as a function of the supply voltage (PCF84C00, PCF84C21, PCF84C41 and PCF84C81).

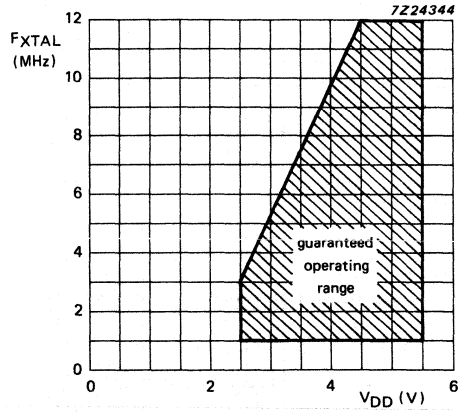
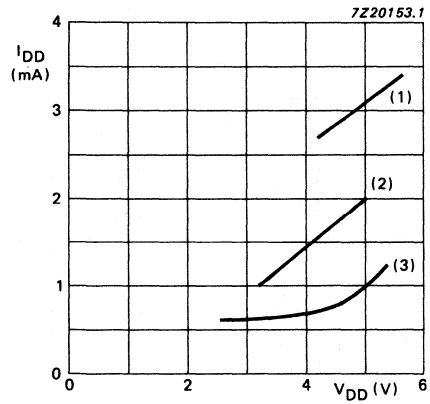
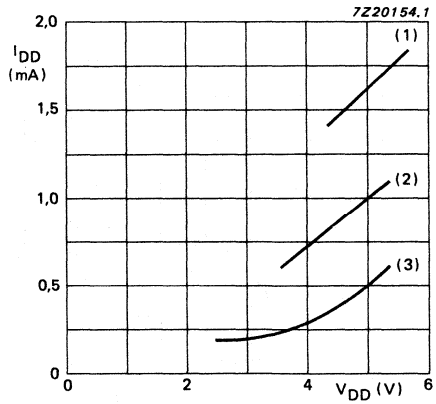


Fig. 9(b) Maximum clock frequency (f_{XTAL}) as a function of the supply voltage (PCF84C21C, PCF84C41C and PCF84C81C).



(1) clock frequency = 10 MHz
(2) clock frequency = 6 MHz
(3) clock frequency = 3,58 MHz

Fig. 10 Maximum supply current (I_{DD}) in operation mode as a function of the supply voltage (V_{DD}).



(1) clock frequency = 10 MHz
(2) clock frequency = 6 MHz
(3) clock frequency = 3,58 MHz

Fig. 11 Maximum supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}).

AC CHARACTERISTICS (continued)

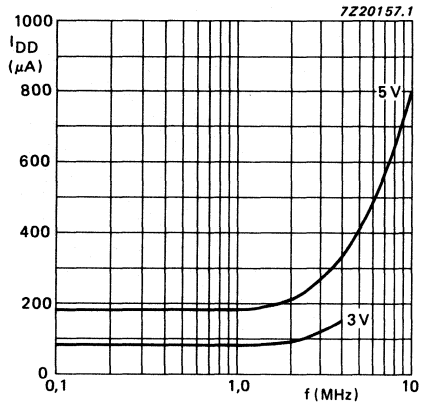


Fig. 12 Typical supply current during IDLE mode as a function of frequency at V_{DD} = 3 V and V_{DD} = 5 V.

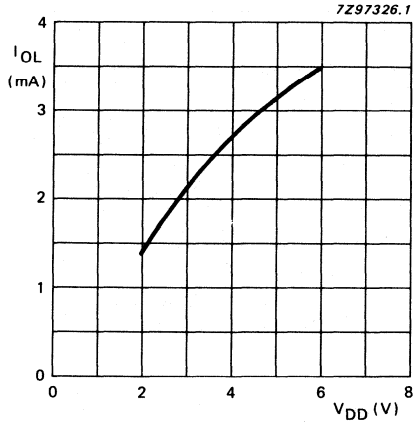


Fig. 13 Typical output sink current (I_{OL}), outputs P0.0 to P0.7 and P2.0 to P2.2, as a function of the supply voltage (V_{DD}); V_O = 0,4 V.

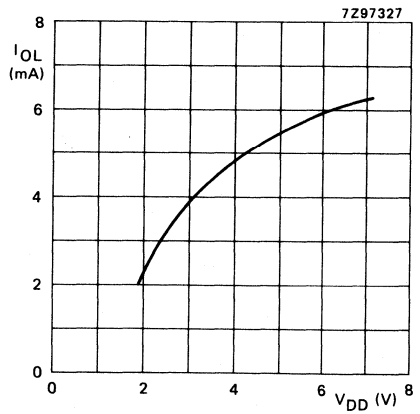


Fig. 14(a) Typical output sink current (I_{OL}), outputs P2.3/SDA and SCLK, as a function of the supply voltage (V_{DD}); V_O = 0,4 V.

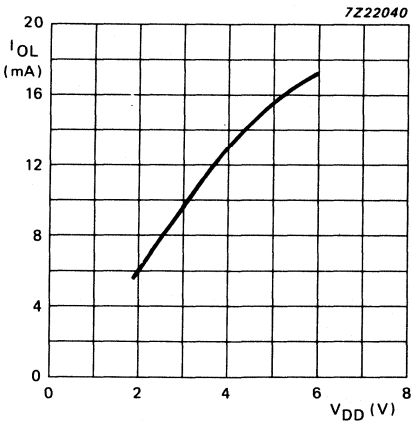
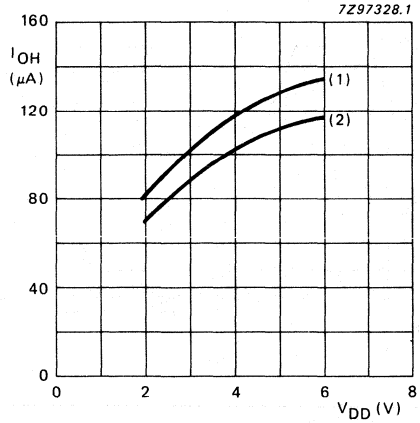


Fig. 14(b) Typical output sink current (I_{OL}), outputs P1.0 to P1.7, as a function of the supply voltage (V_{DD}); V_O = 1,2 V.



(1) $V_O = V_{SS}$
(2) $V_O = 0{,}7\ V_{DD}$

Fig. 15 Typical output source current ($-I_{OH}$) as a function of the supply voltage (V_{DD}).

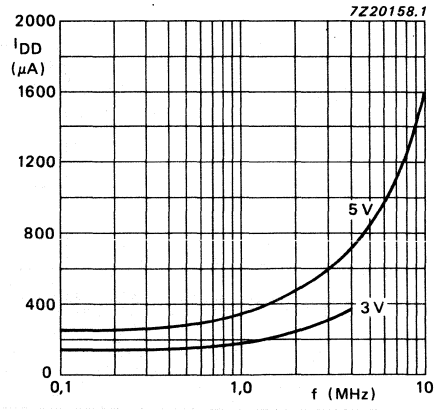
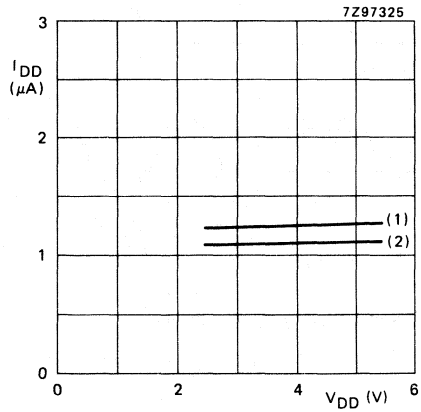


Fig. 16 Typical supply current during operating mode as a function of frequency at V_{DD} = 3 V and V_{DD} = 5 V.



(1) T_{amb} = 85 °C
(2) T_{amb} = 25 °C

Fig. 17 Typical supply current (I_{DD}) in STOP mode as a function of the supply voltage (V_{DD}).

Table 4 Input timing shown in Fig. 18

symbol	timing
t_{BUF}	$\geqslant 14t_{XTAL}$
$t_{HD;STA}$	$\geqslant 14t_{XTAL}$
t_{HIGH}	$\geqslant 17t_{XTAL}$
t_{LOW}	$\geqslant 17t_{XTAL}$
$t_{SU;STO}$	$\geqslant 14t_{XTAL}$
$t_{HD;DAT}$	> 0
$t_{SU;DAT}$	$\geqslant 250$ ns
t_{RD}	$\leqslant 1\ \mu s$
t_{RC}	$\leqslant 1\ \mu s$
t_{FD}	$\leqslant 1\ \mu s$
t_{FC}	$\leqslant 0{,}3\ \mu s$

Notes to Table 4

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 167 ns for f_{XTAL} = 6 MHz
These figures apply to all modes.

AC CHARACTERISTICS (continued)

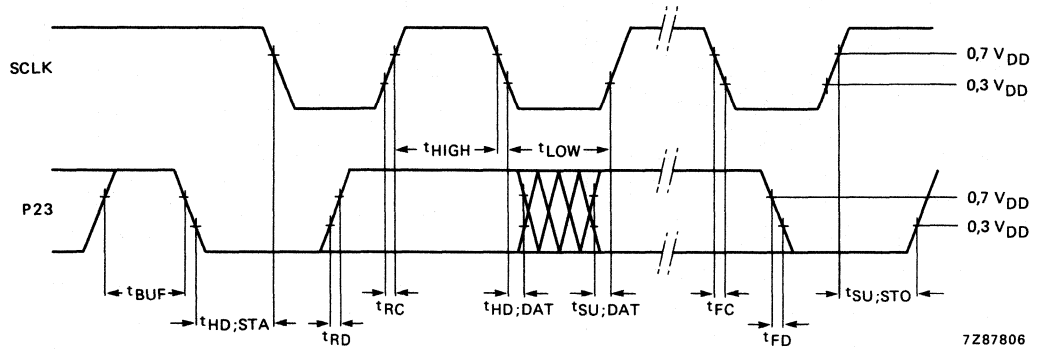


Fig. 18 Timing requirements for the P2.3 and SCLK *input* signals.

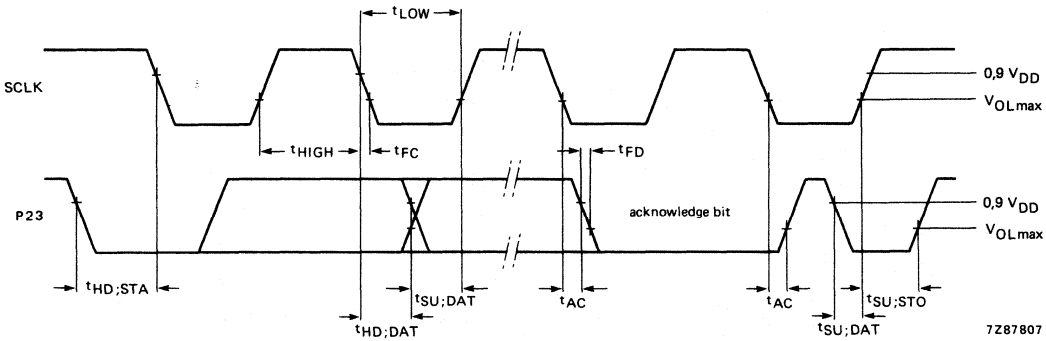


Fig. 19 Timing requirements for the P2.3 and SCLK *output* signals.

Table 5 Output timing shown in Fig. 19

symbol	timing	
	normal mode (ASC in S2 = 0)	low-speed mode (ASC in S2 = 1)
$t_{HD;STA}$	$\frac{1}{2}$ (DF + 9) t_{XTAL}	$\frac{3}{4}$ (DF + 9) t_{XTAL}
t_{HIGH}	$\frac{1}{2}$ (DF) t_{XTAL}	$\frac{3}{4}$ (DF) t_{XTAL}
t_{LOW}	$\frac{1}{2}$ (DF) t_{XTAL}	$\frac{1}{4}$ (DF) t_{XTAL}
$t_{SU;STO}$	$\frac{1}{2}$ (DF − 3) t_{XTAL}	$\frac{1}{4}$ (DF − 3) t_{XTAL}
$t_{HD;DAT}$ (slave transmitter) any DF	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{HD;DAT}$ (master transmitter) for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	– –
for DF $\leqslant$ 99	– –	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{SU;DAT}$ (master transmitter) for DF > 51	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$	– –
for DF > 99	– –	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$
t_{AC}	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
t_{FD}, t_{FC}	$\leqslant$ 100 ns at C_b = 400 pF	$\leqslant$ 100 ns at C_b = 400 pF

Notes to Table 5

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 167 ns for f_{XTAL} = 6 MHz
DF = divisor (see Table 2 Serial I/O section).
C_b = the maximum bus capacitance for each line.

AC CHARACTERISTICS (continued)

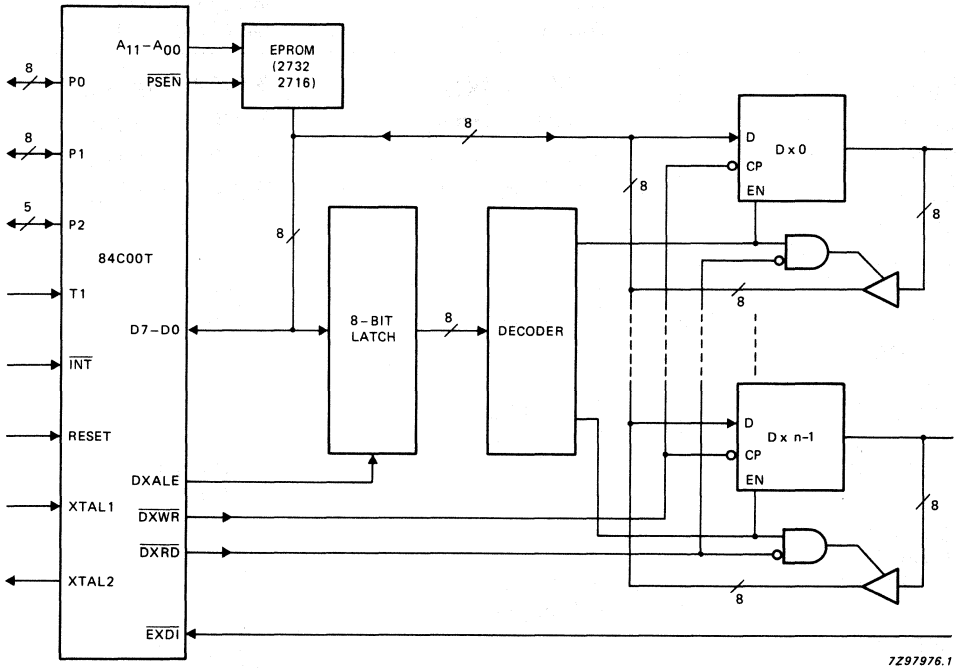


Fig. 20 Block diagram of the external Dx register interface.
The Dx interface can only be used with the PCF84C00T.

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 32 I/O LINES

DESCRIPTION

The PCF84C85 microcontroller is manufactured in CMOS, and is designed to be an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048 and is software compatible with the PCF84CXX family. The PCF84C85 has two additional derivative ports and the microcontroller has bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information on the PCF84CXX see the "Single-chip 8-bit Microcontrollers" user manual.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead DIL or mini-pack package
- 8 K ROM
- 256 RAM bytes
- 32 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C hardware interface for two-line serial data transfer
  (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V
- STOP and IDLE mode
- Power-on-reset circuit
- Operating temperature range: −40 to +85 °C

PACKAGE OUTLINES

PCF84C85P: 40-lead DIL; plastic (SOT-129)
PCF84C85T: 40-lead; mini-pack (VSO-40; SOT-158)

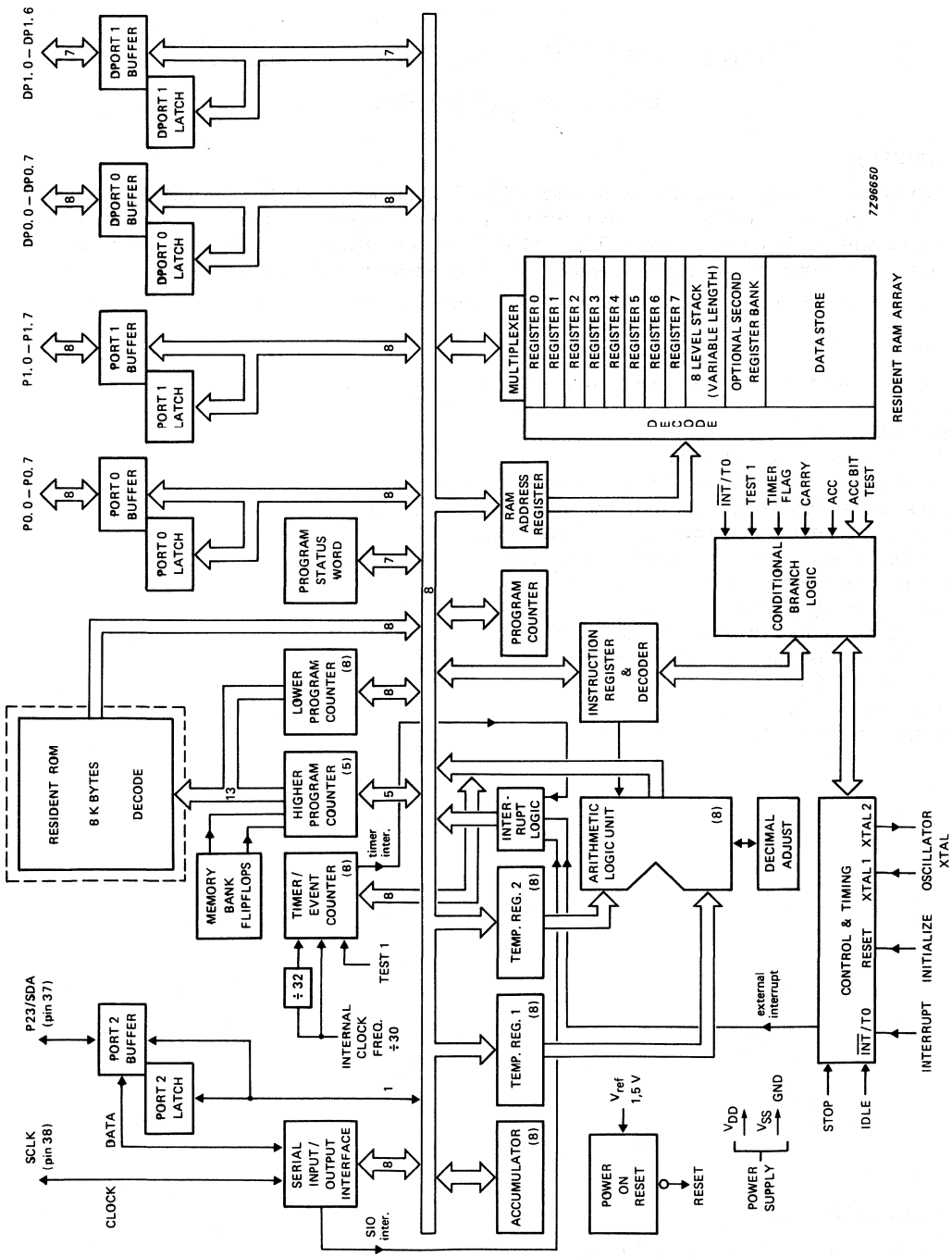


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

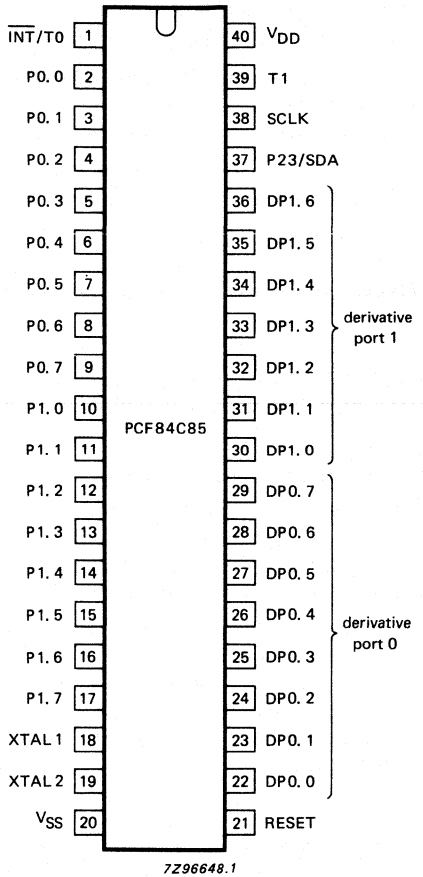


Fig. 2 Pinning diagram.

PIN DESIGNATION

38	SCLK	**Clock:** bidirectional clock for serial I/O.
1	$\overline{\text{INT}}$/T0	**Interrupt/Test 0:** external interrupt input (sensitive to negative-going edge)/test input pin; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
39	T1	**Test 1:** test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
18	XTAL 1	**Crystal input:** connection to timing component (crystal) which determines the frequency of the internal oscillator; also the input for an external clock source.
19	XTAL 2	Connection to the other side of the timing component.
21	RESET	**Reset input:** used to initialize the processor (active HIGH), or output of power-on-reset circuit.

PIN DESIGNATION (continued)

2-9	P0.0-P0.7	**Port 0:** 8-bit quasi-bidirectional I/O port.
10-17	P1.0-P1.7	**Port 1:** 8-bit quasi-bidirectional I/O port.
37	P23/SDA	**Port 2:** 1-bit quasi-bidirectional I/O port or serial data input/output in serial I/O mode.
22-29	DP0.0-DP0.7	**Derivative port 0:** 8-bit quasi-bidirectional I/O port.
30-36	DP1.0-DP1.6	**Derivative port 1:** 7-bit quasi-bidirectional I/O port.
20	V_{SS}	**Ground:** circuit earth potentional.
40	V_{DD}	**Power supply:** 2,5 V to 5,5 V.

FUNCTIONAL DESCRIPTION

Program memory

The program memory consists of 8 K bytes, in a read-only memory (ROM). Each location is directly addressable by the program counter. The memory is mask-programmed at the factory. Figure 3 shows the program memory map.

Four program memory locations are of special importance:

- Location 0; contains the first instruction to be executed after the processor is initialized (RESET),
- Location 3; contains the first byte of an external interrupt service subroutine;
- Location 5; contains the first byte of a serial I/O interrupt service subroutine.
- Location 7; contains the first byte of a timer/event counter interrupt service subroutine.

Program memory is arranged in banks of 2 K bytes, which are selected by SEL MB instructions. The program memory is further divided into location 'pages', each of 256 bytes. This latter division applies only for conditional branches. Memory bank boundaries can be crossed only by using unconditional branch instructions after the appropriate memory bank has been selected. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory

Data memory consists of 256 bytes, random-access data memory (RAM). All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 4 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

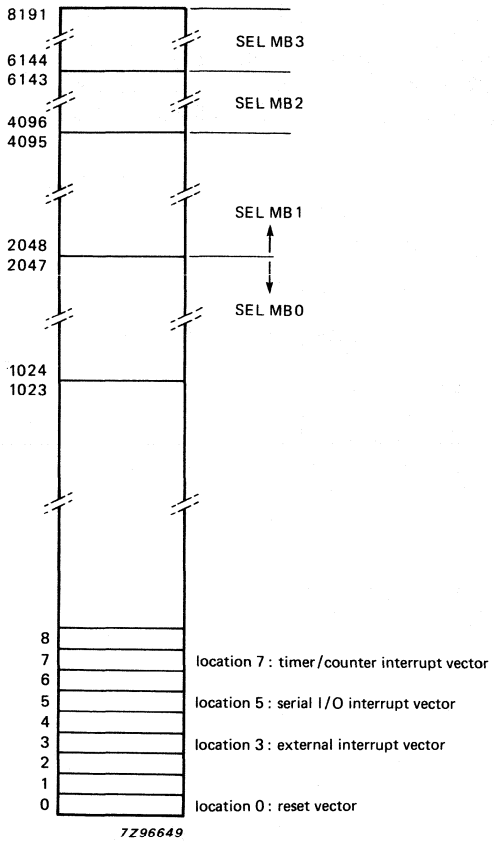


Fig. 3 Program memory map.

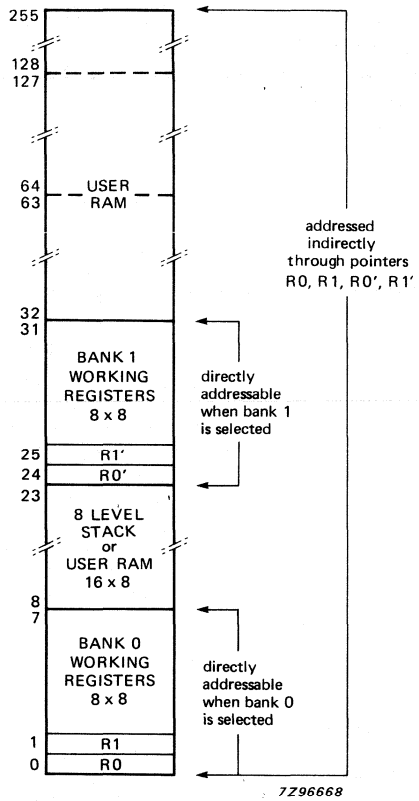


Fig. 4 Data memory map.

Program counter stack

Locations 8 to 23 may be designated as an 8-level program counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Fig.5) enables the processor to keep track of the return addresses and status generated by interrupts or CALL instructions by storing the contents of the program counter prior to servicing the subroutine. A 3-bit stack pointer determines which of the eight register pairs of the program counter stack will be loaded with the next generated return address.

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11 ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If not all 8 levels of subroutine and interrupt nesting are used, the unused portion of the stack may be used as any other indirectly addressable RAM locations.

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

FUNCTIONAL DESCRIPTION (continued)

The value of the saved contents of the program counter is different for an interrupt CALL compared to a normal CALL to subroutine. With an interrupt CALL, the program counter return address is saved; with a subroutine CALL, the saved program counter value is one less than the program counter return address.

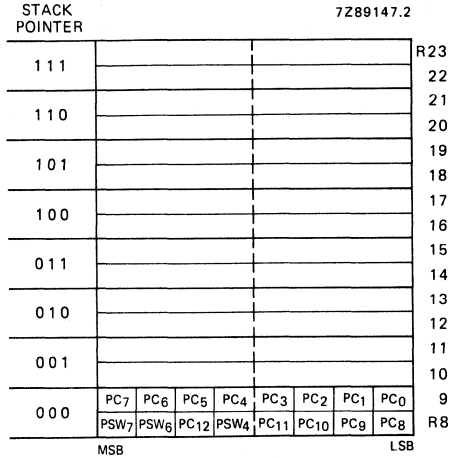


Fig. 5 Program counter stack.

IDLE and STOP modes

IDLE mode

When the microcontroller enters the IDLE mode via the IDLE instruction (01 H) the oscillator, timer/counter and serial I/O are kept running. The microcontroller exits from the IDLE mode by one of three interrupts if they are enabled or by activating a RESET. If the interrupt is not enabled the processor will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig. 6).

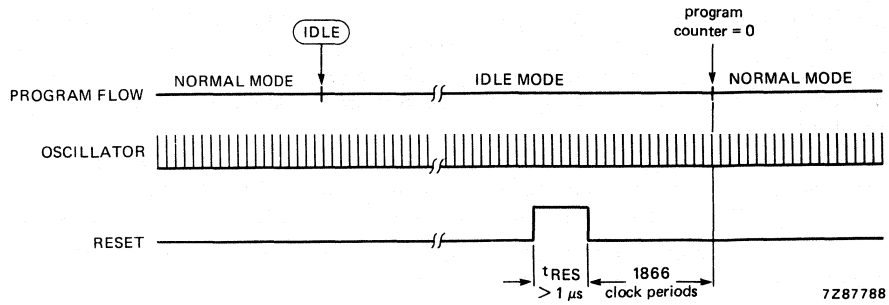


Fig. 6 Exit from IDLE mode via a RESET.

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A HIGH-to-LOW transition on the external interrupt pin ($\overline{INT}$/T0) reactivates the microcontroller. A LOW level applied to $\overline{INT}$/T0 will reactivate the microcontroller only in the STOP mode. Thus,if $\overline{INT}$/T0 was LOW before the microcontroller entered the IDLE mode, it must go HIGH before the microcontroller can be reactivated (see Fig. 7).

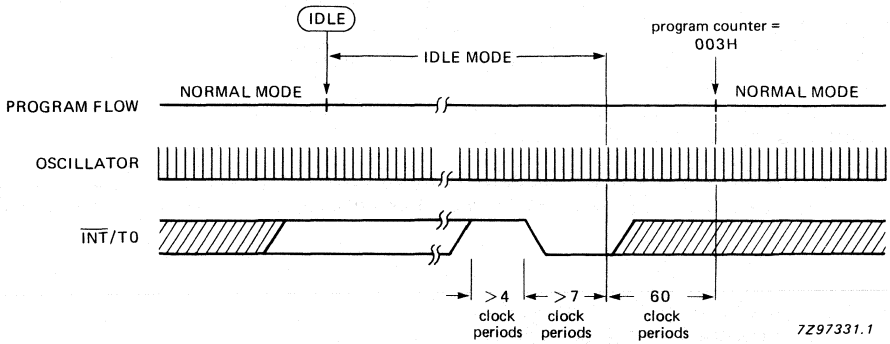


Fig. 7 Exit from IDLE mode via an interrupt.

Wake-up from the IDLE mode is ensured when $\overline{INT}$/T0 is HIGH for at least 4 CP (clock periods) followed by a LOW for 7 CP. After the initial forced CALL (*4H) operation (60 CP) the program continues with the external interrupt service routine.

* 1, 3, 5, 7, 9, B, D and F.

STOP mode

The microcontroller enters the STOP mode by the STOP instruction (22 H). The oscillator is switched off. The internal status of the CPU, RAM contents and the state of I/O ports are not affected. The microcontroller can be brought-out of the STOP mode by an active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied an internal delay of 1866 CP is provided to ensure that all internal clocks are operating correctly before restart (see Fig. 8). Note; the start-up time of a crystal oscillator is measured in milliseconds, and the 1866 CP count begins after this start-up time.

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence is executed.

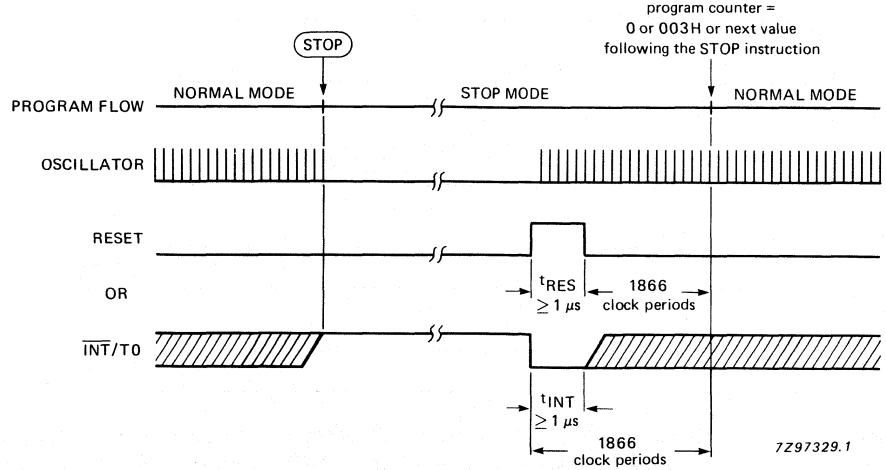


Fig. 8 Entering and exiting the STOP mode.

FUNCTIONAL DESCRIPTION (continued)

If the microcontroller exits the STOP mode by pulling the external interrupt input pin LOW, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence, executing the instruction following the STOP instruction.

The microcontroller is restarted by a LOW level applied at the $\overline{INT}$/T0 pin, and not by a HIGH-to-LOW transition as in a normal interrupt mechanism.
Note: when leaving the STOP mode with an interrupt, a further instruction in the main program series is executed prior to entering the interrupt routine.

When the $\overline{INT}$/T0 level is active during the STOP instruction then no STOP is executed.

A LOW level on the external interrupt input of at least 1 μs will cause the microcontroller to exit the STOP mode.

I/O facilities

The PCF84C85 family has 32 I/O lines arranged as:

- Port 0 parallel port of 8 lines (P0.0 to P0.7)
- Port 1 parallel port of 8 lines (P1.0 to P1.7)
- Port 2 parallel port of 1 line (P2.3)
- D port 0 parallel port of 8 lines (DP0.0-DP.7)
- D port 1 parallel port of 7 lines (DP1.0-DP1.6)

In addition to these the PCF84C43 also comprises four specialized I/O lines:

- SCLK I^2C-bus serial clock line
- SDA I^2C-bus serial data line (shared with P2.3)
- $\overline{INT}$/T0 external interrupt and test input. When used as a test input T0 can be directly tested by conditional branch instructions JT0 and JNT0
- T1 test input which can alter program sequences when tested by conditional jump instructions JT1 and JTN1. T1 also functions as an input to the 8-bit timer/event counter.

Parallel ports

All parallel ports can be used as outputs or inputs, their structure is quasi-bidirectional.
Output data written to a port is latched and remains unchanged until rewritten.
Input data is not latched and so must be present until read by an input instruction.
Input lines are fully CMOS compatible, output lines can drive one TTL or CMOS load.

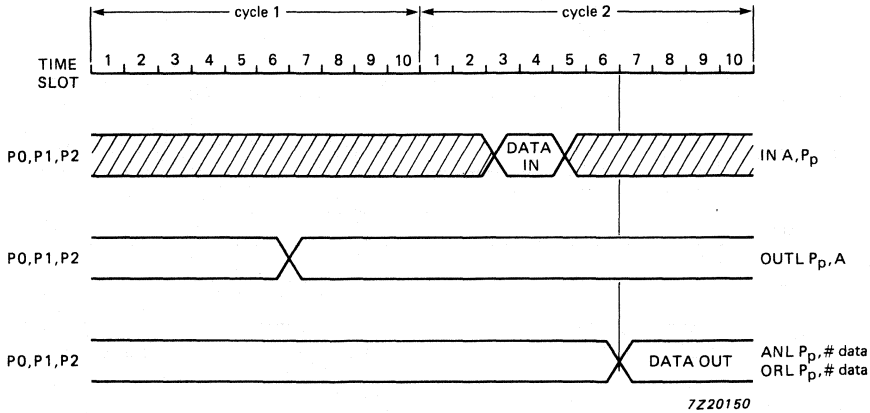


Fig. 9 Shows the timing diagram for all ports using IN, OUTL, ANL and ORL instructions. For the OUTL instruction data changes on time slot 7 of cycle 1. For the MOV, ANL and ORL instructions, the ports change on time slot 7 of cycle 2.

Fig. 10 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source. Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current source is sufficient for a TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output.

When a logic 1 is written to the line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period), to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to the port lines will not switch TR2 on. This prevents unnecessary current through external components connected to the port lines of the same port which might be in the input mode and also connected to ground.

When a logic 0 is written to the line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the line, otherwise TR1 will remain low impedance.

The PCF84C85 family offers the possibility to select individually 31 of the 32 parallel port pins (not P23), by the following mask options:

Option 1 – STANDARD PORT; quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and P-channel booster transistor TR2.
TR2 is only active during 1 clock cycle (Fig. 10).

Option 2 – OPEN DRAIN; quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig. 11).

Option 3 – PUSH-PULL OUTPUT; drive capability of the output will be 1,6 mA (min.) at V_{DD} = 5 V in both polarities. To avoid a large current flowing through the output transistors during the input mode, these push-pull pins must only be used as outputs (Fig. 12).

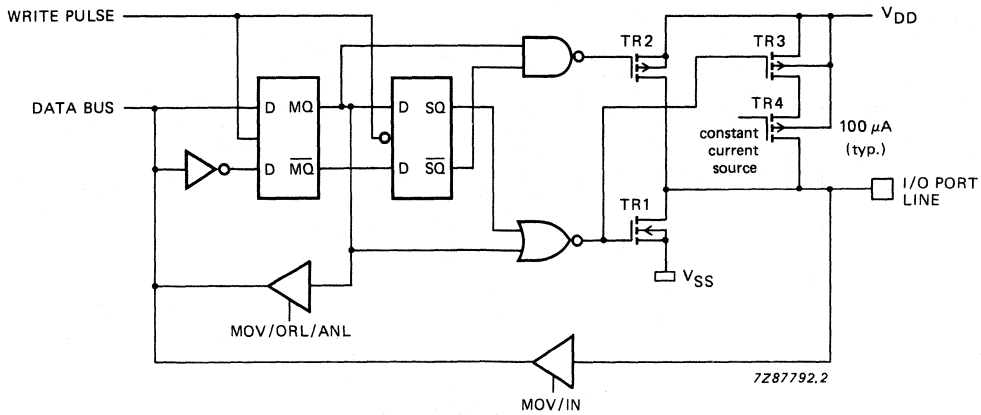


Fig. 10 Standard output with switched pull-up current source.

FUNCTIONAL DESCRIPTION (continued)

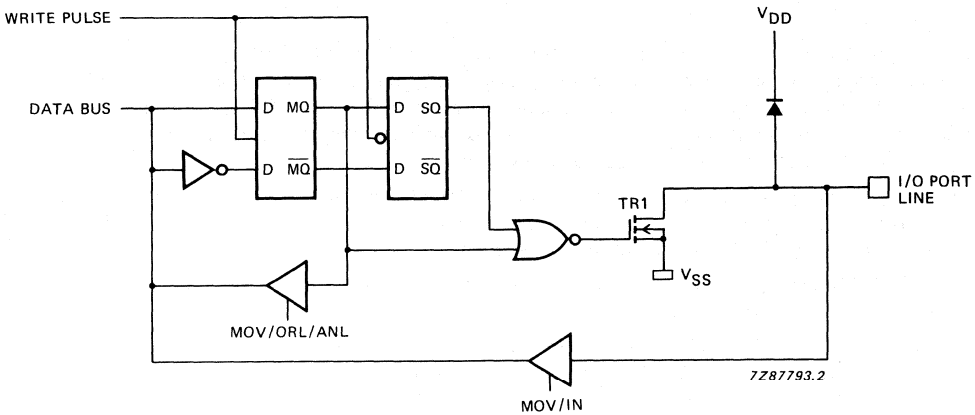


Fig. 11 Open drain output.

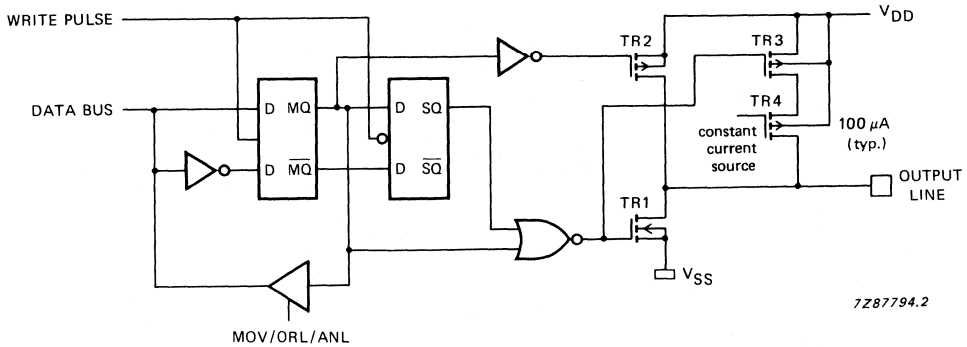


Fig. 12 Push-pull output.

Serial I/O (SIO)

The PCF84C85 has an on-chip serial I/O interface.

Whereas a normal microcontroller must regularly monitor the serial data bus for the presence of data, the serial I/O interface detects, receives and converts the serial data stream into parallel format without interrupting the execution of the current program. An interrupt is sent to the PCF84C85 only when a complete byte is received. It then reads the data byte in one instruction. Likewise during transmission the serial I/O interface performs parallel to serial conversion and subsequent serial output of the data. The microcontroller is only interrupted in the execution of its programmed tasks when a complete byte has been transmitted.

The design of the PCF84C85 serial I/O system allows any number of devices from PCF85XX family (clips) to be connected via the two-line serial bus. The ability of any devices to communicate, without interrupting the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to a message prefixed with its own address or the 'general CALL' address. Address recognition is performed by the interface hardware so that operation of the microcontroller need only be interrupted when a valid address has been received. This saves significant processing time and memory space compared with a conventional microcontroller employing a software serial interface. When the addressing facility is not required, for instance in a system with only two microcontrollers, direct data transfer without addressing can be performed. In multi-master systems, an automatically invoked arbitration procedure prevents two or more devices from continuing simultaneous transmission.

In NORMAL (running) and IDLE mode, the serial I/O logic remains active; its internal system clock will be switched off when there is no activity on the serial bus.

After execution of the STOP instruction, the oscillator of the PCF84C85 is switched off. This means that the serial I/O logic will remain in the state it was at the occurance of the STOP instruction. To avoid "bus block" problems and to assure correct start-up of the bus after exit from the STOP mode, the user should disable the serial logic (ESO = 0) prior to the execution of the STOP instruction. This must be carried out only when the PCF84C85 has finished a serial data transfer.

Serial I/O interface

Figure 13 shows the serial I/O interface. The clock line of the serial bus has exclusive use of pin 38 (SCLK) while the data line shares pin 37 (serial data) with the I/O line P23 of port 2. When the serial I/O is enabled, P23 is disabled as a parallel port line; (P23 and SCLK only open drain).

The microcontroller and interface communicate via the internal microcontroller bus and the Serial Interrupt Request line. Data and information controlling the operation of the interface are stored in four registers:

- Data shift register (S0)
- Serial I/O interface status word (S1)
- Serial clock control word (S2)
- Address register

FUNCTIONAL DESCRIPTION (continued)

Data shift register (S0)

Register S0 converts serial data to parallel format and vice versa. A pending interrupt is generated only after a complete byte has been transmitted, or after a complete data byte, specific address or 'general CALL' address has been received. The most significant bit is transmitted first.

Serial I/O interface status word (S1)

Register S1 provides information concerning the state of the interface and stores information from the microcontroller. Bits 0 to 3 are duplicated: control bits in these positions can only be written by the microcontroller, while interface bits can only be read.

MST and TRX (see Table 1)

These bits determine the operating mode of the serial I/O interface.

Table 1 Operating modes of the serial I/O interface

MST	TRX	operating mode
0	0	slave receiver
1	0	master receiver
0	1	slave transmitter
1	1	master transmitter

BB: Bus Busy.

This is the flag which indicates the status of the bus.

PIN: Pending Interrupt Not

PIN = '0' indicates the presence of a pending interrupt, which will cause a Serial Interrupt Request when the serial interrupt mechanism is enabled.

ESO: Enable Serial output

The ESO flag enables/disables the serial I/O interface: ESO = '1' enables, ESO = '0' disables. ESO can only be written by software.

BC0, BC1 and BC2

Bits BC0, BC1 and BC2 indicate the number of bits received or transmitted in a data stream. These bits can only be written by software.

AL: Arbitration Lost

The arbitration lost flag is set by hardware when the serial I/O interface, as master transmitter, loses a bus arbitration procedure.

AAS: Addressed As Slave

This flag is set by hardware when the interface detects either its own specific address or the 'general CALL' address as the first byte of a transfer and the interface has been programmed to operate in the address recognition mode.

AD0: Address Zero

This flag is set by hardware after detection of the 'general CALL' address when the interface is operating in the address recognition mode.

LRB: Last Received Bit

This contains either the last data bit received or, for a transmitting device in the acknowledgement mode, the acknowledgement signal from the receiving device.

Bits AL, AAS, AD0 and LRB can only be read by software.

Serial clock control word (S2)

Bits 0 to 4 of the clock control register S2 are used to set the frequency of the serial clock signal. When a 6 MHz crystal is used, the frequency of the serial clock can be varied between 154 kHz and 1 kHz (see Table 2). An asymmetrical clock with a HIGH-to-LOW ratio of 3 : 1 can be generated using bit 5. The asymmetrical clock allows a microcontroller more time per clock period for sampling the data line, making the timing of this action less critical. Bit 6 can be used to activate the acknowledge mode of the serial I/O. S2 is a write only register.

Address register

The address register contains the 7-bit address back-up latches and the bit (ALS) used to enable/disable the address recognition mode. The address register can be written using the MOV S0, A and MOV S0, # data instructions, but only when ES0 = '0'.

Serial I/O interrupt logic

An EN SI instruction enables and a DIS SI instruction disables the interrupt logic. When the logic is enabled, a pending interrupt results in a serial I/O interrupt to the processor, causing a CALL to location 5 in the ROM. When disabled, the presence of an interrupt is still indicated by PIN in S1, allowing the interrupt to be serviced. However, vectored interrupt will not occur.

FUNCTIONAL DESCRIPTION (continued)

Table 2 SIO clock pulse frequency control when using 6 MHz crystal

hexadecimal S20-S24 code	divisor	f_{XTAL}(6 MHz) f_{SCLK} (kHz)	f_{XTAL} (10 MHz) f_{SCLK} (kHz)
0	not allowed		
1	39	*154	*256
2	45	*133	*222
3	51	*118	*196
4	63	95	*159
5	75	80	*133
6	87	69	*115
7	99	61	*101
8	123	49	81
9	147	41	68
A	171	35	58
B	195	31	51
C	243	25	41
D	291	21	34
E	339	18	29
F	387	16	26
10	483	12	21
11	579	10	17
12	675	8,9	15
13	771	7,8	13,4
14	963	6,2	10,4
15	1155	5,2	8,7
16	1347	4,5	7,4
17	1539	3,9	6,5
18	1923	3,1	5,2
19	2307	2,6	4,3
1A	2691	2,2	3,7
1B	3075	2,0	3,3
1C	3843	1,6	2,6
1D	4611	1,3	2,2
1E	5379	1,1	1,9
1F	6147	1,0	1,6

* Not permitted for I^2C operation; the maximum clock frequency in the I^2C systems is 100 kHz.

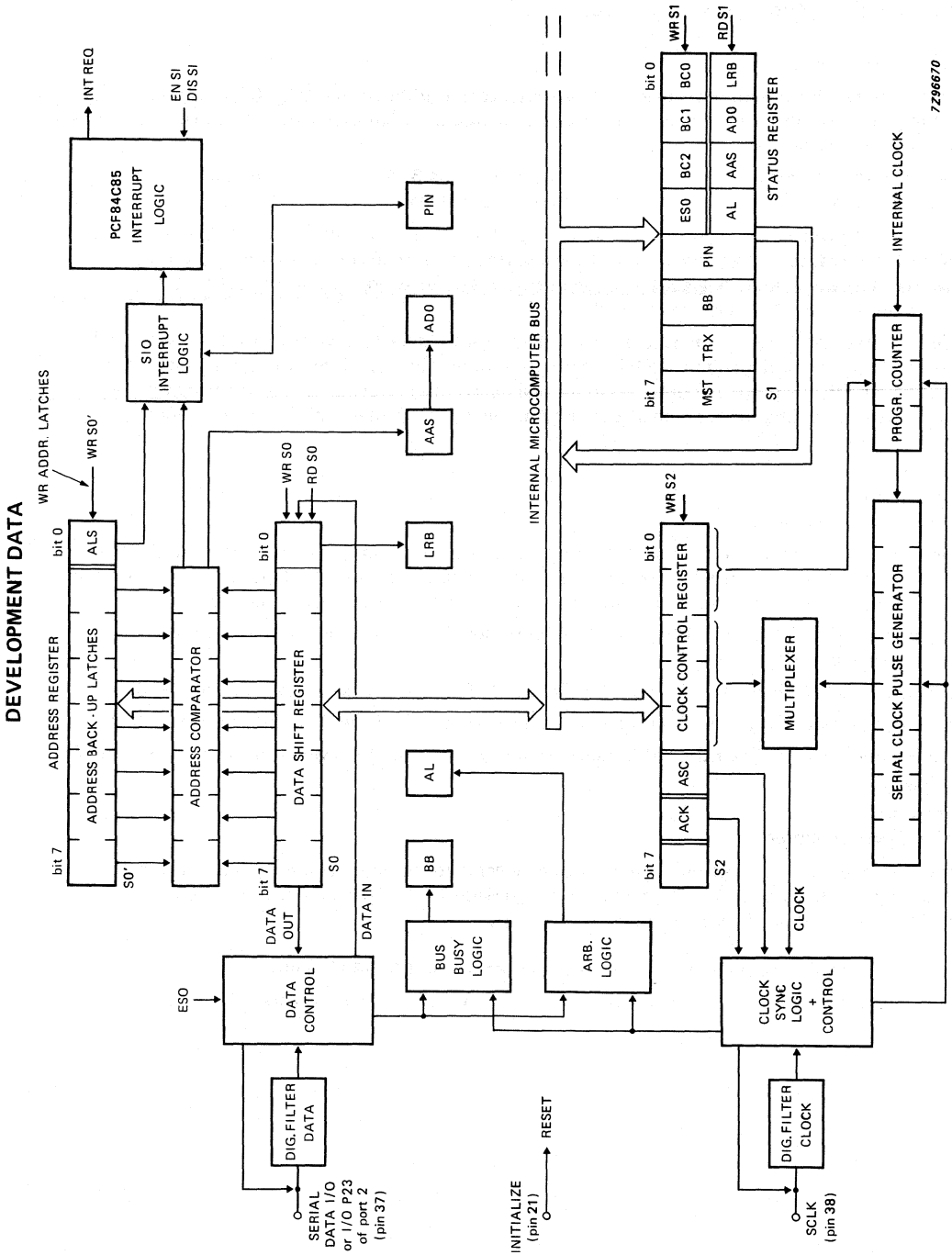


Fig. 13 Serial I/O interface.

FUNCTIONAL DESCRIPTION (continued)

Interrupts (see Fig. 14)

When the external interrupt is enabled, a HIGH-to-LOW transition on the $\overline{INT}$/T0 input initiates an external interrupt subroutine which causes a CALL to program memory location 3 following completion of the current instruction.

Serial I/O interrupt, when enabled, causes a CALL to location 5, and a timer/event counter overflow forces a CALL to location 7 when the timer interrupt is enabled.

When an interrupt subroutine starts, the contents of the program counter and bits 4, 6 and 7 of the PSW have been saved in the program counter stack. Accumulator contents have to be saved by software. Interrupt acknowledgement can be carried out by software via port pins. All interrupt subroutines must reside in memory bank 0.

Since the interrupt system is single level, once an interrupt is detected, all further interrupt requests are latched, but ignored, pending a RETR instruction to re-enable the interrupt input logic. After executing RETR, the program continues in the main part; this is independent of the occurance of a second interrupt during the running of the first routine. If 2 or 3 interrupts occur simultaneously, their priority is:

- (1) external
- (2) serial I/O
- (3) timer/event counter

An external interrupt can be generated by using the timer/counter in the event counter mode. The counter is first preset to (FFH), then EN TCNTI instruction is executed. A LOW-to-HIGH transition of the T1 input will then initiate an interrupt subroutine and cause a CALL to location 7.

On execution of a DIS I instruction, the PCF84C85 always clears the digital filter/latch and the External Interrupt Flag.

The Timer Flag (TF) is reset only when the JTF or JNTF instruction is executed or after RESET.

The Timer Interrupt Flag is set when timer overflow occurs, only if the timer interrupt is enabled.

The microcontroller will exit the IDLE mode when any one of the following three interrupts is enabled:

- External
- Serial I/O
- Timer/event counter

There is no internal pull-up or pull-down device connected to the external interrupt input (pin 1). If required pin 1 must be externally connected to a resistor ($R \leqslant 100\ k\Omega$). When the external interrupt is not used pin 1 must be connected to V_{DD}.

Improvements to interrupt and timer logic with respect to the MAB8400 family

For detailed information see the user manual "Single-chip 8-bit Microcontrollers".

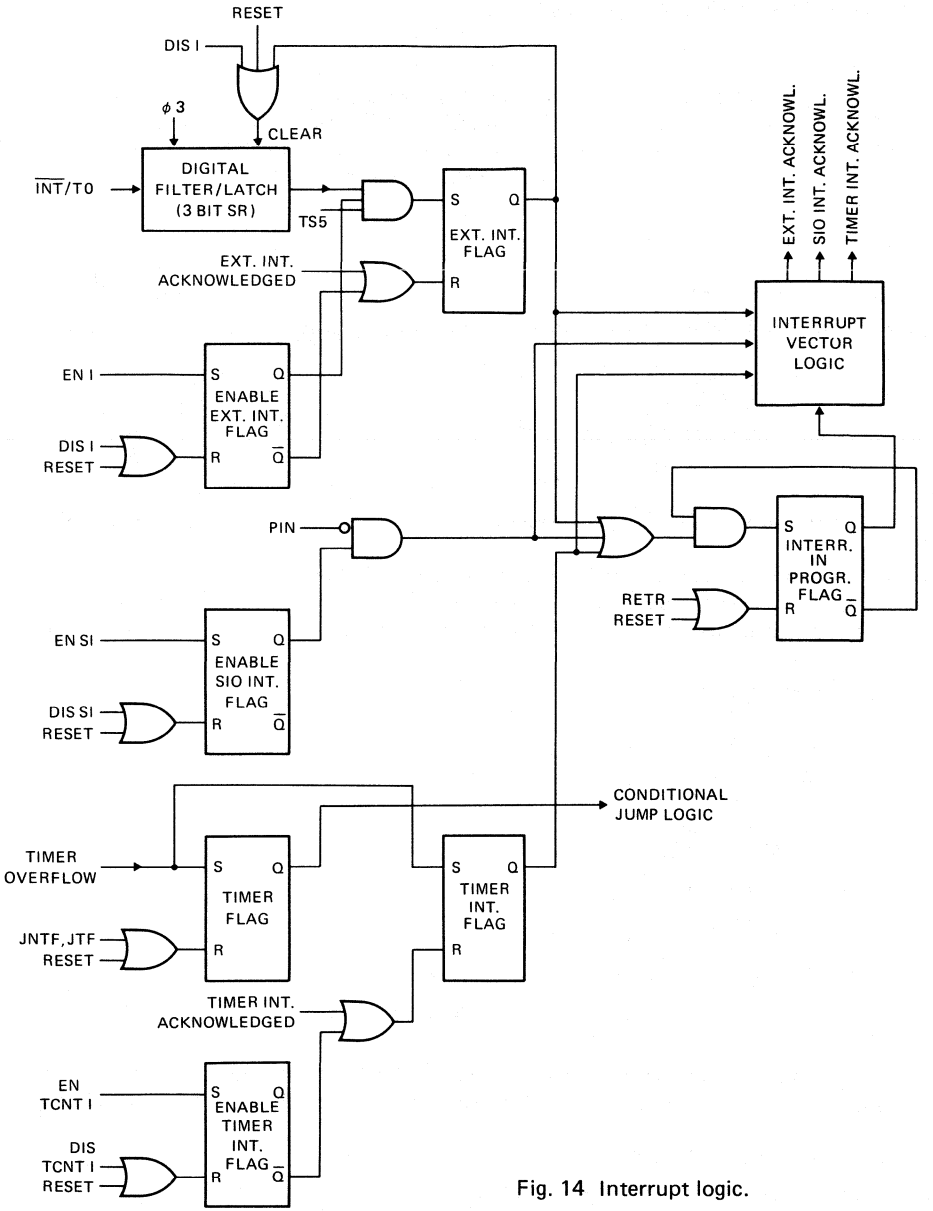


Fig. 14 Interrupt logic.

Notes to figure 14

1. $\overline{INT}$/T0 negative edge is always latched in the digital filter/latch.
2. Correct interrupt timing is ensured when INT/T0 is HIGH for $>$ 4 CP followed by a LOW for $>$ 7 CP.
3. When the interrupt in progress flag is set, further interrupts are latched but ignored, until RETR is executed.
4. A DIS I instruction always clears a pending external interrupt.
5. For all flip-flops, RESET overrules SET.

FUNCTIONAL DESCRIPTION (continued)

Oscillator (see Fig. 15)

The oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-supply voltage condition is present to prevent discharge of a weak back-up battery. Provided the supply voltage is within the operating range the oscillator will be restarted after a STOP instruction by a LOW level at the $\overline{INT}$/T0 pin or a HIGH level at the RESET pin.

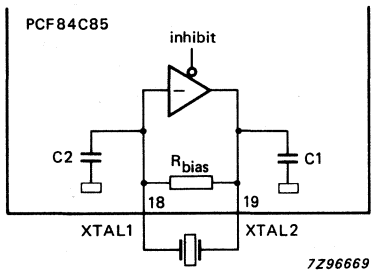


Fig. 15 Oscillator with integrated elements.

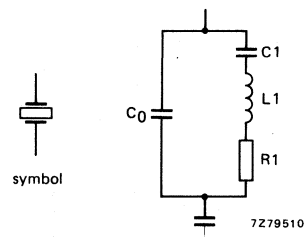


Fig. 16 Crystal unit equivalent circuit.

The values of crystal series resistance R1 and the crystal's total load capacitance C_L (C_0 + wiring + external capacitors) must not be above the curve (Fig. 17) for the corresponding frequency.
Note; if external capacitors are connected to XTAL 1 and XTAL2 they must be of equal value.

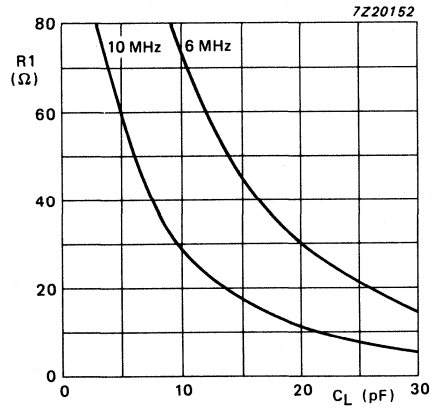


Fig. 17 Crystal circuit criteria.

The oscillator has the output drive capability via pin 19 (XTAL2). An external clock can be applied to pin 18 (XTAL1). A machine cycle consists of 10 time slots, each time slot being 3 oscillator periods.

Timer/event counter (see Fig. 18)

An internal 8-bit up-counter is provided. This can count external events, modulo-32 machine cycles, or machine cycles directly. Table 3 gives the instructions that control the counter and the prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW-to-HIGH transitions on pin 39 (T1) are counted. The maximum rate at which the counter may be incremented is once every machine cycle. When the counter overflows, the timer flag is set. The flag can be tested and reset using the JTF (jump is timer flag = 1) or JNTF instruction. Overflow also generates an interrupt to the processor via setting of the Timer Interrupt Flag when the timer/event counter interrupt is enabled.

Table 3 Timer/event counter control

function	timer mode modulo-1, modulo-32*	counter mode
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ**	MOV A,T	MOV A,T

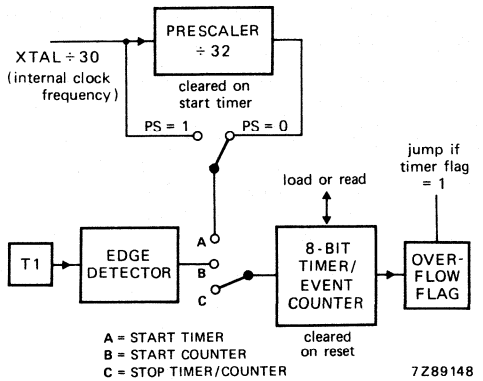


Fig. 18 Timer/event counter.

Program status word (see Fig. 19)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.
The PSW bits are:

- Bits 0 to 2 — stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 — prescaler select (PS);
  0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 — working register bank select (RBS);
  0 = register bank 0; 1 = register bank 1
- Bit 5 — not used (1)
- Bit 6 — auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 — carry (CY); the carry flag indicates that previous operation has resulted in an overflow of the accumulator.

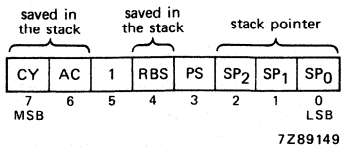


Fig. 19 Program status word.

* With prescaler select, PS = 0, the timer counts modulo-32 machine cycles, with PS = 1 it counts modulo-1 cycles (prescaler not used); prescaler cleared with STRT T, prescaler not readable.

** READ does not disturb the counting process.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Program status word (continued)

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by a SEL RB instruction, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions in the event of an interrupt. Bits 7, 6 and 4 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt and can be used at the end of a normal subroutine. The RET instruction has no restore feature and cannot be used at the end of an interrupt.

Program counter (see Fig. 20)

The 13-bit program counter is able to address 8 K bytes of ROM. The arrangement of the bits is shown in figure 20. During an interrupt subroutine PC_{11} and PC_{12} are forced to logic 0. All 13 bits are saved in the stack during CALL and interrupt routines.

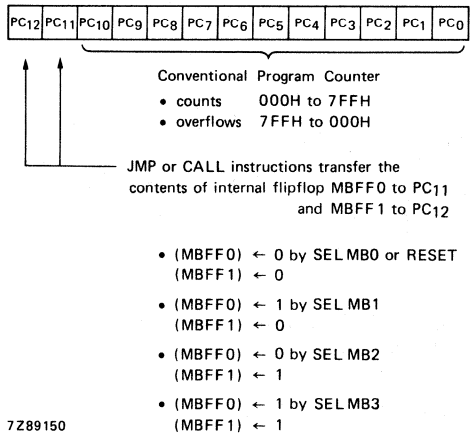


Fig. 20 Program counter.

Central processing unit

The PCF84C85 has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the current ROM page.

Conditional branch logic

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program. Table 4 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Table 4 Conditional branches

test	jump condition	jump instruction
accumulator	all bits zero	JZ
	any bit non-zero	JNZ
accumulator bit test	1	JB0 to JB7
carry flag	1	JC
	0	JNC
timer overflow flag	1	JTF
	0	JNTF
test input T0	1	JT0
	0	JNT0
test input T1	1	JT1
	0	JNT1
register	non-zero	DJNZ

Test input T1 (pin 39)

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for > 4 CP, followed by a HIGH for > 4 CP. The transition can be recognized with a repetition rate of once per 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. If required it must be externally connected to a resistor ($R = \leqslant 100\ k\Omega$). When T1 is not used pin 39 must be connected to V_{DD} or V_{SS}.

Reset (pin 21)

A positive-going signal on the RESET input

- Sets the program counter to zero
- Selects location 0 of memory bank 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external, timer and serial I/O)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to modulo-32
- Resets the timer flag
- Sets all ports to input mode
- Sets the serial I/O to slave receiver mode and disables the serial I/O
- Cancels IDLE and STOP mode

FUNCTIONAL DESCRIPTION (continued)

Power-on-reset

The internal power-on reset circuit monitors the PCF84C85 supply voltage V_{DD}. For as long as the supply voltage remains below the internal reference level V_{ref} (typically 1,5 V) the oscillator is inhibited and RESET (pin 21) has an undefined level. When V_{DD} rises above the internal reference level, the oscillator is released and RESET is pulled high to V_{DD} by TR1 for a period t_D (typically 50 μs).

N.B. Because of the narrow bandwidth of the crystal, the start-up time of the oscillator is typically 10 ms.

Three modes of power-on reset are possible:

1. If V_{DD} can be switched on with fast rise time i.e. V_{DD} reaches its minimum operating value (corresponding to the selected oscillator frequency) before the RESET signal (t_D) has finished, then no extra components are required (see Fig. 21 and 22). Note that the first instruction is executed after the oscillator start-up time plus 1866 clock periods have elapsed.

2. If V_{DD} has a slow rise time then the RESET signal should be stretched by an external RC circuit (see Fig. 23 and 24). In the event of a short drop in the supply voltage, the diode path rapidly discharges the capacitor to ensure a reliable power-on reset. To ensure a correct reset, the RESET signal should reach at least 70% of the final value of V_{DD}. Given that the RESET voltage and V_{DD} rise exponentially, the above requirement is satisfied when the time constant τ of the RESET pulse is >8 times the time constant of V_{DD}. If V_{DD} rises linearly, then a RESET time constant >2 times the rise time of V_{DD} is required.

   When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods have elapsed (see Fig. 24). If the oscillator is started-up prior to the completion of RESET, then program execution begins 1866 clock periods after RESET goes LOW.

3. Figure 25 shows an external reset to the PCF84C85 during power-on. The external reset signal must remain HIGH until V_{DD} has reached its minimum operating value corresponding to the selected oscillator frequency. When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods have elapsed (see Fig. 26). If the oscillator is started-up prior to the completion of RESET, then program execution begins 1866 clock periods after RESET goes LOW.

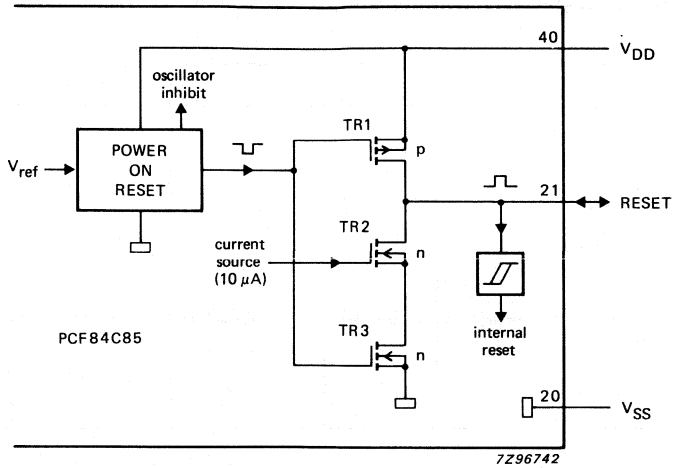


Fig. 21 Power-on-reset configuration.

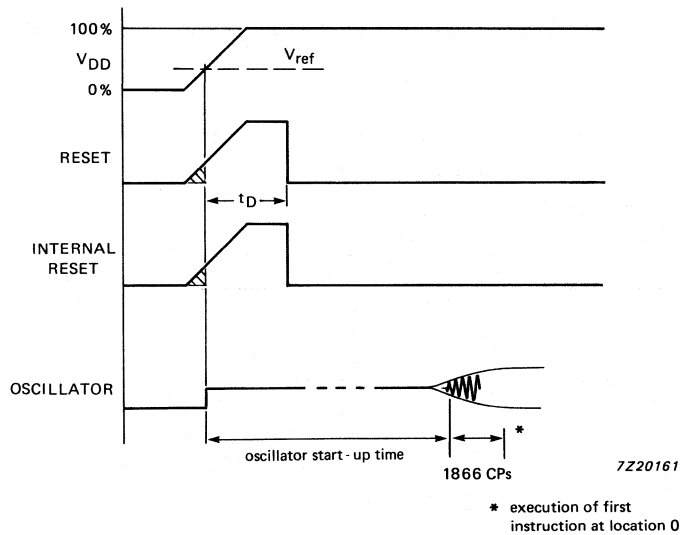


Fig. 22 Timing of power-on-reset with fast rise time.

FUNCTIONAL DESCRIPTION (continued)

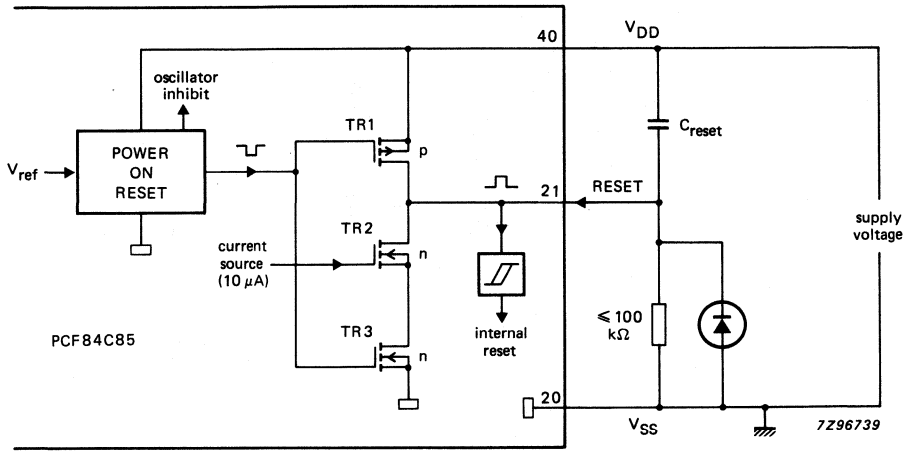


Fig. 23 Stretched power-on-reset with external components.

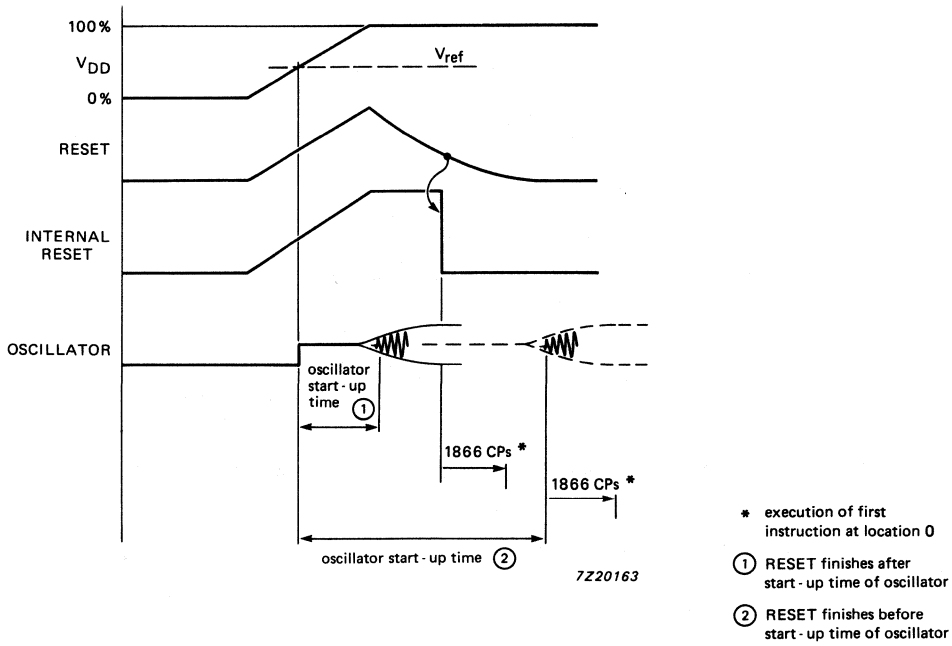


Fig. 24 Timing of power-on-reset with a slowly rising V_{DD} and a stretched RESET pulse.

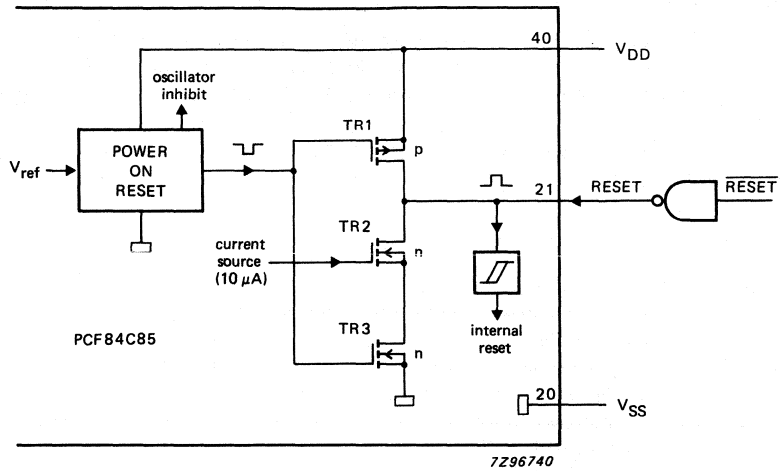


Fig. 25 External power-on-reset configuration.

DEVELOPMENT DATA

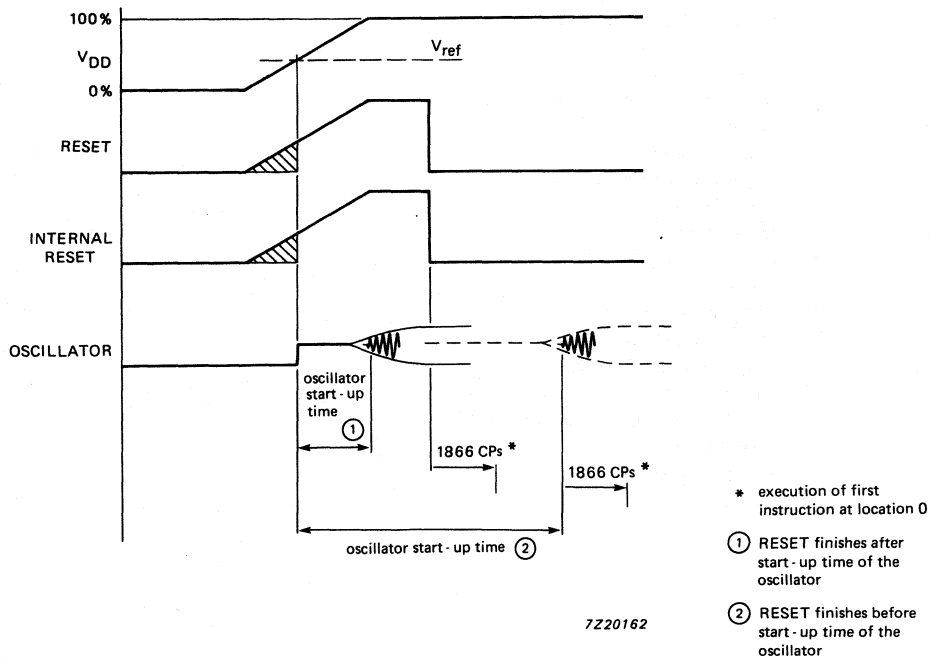


Fig. 26 Timing of external power-on-reset.

INSTRUCTION SET

The PCF84C85 instruction set consists of over 80 one and two byte instructions and is identical to the MAB8400 instruction set. New instructions are added for STOP and IDLE mode. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 7 gives the instruction set of the PCF84C85. Table 6 shows the instruction map and Table 5 details the symbols and definition descriptions that are used.

Table 5 Symbols and definitions used in Table 7

symbol	definition description
A	accumulator
addr	program memory address
Bb	bit designation (b = 0-7)
RBS	register bank select
C	carry bit (bit CY)
CNT	event counter
Dx	Derivative register designation (x = 0,1,2 or 3)
data	8-bit number or expression
I	interrupt
MB	memory bank
MBFF	memory bank flip-flop
P	mnemonic for 'in-page' operation
PC	program counter
Pp	port designation (p = 0, 1 or 2)
PSW	program status word
RB	register bank
Rr	register designation (r = 0-7)
Sn	serial I/O register
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with

Table 6 PCF84C85 instruction map

first hexadecimal character of opcode ↓ / second hexadecimal character of opcode →	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A,#data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp				MOV A,Sn			
									0	1	2		0	1		
1	INC @Rr		JB0	ADDC A,#data	CALL page 0	DIS I	JTF addr	INC A	INC Rr							
	0	1	addr						0	1	2	3	4	5	6	7
2	XCH A,@Rr		STOP	MOV A,#data	JMP page 1	EN TCNTI	JNTO addr	CLR A	XCH A,Rr							
	0	1							0	1	2	3	4	5	6	7
3	XCHD A,@Rr		JB1		CALL page 1	DIS TCNTI	JTO addr	CPL A	OUTL Pp,A				MOV Sn,A			
	0	1	addr						0	1	2		0	1	2	
4	ORL A,@Rr		MOV A,T	ORL A,#data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr							
	0	1							0	1	2	3	4	5	6	7
5	ANL A,@Rr		JB2	ANL A,#data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr							
	0	1	addr						0	1	2	3	4	5	6	7
6	ADD A,@Rr		MOV T,A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr							
	0	1							0	1	2	3	4	5	6	7
7	ADDC A,@Rr		JB3		CALL page 3			RR A	ADDC A,Rr							
	0	1	addr						0	1	2	3	4	5	6	7
8				RET	JMP page 4	EN SI			ORL Pp,#data				MOV A,Dx	MOV Dx,A	ANL Dx,A	ORL Dx,A
									0	1	2					
9			JB4	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,#data				MOV Sn,#data			
			addr						0	1	2		0	1	2	
A	MOV @Rr,A			MOVP A,@A	JMP page 5	SEL MB2		CPL C	MOV Rr,A							
	0	1							0	1	2	3	4	5	6	7
B	MOV @Rr,#data		JB5	JMPP @A	CALL page 5	SEL MB3			MOV Rr,#data							
	0	1	addr						0	1	2	3	4	5	6	7
C	DEC @Rr				JMP page 6	SEL RB0	JZ addr	MOV A,PSW	DEC Rr							
	0	1							0	1	2	3	4	5	6	7
D	XRL A,@Rr		JB6	XRL A,#data	CALL page 6	SEL RB1		MOV PSW,A	XRL A,Rr							
	0	1	addr						0	1	2	3	4	5	6	7
E	DJNZ @Rr,addr				JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr							
	0	1							0	1	2	3	4	5	6	7
F	MOV A,@Rr		JB7		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr							
	0	1	addr						0	1	2	3	4	5	6	7

INSTRUCTION SET (continued)

Table 7 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) −1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

DEVELOPMENT DATA

ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1}) \leftarrow A_n$ $(A_0) \leftarrow (C), (C) \leftarrow (A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (C), (C) \leftarrow (A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7}) \leftrightarrow (A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data		
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3}) \leftrightarrow ((R0_{0-3}))$ $(A_{0-3}) \leftrightarrow ((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3) \leftarrow (A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7}) \leftarrow (A), (A) \leftarrow ((PC))$		
FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2

INSTRUCTION SET (continued)

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1	r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1		
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1	r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1		
BRANCH	JMP addr	• 4 address	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1		
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))		
	DJNZ Rr, addr	E* address	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 if (Rr) not zero (PC_{0-7})←addr	r = 0–7	
	DJNZ @Rr, addr	E0 address	2/2	decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr		
		E1 address			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr		
	JBb addr	▲ 2 address	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr	b = 0–7	
	JC addr	F6 address	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr		
	JNC addr	E6 address	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr		
	JZ addr	C6 address	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr		
	JNZ addr	96 address	2/2	jump to addr if A is NOT zero	if A≠0 : (PC_{0-7})←addr		
	JT0 addr	36 address	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr		
	JNT0 addr	26 address	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr		
	JT1 addr	56 address	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr		
	JNT1 addr	46 address	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr		
	JTF addr	16 address	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr		4
	JNTF addr	06 address	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr		

TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	
	SEL MB2	A5	1/1	select program memory bank 2	(MBFF0)←0, (MBFF1)←1	
	SEL MB3	B5	1/1	select program memory bank 3	(MBFF0)←1, (MBFF1)←1	
	STOP	22	1/1	enter STOP mode		
	IDLE	01	1/1	enter IDLE mode		
SUBROUTINE	CALL addr	▲ 4 address	2/2	jump to subroutine	$((SP))\leftarrow(PC), (PSW_{4,6,7})$ 6 $(SP)\leftarrow(SP)+1$ $(PC_{8-10})\leftarrow addr_{8-10}$ $(PC_{0-7})\leftarrow addr_{0-7}$ $(PC_{11-12})\leftarrow$MBFF 0–1	6
	RET	83	1/2	return from subroutine	$(SP)\leftarrow(SP)-1$ $(PC)\leftarrow((SP))$	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	$(SP)\leftarrow(SP)-1$ $(PSW_{4,6,7})+(PC)\leftarrow((SP))$	6

INSTRUCTION SET (continued)

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	 7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 data 99 data 9A data	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 data 89 data 8A data	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
DERIVATIVE INPUT/OUTPUT	MOV A, Dx	8C 00 8C 01	2/2 2/2	input pin data of port DP0, DP1 to accumulator	(A)←(D0) (A)←(D1)	 8
	MOV Dx, A	8D 02 8D 03	2/2 2/2	move contents of accumulator to latch of port DP0, DP1	(D2)←(A) (D3)←(A)	
	ANL Dx, A	8E 02 8E 03	2/2 2/2	AND contents of DP0, DP1 latch with accumulator	(D2)←(D2) AND (A) (D3)←(D3) AND (A)	
	ORL Dx, A	8F 02 8F 03	2/2 2/2	OR contents of DP0, DP1 latch with accumulator	(D2)←(D2) OR (A) (D3)←(D3) OR (A)	
	MOV A, Dx	8C 02 8C 03	2/2 2/2	move contents of DP0, DP1 latch to accumulator	(A)←(D2) (A)←(D3)	 8

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
SERIAL INPUT/OUTPUT	MOV A, S_n	0C 0D	1/2	move serial I/O register contents to accumulator	(A)←(S0) (A)←(S1)	9
	MOV S_n, A	3C 3D 3E	1/2	move accumulator contents to serial I/O register	(S0)←(A) (S1)←(A) (S2)←(A)	
	MOV S_n, #data	9C data 9D data 9E data	2/2	move immediate data to serial I/O register	(S0)←data (S1)←data (S2)←data	
	EN SI	85	1/1	enable serial I/O interrupt		
	DIS SI	95	1/1	disable serial I/O interrupt		
	NOP	00	1/1	no operation		

Notes to Table 8

1. PSW CY, AC affected
2. PSW CY affected
3. PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF).
5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 0000 (P23) 111
8. The MSB of A becomes a logic 0
9. (S1) has a different function in read and write operations, see serial I/O interface.

* : 8,9,A,B,C,D,E,F
● : 0,2,4,6,8,A,C,E
▲ : 0,3,5,7,9,B,D,F

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 40)	V_{DD}		−0,8 to +8	V
All input voltages	V_I		−0,8 to V_{DD} +0,8	V
D.C. current into any input or output	$\pm I_I$, $\pm I_O$	max.	10	mA
Total power dissipation				
Power dissipation per output				
except P23, SCLK	P_O	max.	50	mW
P23, SCLK	P_O	max.	180	mW
Storage temperature range	T_{stg}		−65 to +150	°C
Operating ambient temperature range	T_{amb}		−40 to +85	°C
Operating junction temperature	T_j	max.	125	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DEVELOPMENT DATA

D.C. CHARACTERISTICS

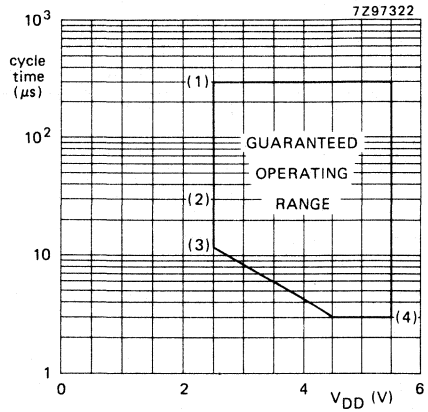
V_{DD} = 2,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; all voltages with respect to V_{SS}; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating (see Fig. 27)	V_{DD}	2,5	–	5,5	V
Supply current					
operating (see Fig. 28)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	1,6	3,2	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	1	2	mA
at V_{DD} = 3 V; f_{XTAL} = 3,58 MHz	I_{DD}	–	0,5	0,6	mA
IDLE mode (see Fig. 29)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	0,8	1,6	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	1	1	mA
at V_{DD} = 3 V; f_{XTAL} = 3,58 MHz	I_{DD}	–	0,25	0,4	mA
STOP mode (see Fig. 35 and note 1)					
at V_{DD} = 2,5 V; T_{amb} = 25 °C	I_{DD}	–	1,2	2,5	μA
at V_{DD} = 2,5 V; T_{amb} = 70 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current					
as $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output voltage LOW					
at V_I = V_{SS} or V_{DD}; $\|I_O\| < 1$ μA	V_{OL}	–	–	0,05	V
Output sink current LOW					
at V_{DD} = 5 V ± 10%; V_O = 0,4 V					
except P23/SDA, SCLK (see Fig. 31)	I_{OL}	1,6	3	–	mA
P23/SDA, SCLK (see Fig. 32)	I_{OL}	3	–	–	mA
Pull-up output source current HIGH (see Fig. 33)					
at V_{DD} = 5 V ± 10%; V_O = $0{,}7V_{DD}$	$-I_{OH}$	40	–	–	μA
at V_{DD} = 5 V ± 10%; V_O = V_{SS}	$-I_{OH}$	–	–	400	μA
Push-pull output source current HIGH					
at V_{DD} = 5 V ± 10%; V_O = V_{DD}−0,4 V	$-I_{OH}$	1,6	3	–	mA

Note 1

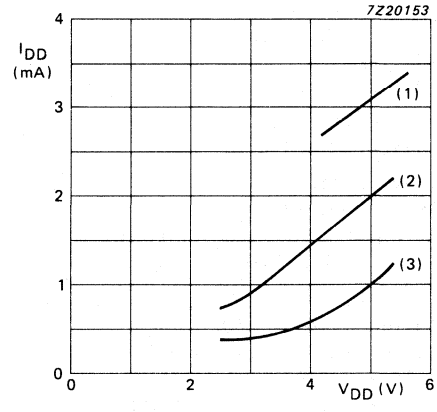
Crystal connected between XTAL1 and XTAL2; SCL and SDA pulled to V_{DD} via 5,6 kΩ resistor; T1 at V_{SS}, $\overline{INT}$ at V_{DD}.

A.C. CHARACTERISTICS (continued)



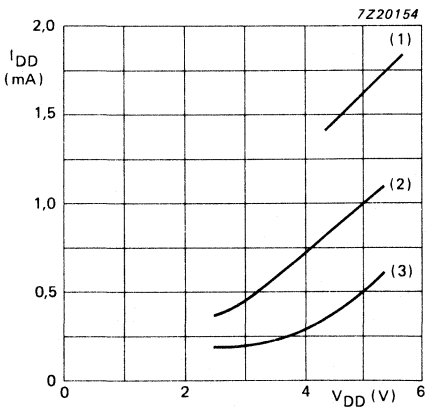
(1) clock frequency = 100 kHz
(2) clock frequency = 1 MHz
(3) clock frequency = 3 MHz
(4) clock frequency = 10 MHz

Fig. 27 Maximum clock frequency (f_{XTAL}) as a function of the supply voltage (V_{DD}).



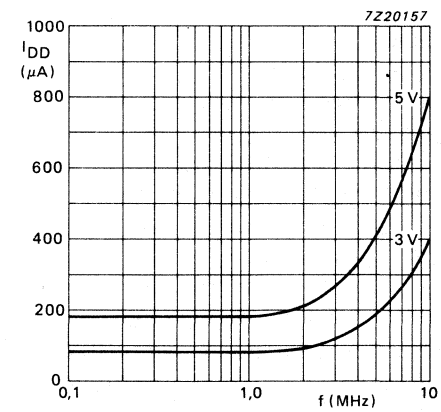
(1) clock frequency = 10 MHz
(2) clock frequency = 6 MHz
(3) clock frequency = 3,58 MHz

Fig. 28 Maximum supply current (I_{DD}) in operating mode as a function of the supply voltage.



(1) clock frequency = 10 MHz
(2) clock frequency = 6 MHz
(3) clock frequency = 3,58 MHz

Fig. 29 Maximum supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}).



(1) V_{DD} = 3 V
(2) V_{DD} = 5 V

Fig. 30 Typical supply current during IDLE mode as a function of frequency.

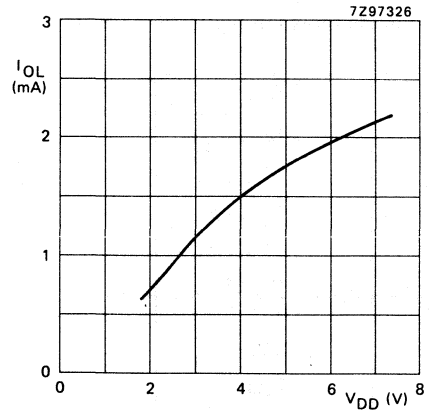


Fig. 31 Output sink current LOW (I_{OL}), except outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); V_O = 0,4 V.

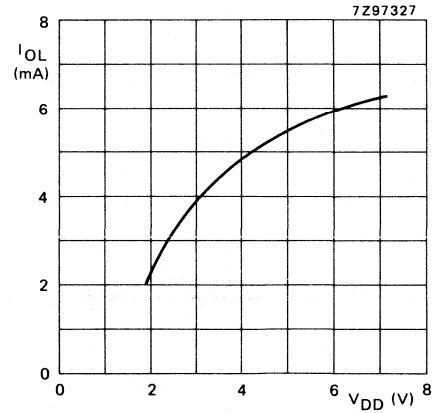
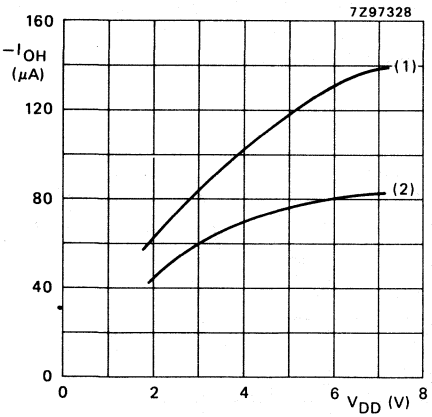


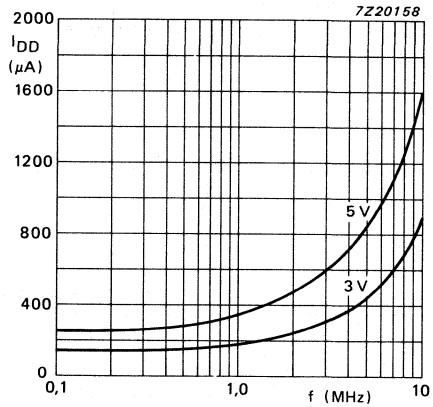
Fig. 32 Output current LOW (I_{OL}), outputs P23/SDA and SCLK, as a function of supply voltage (V_{DD}); V_O = 0,4 V.

DEVELOPMENT DATA



(1) $V_O = V_{SS}$
(2) $V_O = 0{,}7\ V_{DD}$

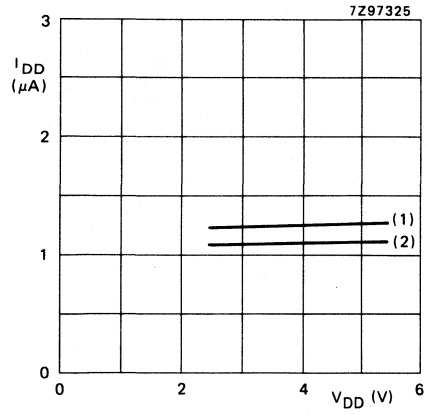
Fig. 33 Output source current HIGH ($-I_{OH}$) as a function of supply voltage (V_{DD}).



(1) V_{DD} = 3 V
(2) V_{DD} = 5 V

Fig. 34 Typical supply current during operating mode as a function of frequency.

A.C. CHARACTERISTICS (continued)



(1) T_{amb} = 85 °C
(2) T_{amb} = 25 °C

Fig. 35 Typical supply current (I_{DD}) in STOP mode as a function of the supply voltage (V_{DD}).

Table 8 Input timing shown in figure 36.

symbol	timing
t_{BUF}	$\geqslant 14t_{XTAL}$
$t_{HD;STA}$	$\geqslant 14t_{XTAL}$
t_{HIGH}	$\geqslant 17t_{XTAL}$
t_{LOW}	$\geqslant 17t_{XTAL}$
$t_{SU;STO}$	$\geqslant 14t_{XTAL}$
$t_{HD;DAT}$	> 0
$t_{SU;DAT}$	$\geqslant 250$ ns
t_{RD}	$\leqslant 1$ μs
t_{RC}	$\leqslant 1$ μs
t_{FD}	$\leqslant 1$ μs
t_{FC}	$\leqslant 0{,}3$ μs

Notes to Table 8

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 167 ns for f_{XTAL} = 6 MHz.
These figures apply to all modes.

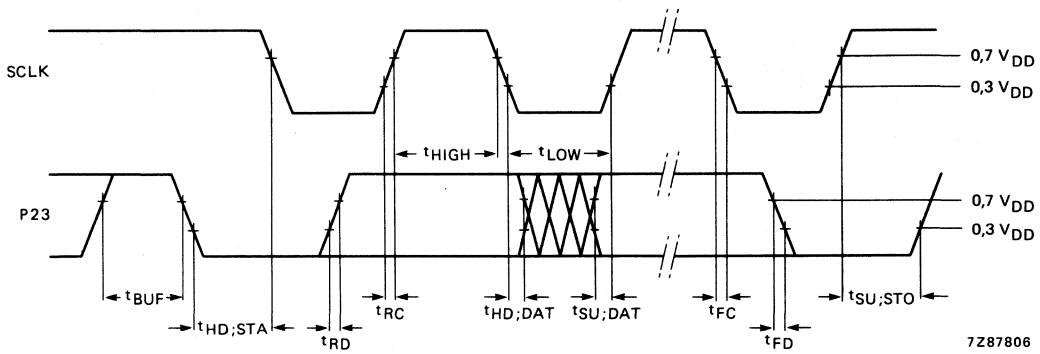


Fig. 36 PCF84C85 timing requirements for the P23 and SCLK *input* signals.

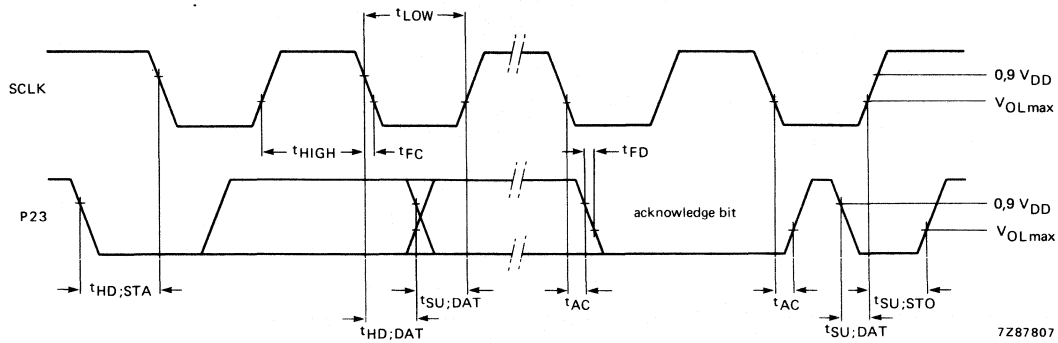


Fig. 37 PCF84C85 timing requirements for the P23 and SCLK *output* signals.

Table 9 Output timing shown in Figure 37

symbol	timing	
	normal mode (ASC in S2 = 0)	low-speed mode (ASC in S2 = 1)
$t_{HD;STA}$	$\frac{1}{2}$ (DF + 9) t_{XTAL}	$\frac{3}{4}$ (DF + 9) t_{XTAL}
t_{HIGH}	$\frac{1}{2}$ (DF) t_{XTAL}	$\frac{3}{4}$ (DF) t_{XTAL}
t_{LOW}	$\frac{1}{2}$ (DF) t_{XTAL}	$\frac{1}{4}$ (DF) t_{XTAL}
$t_{SU;STO}$	$\frac{1}{2}$ (DF − 3) t_{XTAL}	$\frac{1}{4}$ (DF − 3) t_{XTAL}
$t_{HD;DAT}$ (slave transmitter)		
any DF	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{HD;DAT}$ (master transmitter)		
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	–
for DF $\leqslant$ 99	–	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{SU;DAT}$ (master transmitter)		
for DF > 51	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$	–
for DF > 99	–	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$
t_{AC}	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
t_{FD}, t_{FC}	$\leqslant$ 100 ns at C_b = 400 pF	$\leqslant$ 100 ns at C_b = 400 pF

DEVELOPMENT DATA

Notes to Table 9

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 167 ns for f_{XTAL} = 6 MHz.
DF = divisor (see Table 2 Serial I/O section).
C_b = the maximum bus capacitance for each line.

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH LCD DRIVER

DESCRIPTION

The PCF84C430 microcontroller is a derivative of the PCF84CXX family of microcontrollers and is manufactured in CMOS technology. For detailed information see the "Single-chip 8-bit Microcontrollers user manual".

The PCF84C430 contains a PCF84CXX core CPU and is completely software compatible. In addition, the PCF84C430 contains an LCD driver supporting four back planes and a maximum driving capacity of up to 96 segments.

The PCF84C430 has 16 quasi-bidirectional I/O port lines, plus a derivative 8-bit port, a serial I/O interface, a single-level vectored interrupt circuit, an 8-bit timer/event counter and on-board clock oscillator and clock circuits.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 64-lead QFP package
- 4 K ROM bytes
- 128 RAM bytes
- On-chip LCD driver with 24 outputs (max. 96 segments)
- LCD multiplexing rates at 1:1 (static), 1:2, 1:3 and 1:4
- Low-power oscillator for LCD driver during STOP mode
- 25 quasi-bidirectional I/O port lines are configured as two 8-bit ports, a 1-bit port (shared with SDA) and an 8-bit derivative port
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C-bus hardware interface for serial data transfer on two separate lines
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V ($V_{SS} \leqslant V_{LCD} < V_{DD}$)
- STOP and IDLE mode
- Power-on-reset circuit
- Operating temperature range: −40 to + 85 °C

PACKAGE OUTLINE

PCF84C430H: 64-lead quad flat-pack; plastic (SOT208).

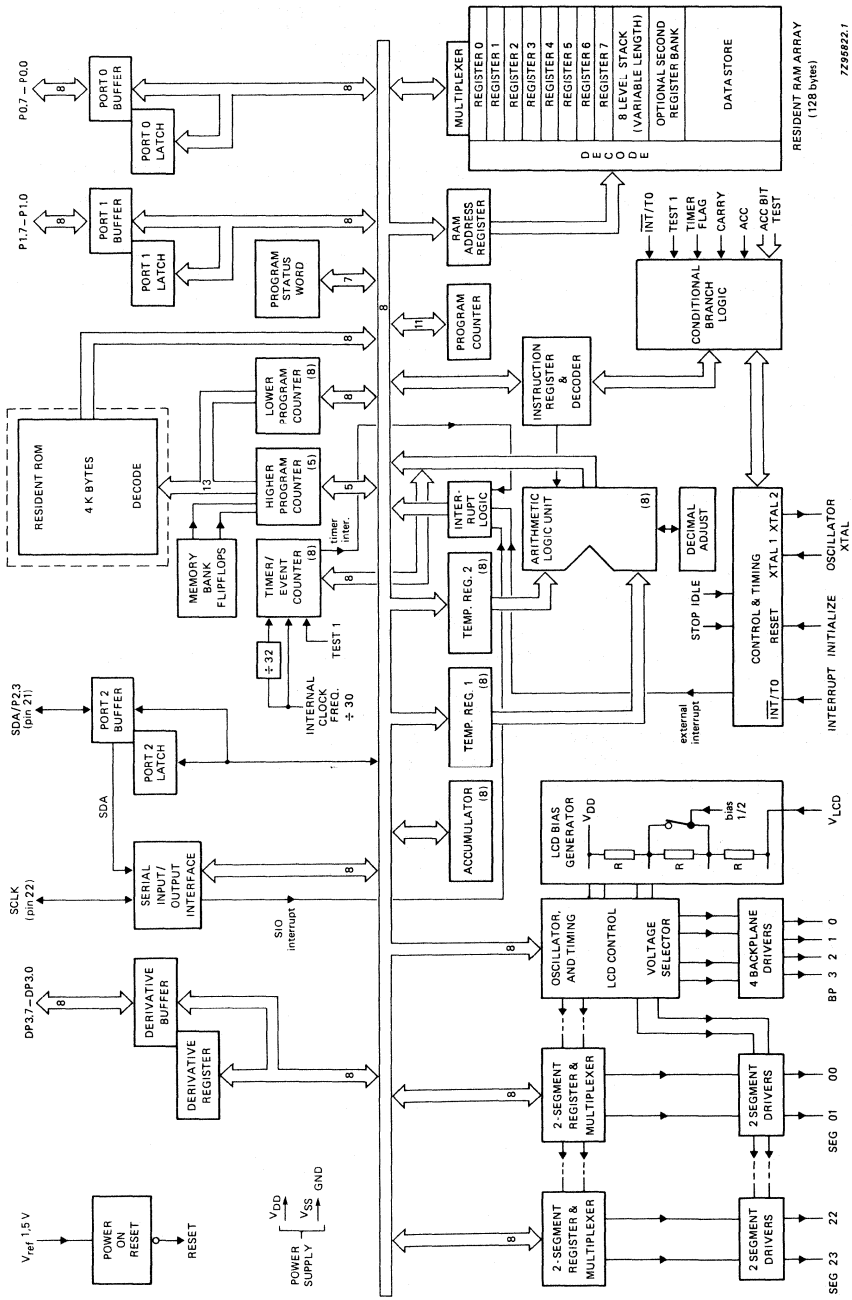


Fig. 1 Block diagram; PCF84C430.

DEVELOPMENT DATA

PINNING

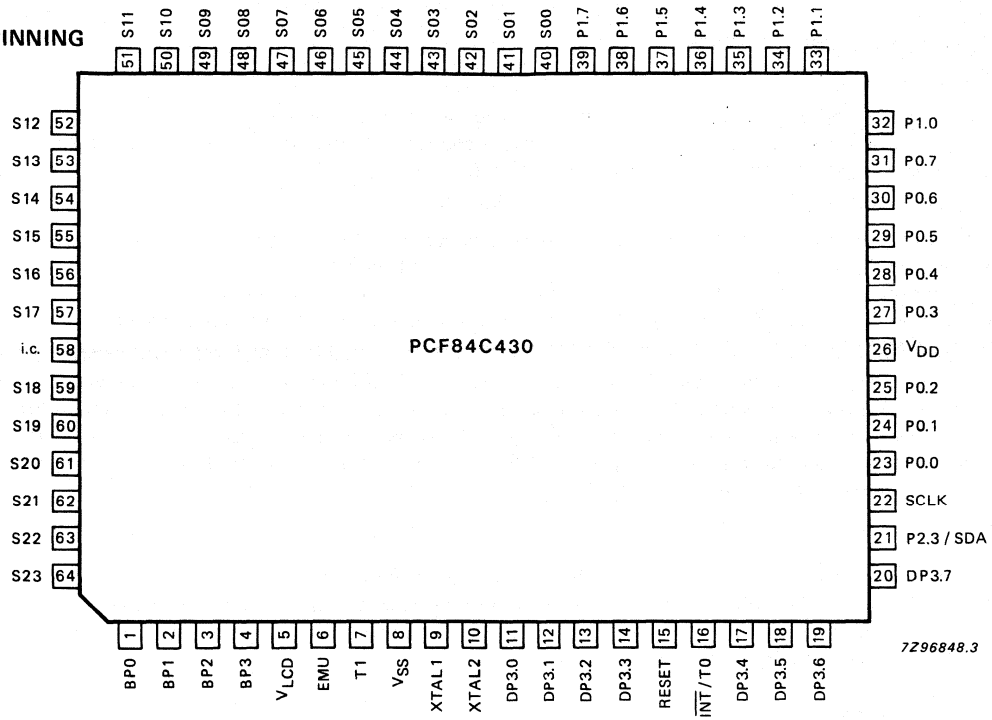


Fig. 2 Pin designation of the PCF84C430.

PIN DESIGNATION

pin	symbol	type	function
1-4	BP0-BP3	O	**LCD:** backplane outputs.
5	V_{LCD}		**LCD:** supply ground level.
6	EMU	I	**EMU pin:** to be grounded for normal operation.
7	T1	I	**Test 1:** test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
8	V_{SS}		**Ground:** circuit earth potential.
9	XTAL1	I	**Oscillator input:** crystal which determines the internal oscillator frequency or the external clock generator.
10	XTAL2	I/O	Connection to other side of oscillator.
11-14	DP3.0-DP3.3	I/O	**Derivative port 3:** 8-bit parallel port LSBs.
15	RESET	I/O	**Reset input:** used to initialize the processor (active HIGH), or output of power-on-reset circuit.
16	$\overline{INT}$/T0	I	**Interrupt/Test 0:** external interrupt input (sensitive to negative going edge)/test input; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
17-20	DP3.4-DP3.7	I/O	**Derivative port 3:** 8-bit parallel port MSBs.
21	SDA/P23	I/O	**Serial data:** input/output in serial I/O mode. If not selected as serial data pin, P23 functions as a quasi-bidirectional I/O line.
22	SCLK	I/O	**Serial clock:** bidirectional clock for serial I/O.
23-25 27-31	P0.0-P0.7	I/O	**Port 0:** 8-bit quasi-bidirectional I/O port.
26	V_{DD}		**Power supply:** 2,5 V to 5,5 V.
32-39	P1.0-P1.7	I/O	**Port 1:** 8-bit quasi-bidirectional I/O port.
40-57 59-64	S00-S23	O	**LCD** segment driver outputs.

FUNCTIONAL DESCRIPTION

Program memory

The program memory consists of 4 K bytes, in a read-only memory (ROM).
Each location is directly addressable by the program counter. The memory is mask-programmed at the factory. Figure 3 shows the program memory map.

Four program memory locations are of special importance:

- Location 0; contains the first instruction to be executed after the processor is initialized (RESET)
- Location 3; contains the first byte of an external interrupt service subroutine
- Location 5; contains the first byte of a serial I/O and interrupt service subroutine
- Location 7; contains the first byte of a timer/event counter interrupt service subroutine

Program memory is arranged in banks of 2 K bytes, which are selected by SEL MB instructions. The program memory is further divided into location 'pages', each of 256 bytes. This latter division applies only for conditional branches. Memory bank boundaries can be crossed only by using the unconditional branch instructions after the appropriate memory bank has been selected. A CALL instruction can transfer control to a subroutine on any 'page'; RET and RETR instructions can transfer control from a subroutine back to the main program.

Data memory

Data memory consists of 128 bytes, random-access data memory (RAM).
All locations are indirectly addressable using RAM pointer registers; up to 16 designated locations are directly addressable. Memory also includes an 8-level program counter stack addressed by a 3-bit stack pointer. Figure 4 shows the data memory map.

Working registers

Locations 0 to 7 are designated as working registers, directly addressable by the direct register instructions. Ease of addressing, and a minimum requirement of instruction bytes to manipulate their contents, makes these locations suitable for storing frequently addressed intermediate results. This bank of registers can be selected by the SEL RB0 instruction.

Executing the select register bank instruction SEL RB1, designates locations 24 to 31 as working registers, instead of locations 0 to 7, and these are then directly addressable. This second bank of working registers may be used as an extension of the first or reserved for use during interrupt service subroutines saving the first bank for use in the main program. If the second bank is not used, locations 24 to 31 may serve as general purpose RAM.

The first locations of each bank contain the RAM pointer registers R0, R1, R0' and R1', which indirectly address all RAM locations.

All RAM locations make efficient program loop counters when used with the decrement register and test instruction DJNZ.

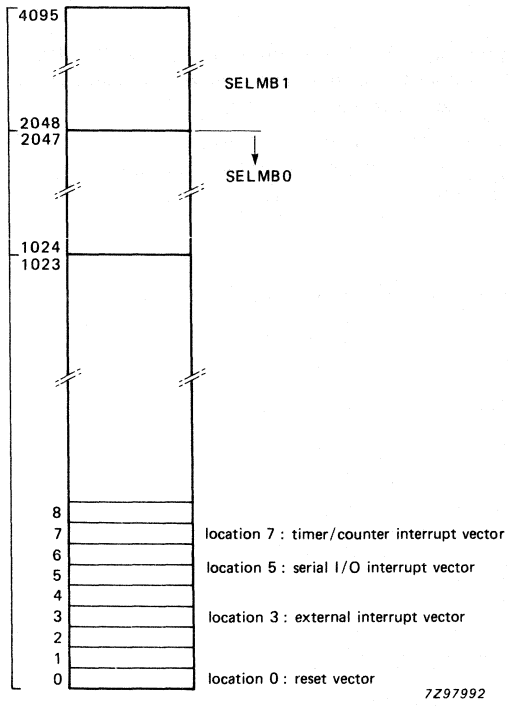


Fig. 3 Program memory map.

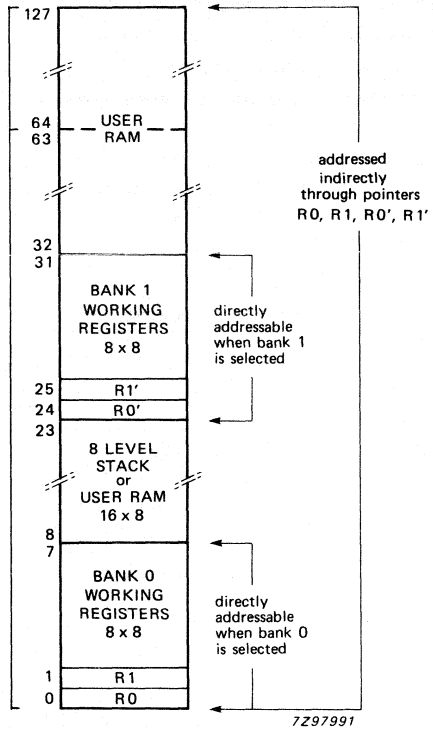


Fig. 4 Data memory map.

Program counter stack

Locations 8 to 23 may be designated as an 8-level program counter stack (2 locations per level), or as general purpose RAM. The program counter stack (Fig. 5) enables the processor to keep track of the return addresses and status generated by interrupts or CALL instructions by storing the contents of the program counter prior to servicing the subroutine. A 3-bit stack pointer determines which of the eight register pairs of the program counter stack will be loaded with the next generated return address.

The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. On the first subroutine CALL or interrupt, the contents of the program counter and bits 4, 6 and 7 of the program status word (PSW) are transferred to locations 8 and 9. The stack pointer increments by one and points to locations 10 and 11 ready for another CALL. Because an address may be up to 13 bits long, two bytes must be used to store each address.

At the end of a subroutine, which is signalled by a return instruction (RET or RETR), the stack pointer decrements by one and the contents of the register pair on top of the stack are transferred to the program counter. The saved PSW bits are transferred to the PSW only by the RETR instruction.

If not all 8 levels of subroutine and interrupt nesting are used, the unused portion of the stack may be used as any other indirectly addressable RAM locations.

FUNCTIONAL DESCRIPTION (continued)

Program counter stack (continued)

Nesting of subroutines within subroutines can continue up to 8 times without overflowing the stack. If overflow does occur the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

The value of the saved contents of the program counter is different for an interrupt CALL compared to a normal CALL to subroutine. With an interrupt CALL, the program counter return address is saved; with a subroutine CALL, the saved program counter value is one less than the program counter return address.

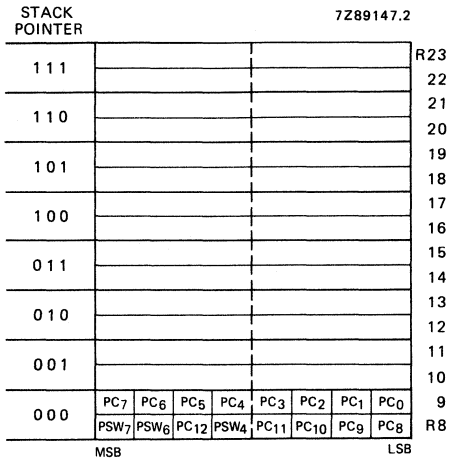


Fig. 5 Program counter stack.

IDLE and STOP modes

Idle mode

When the microcontroller enters the IDLE mode via the IDLE instruction (01 H) the oscillator, timer/counter and serial I/O are kept running. The microcontroller exits from the IDLE mode by one of three interrupts if they are enabled,or by activating a RESET. If the interrupt is not enabled the processor will remain in the IDLE mode. An active signal on the RESET pin restarts the microcontroller and a normal RESET sequence is executed (see Fig. 6).

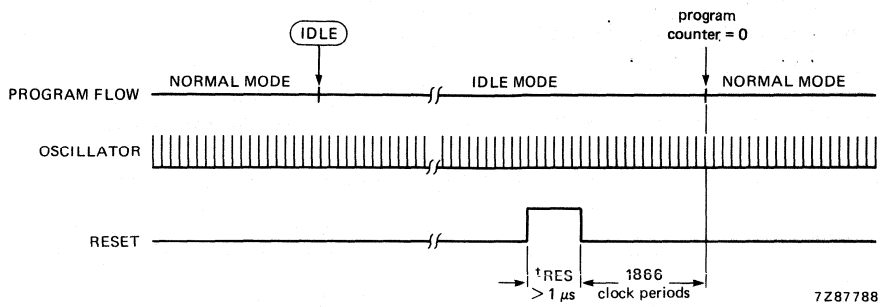


Fig. 6 Exit from IDLE mode via a RESET.

An active signal coming from an enabled interrupt causes the execution of the normal interrupt routine since normal interrupt scanning is still being carried out. A HIGH-to-LOW transition on the external interrupt pin ($\overline{INT}$/T0) reactivates the microcontroller. A LOW level applied to $\overline{INT}$/T0 will reactivate the microcontroller only in the STOP mode. Thus, if $\overline{INT}$/T0 was LOW before the microcontroller entered the IDLE mode, it must go HIGH before the microcontroller can be reactivated (see Fig. 7.).

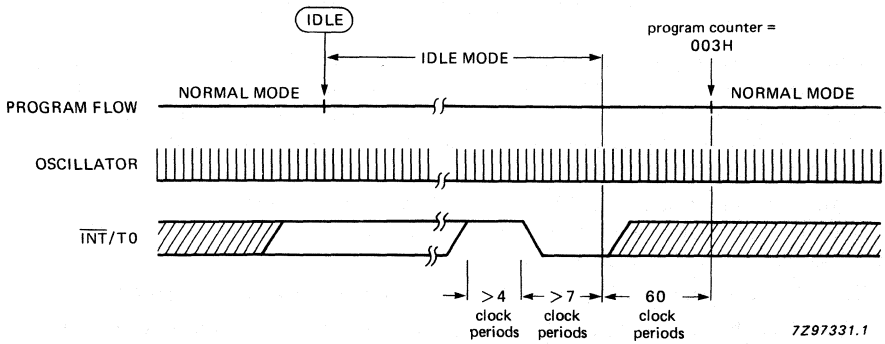


Fig. 7 Exit from IDLE mode via an interrupt.

Wake-up from the IDLE mode is ensured when $\overline{INT}$/T0 is HIGH for at least 4 CP (clock periods) followed by a LOW for 7 CP. After the initial forced CALL 003 H operation (60 CP) the program continues with the external interrupt service routine. During IDLE mode operation, the address of the instruction immediately following that which caused the processor to enter the IDLE mode is present on the address bus.

STOP mode

The microcontroller enters the STOP mode via the STOP instruction (22H). The oscillator is switched off but internal status of the CPU, RAM contents and the state of I/O ports are unaffected. The microcontroller can be brought-out of the STOP mode by an active signal at the external interrupt input or by an external RESET signal. When one of these two signals is applied an internal delay of 1866 CP is provided to ensure that all internal clocks are operating correctly before restart (see Fig. 8). Note: the start-up time of a crystal oscillator is measured in milliseconds, and the 1866 CP count begins after this start-up time.

If the microcontroller exits from the STOP mode by activating RESET, a normal RESET sequence is executed.

FUNCTIONAL DESCRIPTION (continued)

STOP mode (continued)

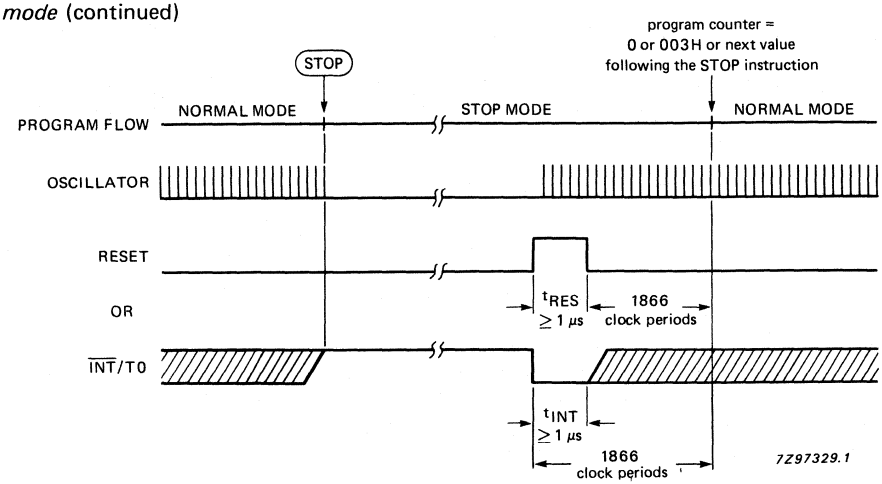


Fig. 8 Entering and exiting the STOP mode.

If the microcontroller exits the STOP mode by pulling the external interrupt input pin LOW, an interrupt sequence is executed only if the external interrupt is enabled. In this event the microcontroller resumes the normal program sequence after returning from the interrupt routine, as in the normal mode. If the interrupt is not enabled, it continues the normal program sequence, executing the instruction following the STOP instruction.

The microcontroller is restarted by a LOW level applied at the $\overline{INT}$/T0 pin.
Note: when leaving the STOP mode via an interrupt, a further instruction in the main program series is executed prior to entering the interrupt routine.

When the $\overline{INT}$/T0 level is active during the STOP instruction then no STOP is executed.

A LOW level on the external interrupt input of at least 1 μs will cause the microcontroller to exit the STOP mode. During the STOP mode, the address of the instruction immediately following the last STOP instruction is present on the address bus.

I/O facilities

The PCF84C430 has 25 quasi-bidirectional I/O lines arranged as:

- Port 0 — parallel port of 8 lines (P0.0 to P0.7)
- Port 1 — parallel port of 8 lines (P1.0 to P1.7)
- Port 2 — I/O port of 1 line (SDA/P2.3) active when not selected as serial I/O
- Port 3 — a derivative 8-bit parallel port (DP3.0 to DP3.7)

In addition 4 specialized I/O lines are comprised:

- SCLK — serial I/O clock line
- SDA/P2.3 — serial I/O data line
- $\overline{INT}$/T0 — external interrupt and test input. When used as a test input it can be directly tested by conditional branch instructions JT0 and JNT0
- T1 — test input which can alter program sequences when tested by conditional jump instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter.

Parallel ports

All parallel ports can be used as outputs or inputs, their structure is quasi-bidirectional.
Output data written to a port is latched and remains unchanged until rewritten.
Input data is not latched and so must be present until read by an input instruction.

Input lines are fully CMOS compatible, output lines can drive one TTL or CMOS load.

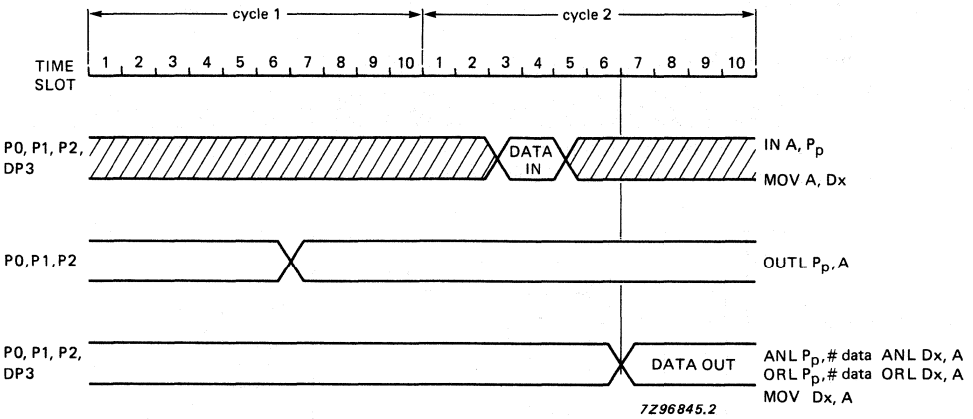


Fig. 9 Shows the timing diagram for all ports using IN, OUTL, ANL and ORL instructions. For the OUTL instruction data changes on time slot 7 of cycle 1. For the MOV, ANL and ORL instructions, the ports change on time slot 7 of cycle 2.

DEVELOPMENT DATA

Fig. 10 shows the quasi-bidirectional I/O interface with push-pull output and switched pull-up current source.
Each line is pulled up to V_{DD} via a constant current source (TR4), which is enabled via TR3 whenever one of the two output latches contains a logic 1. This current source is sufficient for a TTL HIGH level, yet can be pulled LOW by an external CMOS device, thus allowing the same pin to be used for both input and output.

When a logic 1 is written to the line for the first time (MQ = 1, SQ = 0), TR2 is switched on for the duration of the internal write pulse (one oscillator period), to provide a fast transition from logic 0 to logic 1. Subsequent writing of a logic 1 to the port lines will not switch TR2 on. This prevents unnecessary current through external components connected to the port lines of the same port which might be in the input mode and also connected to ground.

When a logic 0 is written to the line, TR3 switches off the current source. Current sinking capability is provided by TR1, which is now switched on. When used as an input, a logic 1 must first be written to the line, otherwise TR1 will remain low impedance.

FUNCTIONAL DESCRIPTION (continued)

Parallel ports (continued)

The PCF84C430 family offers the possibility to select individually 24 of the 25 parallel port pins (not P2.3)* from the following mask options:

Option 1 – STANDARD PORT; quasi-bidirectional I/O with switched pull-up current source of 100 μA (typ.) and P-channel booster transistor TR2.
TR2 is only active during 1 clock cycle (Fig. 10).

Option 2 – OPEN DRAIN; quasi-bidirectional I/O with only an N-channel open drain output. Application as an output requires connection of an external pull-up resistor (Fig. 11). When an open drain port is unused it must be connected to V_{SS}.

Option 3 – PUSH-PULL OUTPUT; drive capability of the output is 1,6 mA (min.) at V_{DD} = 5 V in both polarities. To avoid a large current flowing through the output transistors during the input mode, these push-pull pins must only be used as outputs (Fig. 12).
Note: the port latch may be read back using the IN A,pp instruction.

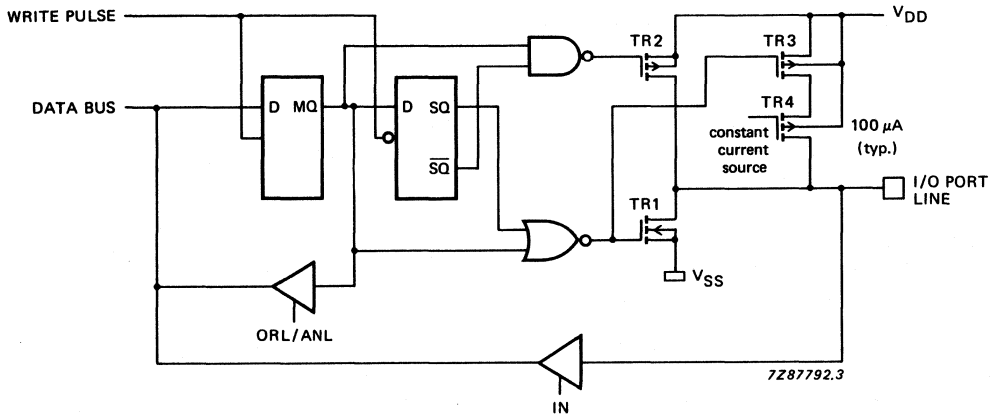


Fig. 10 Standard output with switch pull-up current source.

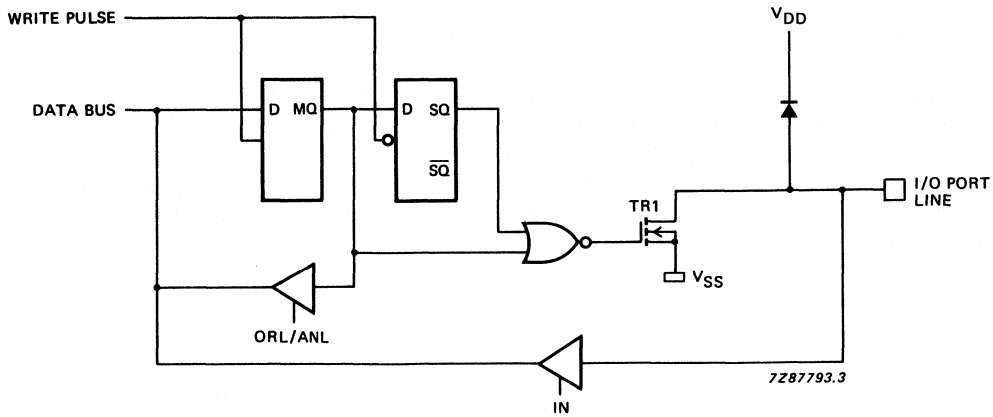


Fig. 11 Open drain output.

* P2.3 is always open drain.

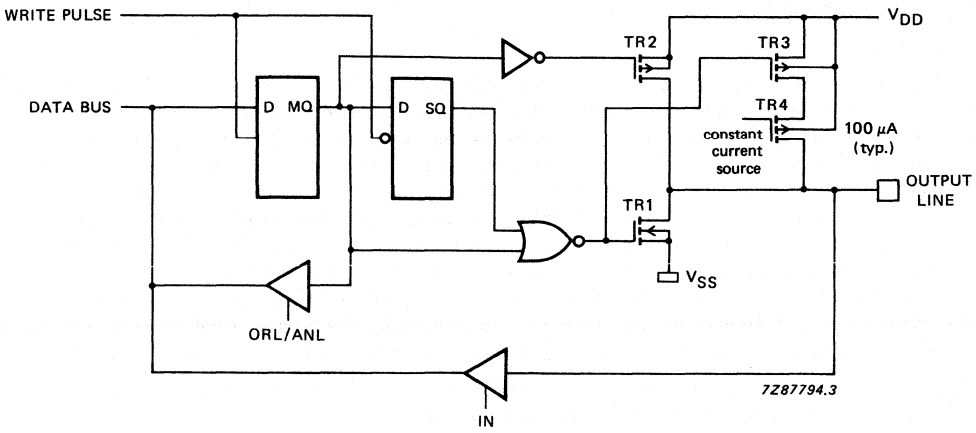


Fig. 12 Push-pull output.

Derivative I/O addresses

For extension of the I/O facilities, instructions MOV A,Dx, MOV Dx,A, ANL Dx,A and ORL Dx,A have been added to the instruction set. The derivative register address is the second byte of the instruction. The address map for the derivative registers is given in Table 1.

Table 1 address map of PCF84C430 derivative registers

Dx	R/W	bits	description
4	R/W	8	PR3; derivative I/O port 3 latch
5	R	8	PR3; derivative I/O port 3 input pins
16	R/W	8	LCDC; LCD control register
17-28	R/W	8	LCDB1-LCDB12; 12 consecutive segment data bytes

Serial I/O (SIO)

The PCF84C430 has an on-chip serial I/O interface that supports I^2C-bus communication. Whereas a normal microcontroller must regularly monitor the serial data bus for the presence of data, the serial I/O interface detects, receives and converts the serial data stream into parallel format without interrupting the execution of the current program. An interrupt is sent to the PCF84C430 only when a complete byte is received. It then reads the data byte in one instruction.

During transmission, the serial I/O interface performs parallel to serial conversion and subsequent serial output of the data. The microcontroller is only interrupted in the execution of its programmed tasks when a complete byte has been transmitted.

FUNCTIONAL DESCRIPTION (continued)

Serial I/O (SIO) (continued)

The design of the PCF84C430 serial I/O system allows any number of devices from PCF85XX family (clips) to be connected via the two-line serial bus. The ability of any devices to communicate, without interrupting the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to a message prefixed with its own address or the 'general CALL' address. Address recognition is performed by the interface hardware so that operation of the microcontroller need only be interrupted when a valid address has been received. This saves significant processing time and memory space compared with a conventional microcontroller employing a software serial interface. When the addressing facility is not required, for instance in a system with only two microcontrollers, direct data transfer without addressing can be performed. In multi-master systems, an automatically, invoked arbitration procedure prevents two or more devices from continuing simultaneous transmission.

In NORMAL (running) and IDLE mode, the serial I/O logic remains active; its internal system clock will be switched off when there is no activity on the serial bus.

After execution of the STOP instruction, the oscillator of the PCF84C430 is switched off. This means that the serial I/O logic will remain in the state it was at the occurance of the STOP instruction. To avoid "bus block" problems and to assure correct start-up of the bus after exit from the STOP mode, the user should disable the serial logic (ESO = 0) prior to the execution of the STOP instruction. This must be carried out only when the PCF84C430 has finished a serial data transfer.

After a negative-going RESET signal, the first 30 clock pulses of the 1866-pulse initialization phase set P2.3/SDA and SCLK to HIGH. When P2.3/SDA or SCLK are not used they must be connected to V_{SS}.

Serial I/O interface

Figure 13 shows the serial I/O interface. The clock line of the serial bus has exclusive use of pin 22 (SCLK) while the data line shares pin 21 (SERIAL DATA) with the I/O line P2.3 of port 2. When the serial I/O is enabled, P2.3 is disabled as a parallel port line, (P2.3 and SCLK only open drain).

The microcontroller and interface communicate via the internal microcontroller bus and the Serial Interrupt Request line. Data and information controlling the operation of the interface are stored in four registers:

- Data shift register (S0)
- Serial I/O interface status word (S1)
- Serial clock control word (S2)
- Address register (SO')

Data shift register (S0)

Register S0 converts serial data to parallel format and vice versa. A pending interrupt is generated only after a complete byte has been transmitted, or after a complete data byte, specific address or 'general CALL' address has been received. The most significant bit is transmitted first.

Serial I/O interface status word (S1)

Register S1 provides information concerning the state of the interface and stores information from the microcontroller. Bits 0 to 3 are duplicated: control bits in these positions can only be written by the microcontroller, while status bits can only be read.

MST and TRX (see Table 2)

These bits determine the operating mode of the serial I/O interface.

Table 2 Operating modes of the serial I/O interface

MST	TRX	operating mode
0	0	slave receiver
1	0	master receiver
0	1	slave transmitter
1	1	master transmitter

BB: Bus Busy.

This is the flag which indicates the status of the bus.

PIN: Pending Interrupt Not

PIN = '0' indicates the presence of a pending interrupt, which will cause a Serial Interrupt Request when the serial interrupt mechanism is enabled.

ESO: Enable Serial Output

The ESO flag enables/disables the serial I/O interface: ESO = 1 enables, ESO = 0 disables. ESO can only be written by software.

BC0, BC1 and BC2

Bits BC0, BC1 and BC2 indicate the number of bits received or transmitted in a data stream. These bits can only be written by software.

AL: Arbitration Lost

The arbitration lost flag is set by hardware when the serial I/O interface, as master transmitter, loses a bus arbitration procedure.

AAS: Addressed As Slave

This flag is set by hardware when the interface detects either its own specific address or the 'general CALL' address as the first byte of a transfer and the interface has been programmed to operate in the address recognition mode.

AD0: Address Zero

This flag is set by hardware after detection of the 'general CALL' address when the interface is operating in the address recognition mode.

LRB: Last Received Bit

This contains either the last data bit received or, for a transmitting device in the acknowledgement mode, the acknowledgement signal from the receiving device.

Bits AL, AAS, AD0 and LRB can only be read by software.

FUNCTIONAL DESCRIPTION (continued)

Serial I/O interface (continued)

Serial clock control word (S2)

Bits 0 to 4 of the clock control register S2 are used to set the frequency of the serial clock signal. When a 6 MHz crystal is used, the frequency of the serial clock can be varied between 154 kHz and 1 kHz (see Table 3).
An asymmetrical clock with a HIGH-to-LOW ratio of 3:1 can be generated using bit 5. The asymmetrical clock allows a microcontroller more time per clock period for sampling the data line, making the timing of this action less critical. Bit 6 can be used to activate the acknowledge mode of the serial I/O.
S2 is a write only register.

Address register

The address register contains the 7-bit address back-up latches and the bit (ALS) used to enable/disable the address recognition mode. The address register can be written using the MOV S0, A and MOV S0, # data instructions, but only when ESO = 0 .

Serial I/O interrupt logic

An EN SI instruction enables and a DIS SI instruction disables the interrupt logic. When the logic is enabled, a pending interrupt results in a serial I/O interrupt to the processor, causing a CALL to location 5 in the ROM. When disabled, the presence of an interrupt is still indicated by PIN in S1, allowing the interrupt to be serviced. However, vectored interrupt will not occur.

Table 3 SIO clock pulse frequency control when using a 6 MHz and a 10 MHz crystal

hexadecimal S20-S24 code	divisor	f_{XTAL} (6 MHz) f_{SCLK} (kHz)▲	f_{XTAL} (10 MHz) f_{SCLK} (kHz)▲
0	not allowed		
1	39	*154	*256
2	45	*133	*222
3	51	*118	*196
4	63	95	*159
5	75	80	*133
6	87	69	*115
7	99	61	*101
8	123	49	81
9	147	41	68
A	171	35	58
B	195	31	51
C	243	25	41
D	291	21	34
E	339	18	29
F	387	16	26
10	483	12	21
11	579	10	17
12	675	8,9	15
13	771	7,8	13,4
14	963	6,2	10,4
15	1155	5,2	8,7
16	1347	4,5	7,4
17	1539	3,9	6,5
18	1923	3,1	5,2
19	2307	2,6	4,3
1A	2691	2,2	3,7
1B	3075	2,0	3,3
1C	3843	1,6	2,6
1D	4611	1,3	2,2
1E	5379	1,1	1,9
1F	6147	1,0	1,6

DEVELOPMENT DATA

* Not permitted for I^2C operation.

▲ The maximum clock frequency in the I^2C systems is 100 kHz.

FUNCTIONAL DESCRIPTION (continued)

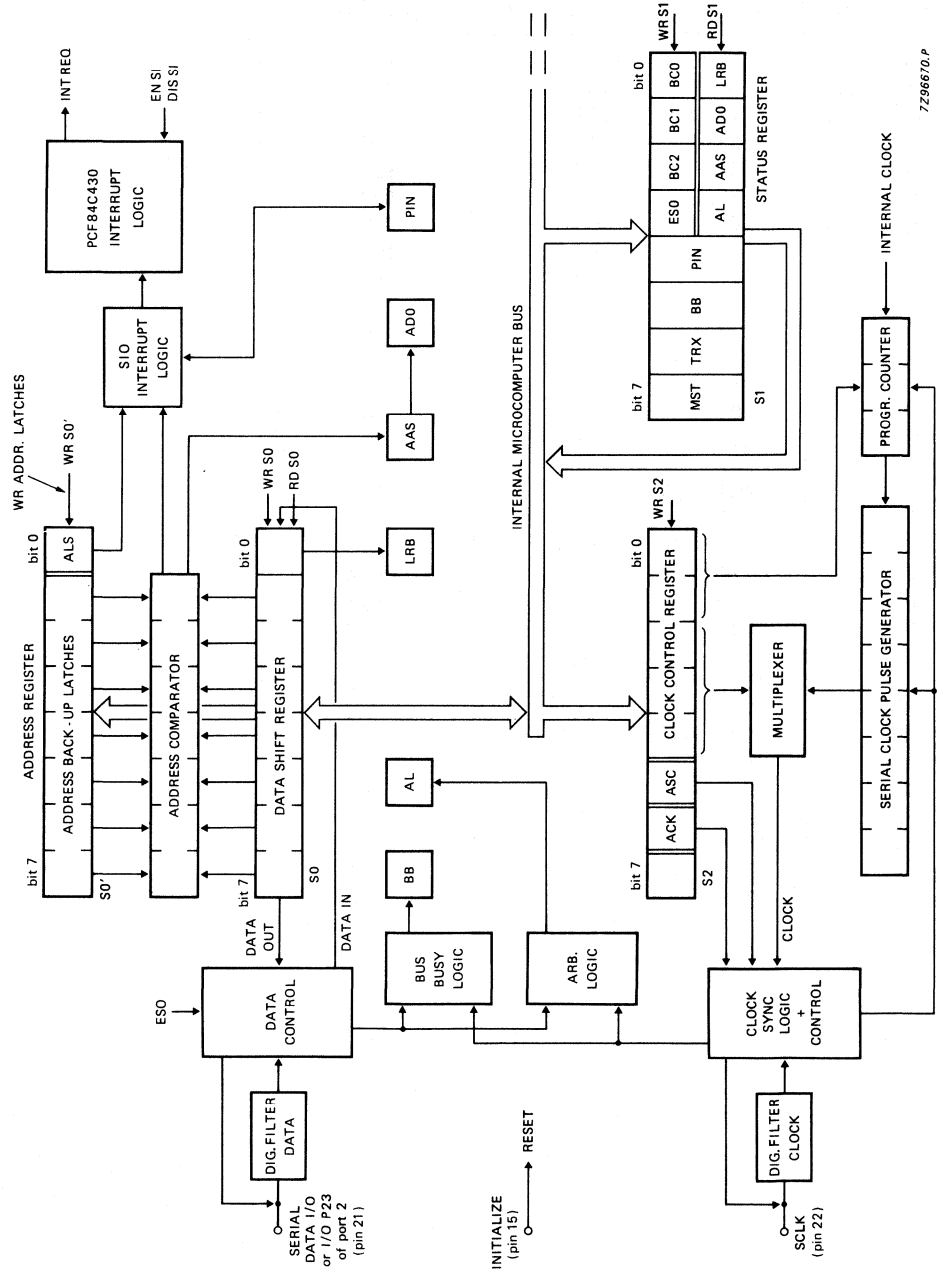


Fig. 13 Serial I/O interface.

Interrupts

Upon entering an interrupt routine, the contents of the program counter and bits 4, 6 and 7 of the PSW are saved in the program counter stack. The contents of the accumulator must be saved by user software. Interrupt acknowledgement may be carried out by software via I/O ports. All interrupt routines must reside in memory bank 0; the SEL MB instructions may not be used within an interrupt routine. An interrupt routine can only be terminated by the RETR (return and restore) instruction. During an interrupt routine, further subroutine calls must be terminated using the RET instruction. Using the RETR instruction to terminate such a nested subroutine would terminate the interrupt routine prematurely.

External interrupt

When the external interrupt is enabled and no interrupt routine is in progress, a HIGH-to-LOW transition on the $\overline{INT}$/T0 pin sets the External Interrupt Flag (EIF) and invokes the external interrupt routine by forcing a CALL to location 3*. The program counter points to the external interrupt vector address (003 H) between 2,6 and 3,6 machine cycles after the transition occurs. Interrupt latency will depend upon the instruction that is being executed when the transition occurs. If an interrupt routine is already in progress, an external interrupt request is stored in the External Interrupt flag (EIF). When the external interrupt is disabled the request is still latched into the digital filter. Execution of a DIS I instruction cancels a stored interrupt request by clearing both the digital filter and the (EIF).

Another external interrupt can be created by enabling the timer/event counter interrupt and loading FFH into the counter (one less than overflow). The STRT CNT instruction is then executed in user software, this enables the event counter mode and a LOW-to-HIGH transition on the T1 input will then initiate an interrupt subroutine and invoke a call to the timer/counter interrupt vector location 7.

SIO Interrupt

An interrupt request from the SIO hardware will set the PIN flag to its active LOW state. This action is fully independant of the Enable SIO interrupt flag. When the SIO interrupt is enabled and no interrupt routine is in progress, the PIN flag at active LOW will invoke the SIO interrupt routine by forcing a CALL to program memory location 5. After the SIO interrupt is initiated, the PIN flag is **not** automatically set back to a HIGH state, this must be done as part of the interrupt subroutine.

Timer/counter Interrupt

When no interrupt routine is in progress and the timer/counter is enabled, a timer/counter overflow sets the Timer interrupt flag (TIF). This initiates the timer interrupt routine by forcing a CALL to program memory location 7**. If an interrupt routine is in progress, the interrupt request is stored in the (TIF) only if the timer interrupt has been enabled. Execution of a DIS TCNTI instruction deletes a previously stored interrupt request. The timer flag (TF) is set every time the timer/counter overflows and is not automatically reset after the timer counter routine is called. It can only be cleared by either the JTF or JNTF or by a hardware RESET.

Interrupt Priority

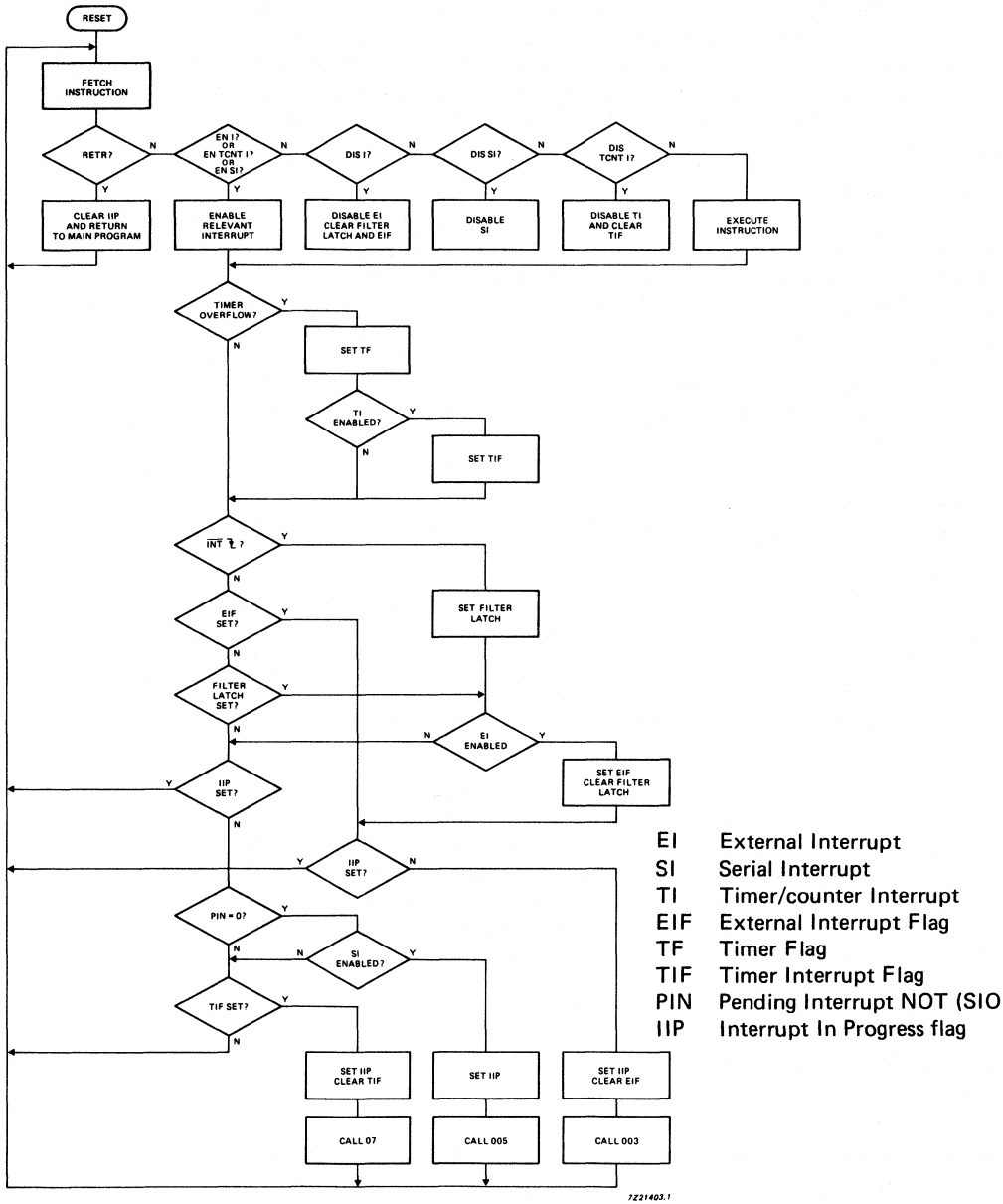
If simultaneous interrupts occur, their priority is as follows:

- External (highest)
- SIO
- Timer/Counter (lowest)

An interrupt routine can only be interrupted by a hardware RESET and cannot be interrupted by other interrupts (which will be latched). When the interrupt routine is terminated by the RETR instruction, at least one instruction of the main program will be executed before another interrupt routine is entered.

* This CALL clears the EIF flag.
** This CALL clears the TIF flag.

FUNCTIONAL DESCRIPTION (continued)



EI	External Interrupt
SI	Serial Interrupt
TI	Timer/counter Interrupt
EIF	External Interrupt Flag
TF	Timer Flag
TIF	Timer Interrupt Flag
PIN	Pending Interrupt NOT (SIO)
IIP	Interrupt In Progress flag

Fig. 14(a) Flow chart illustrating the interrupt handling sequence.

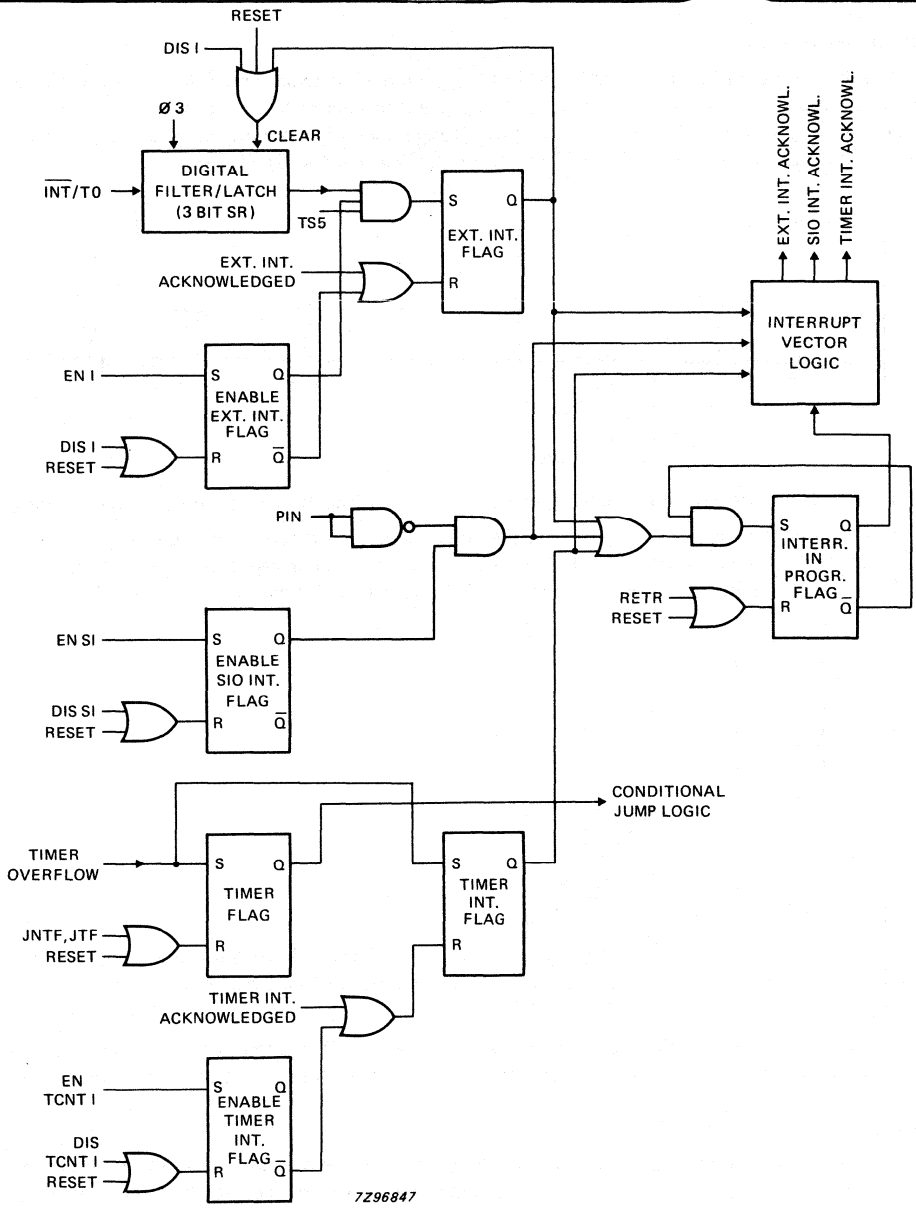


Fig. 14(b) Simplified schematic of interrupt logic, to be used in conjunction with the functional description.

Note to figure

1. $\overline{INT}$/T0 negative edge is always latched in the digital filter/latch.
2. Correct interrupt timing is ensured when $\overline{INT}$/T0 is HIGH for $>$ 4 CP followed by a LOW for $>$ 7 CP.
3. When the interrupt in progress flat is set, further external and timer interrupts are latched but ignored, until RETR is executed.
4. A DIS I instruction always clears a pending external interrupt.
5. For all flip-flops, RESET overrules SET.

Oscillator (see Fig. 15)

The oscillator can be inhibited by the STOP instruction under software control. It is also inhibited when a low-supply voltage condition is present to prevent discharge of a weak back-up battery. Provided the supply voltage is within the operating range the oscillator will be restarted after a STOP instruction by a LOW level at the $\overline{INT}$/T0 pin or a HIGH level at the RESET pin.

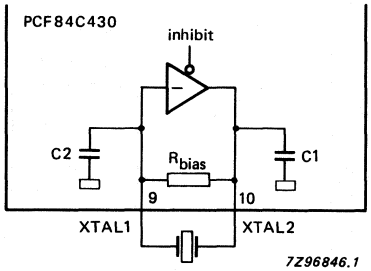


Fig. 15 Oscillator with integrated elements.

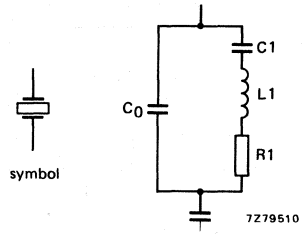


Fig. 16 Crystal unit equivalent circuit.

The values of crystal series resistance R1 and the crystal's total load capacitance C_L (C_0 + wiring + external capacitors) must not be above the curve (Fig. 17) for the corresponding frequency.
Note: if external capacitors are connected to XTAL 1 and XTAL 2 they must be of equal value.

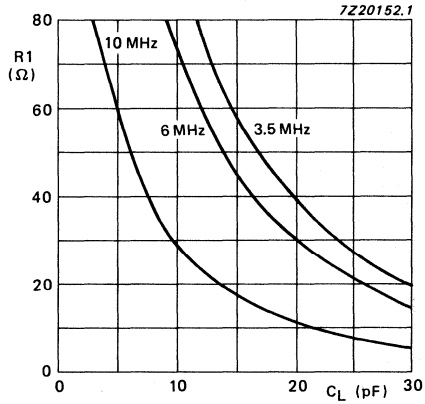


Fig. 17 Crystal circuit series resistance (R1) as a function of load capacitance (C_L).

The oscillator has the output drive capability via pin 10 (XTAL 2). An external clock can be applied to pin 9 (XTAL 1). A machine cycle consists of 10 time slots, each time slot being 3 oscillator periods.

Timer/event counter (see Fig. 18)

An internal 8-bit up-counter is provided. It can count external events, modulo-32 machine cycles, or machine cycles directly. Table 4 gives the instructions that control the counter and the prescaler, and the functions performed.

When used as a timer, the input to the counter is either the overflow or input of a 5-bit prescaler. When used as an event counter, LOW-to-HIGH transitions on pin T1 are counted. The counter is incremented during a machine cycle only if the falling edge occurs during the first 7 time slots; otherwise it is incremented during the next cycle. The maximum rate at which the counter may be incremented is once every machine cycle. When the counter overflows, the Timer flag is set. The flag can be tested and reset using the JTF (jump if Timer flag = logic 1) or JNTF (jump if Timer flag = logic 0) instruction. Overflow also generates an interrupt request to the processor via setting of the Timer Interrupt Flag when the timer/event counter interrupt is enabled.

Table 4 Timer/event counter control

function	timer mode modulo-1, modulo-32*	counter mode
CLEAR	MOV T,A (A) = 0 or RESET	MOV T,A (A) = 0 or RESET
PRESET	MOV T,A	MOV T,A
START	STRT T	STRT CNT
STOP	STOP TCNT or RESET	STOP TCNT or RESET
TEST	JTF/JNTF	JTF/JNTF
READ**	MOV A,T	MOV A,T

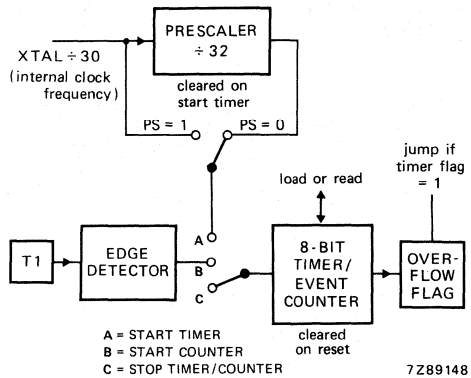


Fig. 18 Timer/event counter.

Program status word (see Fig. 19)

The program status word (PSW) is an 8-bit word (1 byte) in the CPU which stores information about the current status of the microcontroller.
The PSW bits are:

- Bits 0 to 2 — stack pointer bits (SP_0, SP_1, SP_2)
- Bit 3 — prescaler select (PS);
  0 = modulo-32; 1 = modulo-1 (no prescaling)
- Bit 4 — working register bank select (RBS);
  0 = register bank 0; 1 = register bank 1
- Bit 5 — not used (1)
- Bit 6 — auxiliary carry (AC); half-carry bit generated by an ADD instruction and used by the decimal adjust instruction DA A
- Bit 7 — carry (CY); the carry flag indicates that previous operation has resulted in an overflow of the accumulator.

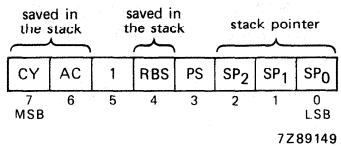


Fig. 19 Program status word.

* With prescaler select, PS = logic 0, the timer is incremented every 32 machine cycles; with PS = logic 1 the timer will be incremented every machine cycle (prescaler not used); the prescaler is cleared by the STRT T instruction and is not readable.

** READ does not disturb the counting process.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Program status word (continued)

All bits can be read using the MOV A, PSW instruction. Bits 7 and 6 are set and cleared by CPU operation. Bit 4 can be changed by a SEL RB instruction, bit 3 by the MOV PSW, A instruction, and bits 0, 1 and 2 by the CALL, RET or RETR instructions in the event of an interrupt. Bits 7, 6 and 4 are stored in the program counter stack during subroutine and interrupt calls. These bits are restored in the PSW with a RETR (return and restore) instruction which must be used at the end of an interrupt and can be used at the end of a normal routine, which is not part of an interrupt subroutine. The RET instruction has no restore feature and must not be used at the end of an interrupt.

Program counter (see Fig. 20)

The 12-bit program counter is able to address 4 K bytes of ROM. The arrangement of the bits is shown in Fig. 20. During an interrupt subroutine PC_{11} is forced to logic 0. All 12 bits are saved in the stack during CALL and interrupt routines.

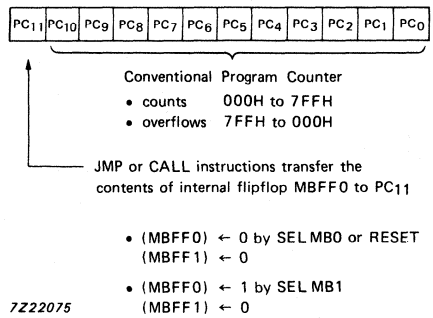


Fig. 20 Program counter.

Central processing unit

The PCF84C430 has arithmetic, logical and branching capabilities. The DA A, SWAP A and XCHD instructions simplify BCD arithmetic and the handling of nibbles. The MOVP A,@A instruction permits efficient table look-up from the current ROM page.

Conditional branch logic

The conditional branch logic within the processor enables several conditions, internal and external to the processor, to be tested by the user's program. Table 5 lists the conditional jump instructions used to change the program sequence. The DJNZ instruction decrements a designated register or data memory location and branches if the contents are not zero. This instruction is useful for looping control. The JMPP@A instruction allows multiway branches to destinations determined by the contents of the accumulator.

Table 5 Conditional branches

test	jump condition	jump instruction
accumulator	all bits zero	JZ
	any bit non-zero	JNZ
accumulator bit test	1	JB0 to JB7
carry flag	1	JC
	0	JNC
timer overflow flag	1	JTF
	0	JNTF
test input T0	1	JT0
	0	JNT0
test input T1	1	JT1
	0	JNT1
register	non-zero	DJNZ

Test input T1 (pin 7)

The T1 input line can be used as:

- A test input for branch instructions JT1 and JNT1
- An external input to the event counter

When used as a test input:

- JT1 instruction tests for logic 1 level
- JNT1 instruction tests for logic 0 level

When used as an input to the event counter, T1 must be LOW for > 4 CP, followed by a HIGH for > 4 CP. A transition can be recognized every 30 oscillator clock periods (1 machine cycle).

There is no internal pull-up or pull-down resistor connected to the T1 input. If required it must be externally connected to a resistor ($R = \leqslant 100\ k\Omega$). When T1 is not used pin 7 must be connected V_{DD} or V_{SS}.

Reset (pin 15)

A positive-going signal on the RESET input/output

- Sets the program counter to zero
- Selects location 0 of memory bank 0 and register bank 0
- Sets the stack pointer to zero (000); pointing to RAM address 8
- Disables the interrupts (external, timer and serial I/O)
- Stops the timer/event counter, then sets it to zero
- Sets the timer prescaler to divide by 32
- Resets the timer flag
- Sets all ports except P2.3 to input mode (see serial I/O section)
- Sets the serial I/O to slave receiver mode and disables the serial I/O
- Cancels IDLE and STOP mode
- Re-defines the LCD control byte

A negative-going signal on the RESET input/output:

- Sets P2.3/SDA and SCLK to HIGH after a maximum of 30 clock pulses
- Sets the serial I/O to slave receiver mode and disables the serial I/O after a maximum of 30 clock pulses
- Starts program execution after 1866 clock pulses

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Power-on reset

The internal power-on reset circuit monitors the PCF84C430 supply voltage V_{DD}. For as long as the supply voltage remains below the internal reference level V_{ref} (typically 1,5 V) the oscillator is inhibited and RESET (pin 15) has an undefined level. When V_{DD} rises above the internal reference level, the oscillator is released and RESET is pulled high to V_{DD} by TR1 for a period t_D (typically 50 μs).

N.B. Because of the narrow bandwidth of the crystal, the start-up time of the oscillator is typically 10 ms.

Three modes of power-on reset are possible:

1. If V_{DD} can be switched with a fast rise time i.e. V_{DD} reaches its minimum operating value (corresponding to the selected oscillator frequency) before the RESET signal (t_D) has finished, then no extra components are required (see Fig. 21 and 22). Note that the first instruction is executed after the oscillator start-up time plus 1866 clock periods have elapsed.
2. If V_{DD} has a slow rise time then the RESET signal should be stretched by an external RC circuit (see Fig. 23 and 24). In the event of a short drop in the supply voltage, the diode path rapidly discharges the capacitor to ensure a reliable power-on reset. To ensure a correct reset, the RESET signal should reach at least 70% of the final value of V_{DD}. Given that the RESET voltage and V_{DD} rise exponentially, the above requirement is satisfied when the time constant τ of the RESET pulse is >8 times the time constant of V_{DD}. If V_{DD} rises linearly, then a RESET time constant >2 times the rise time of V_{DD} is required.

   When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods have elapsed (see Fig. 24). If the oscillator is started-up prior to the completion of RESET, then program execution begins 1866 clock periods after RESET goes LOW.
3. Figure 25 shows an external reset to the PCF84C430 during power-on. The external reset signal must remain HIGH until V_{DD} has reached its minimum operating value corresponding to the selected oscillator frequency. When a reset is completed (RESET goes LOW) before the oscillator has started up, program execution begins after the oscillator start-up time plus 1866 clock periods have elapsed (see Fig. 26). If the oscillator is started-up prior to the completion of RESET, then program execution begins 1866 clock periods after RESET goes LOW.

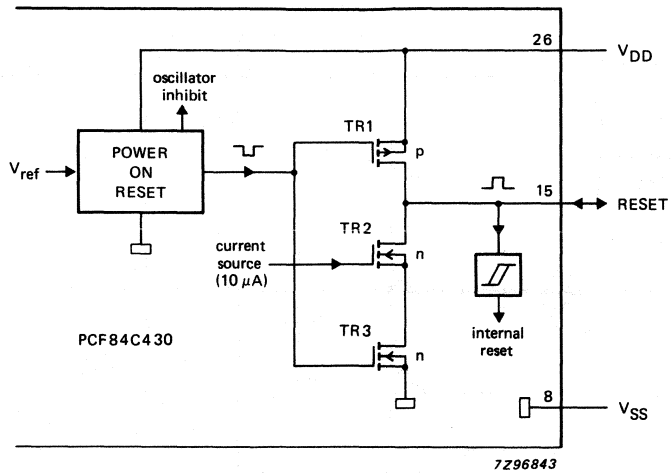


Fig. 21 Power-on-reset configuration.

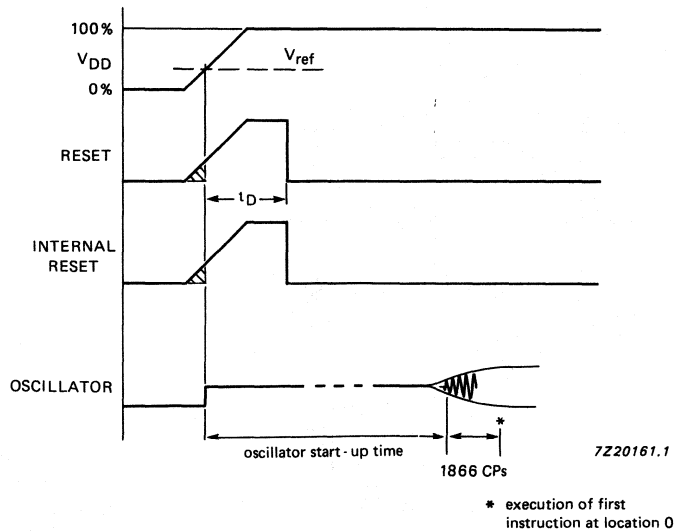


Fig. 22 Timing of power-on-reset with fast rise time.

FUNCTIONAL DESCRIPTION (continued)

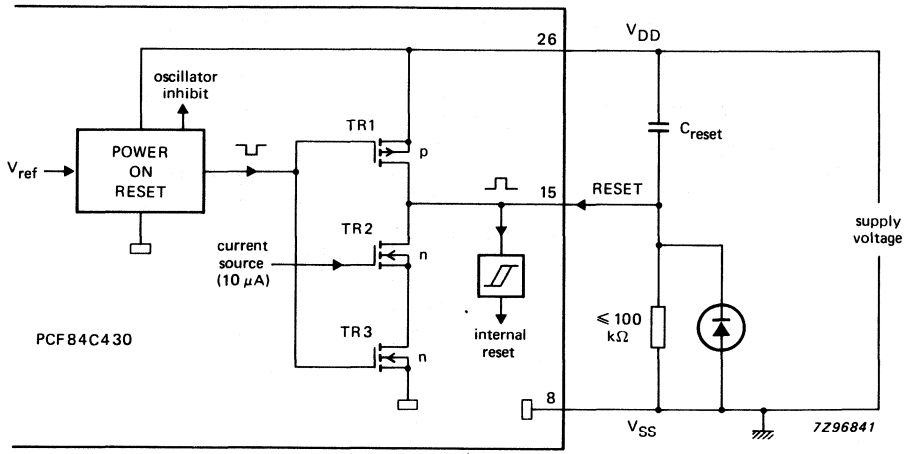


Fig. 23 Stretched power-on-reset with external components.

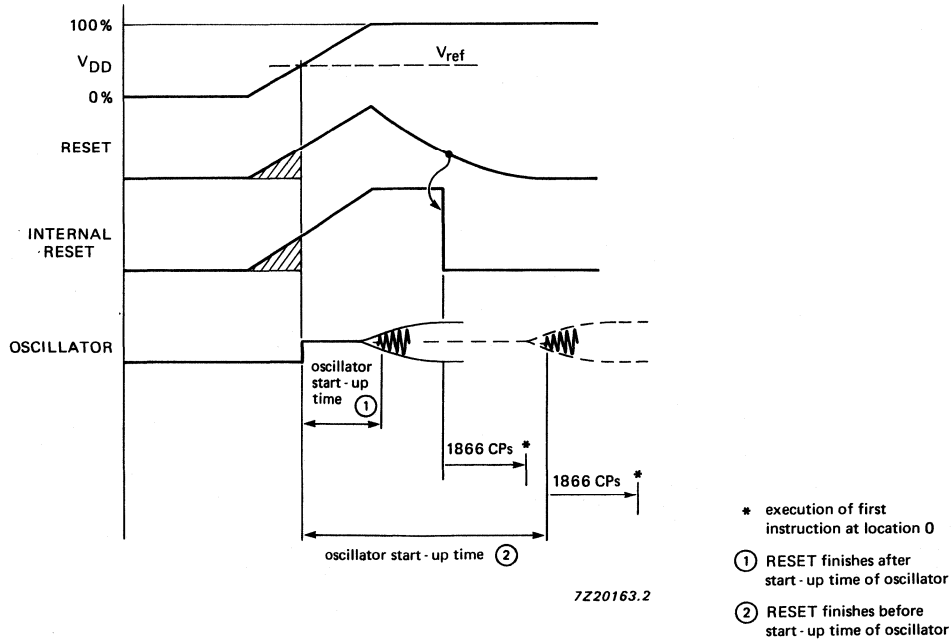


Fig. 24 Timing of power-on-reset with a slowly rising V_{DD} and a stretched RESET pulse.

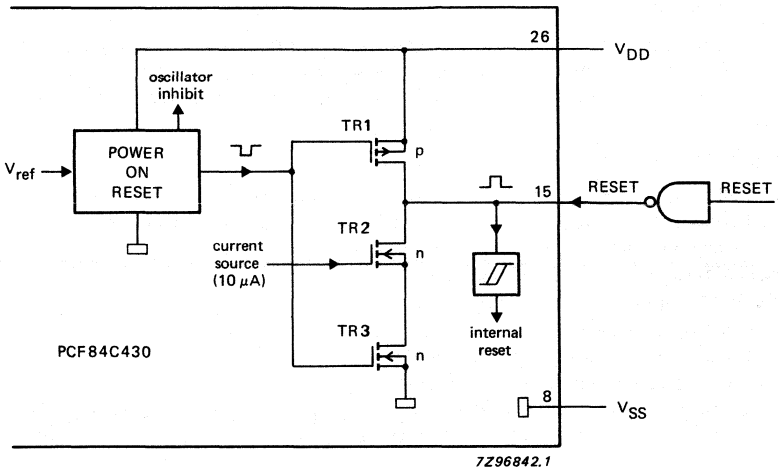


Fig. 25 External power-on-reset configuration.

DEVELOPMENT DATA

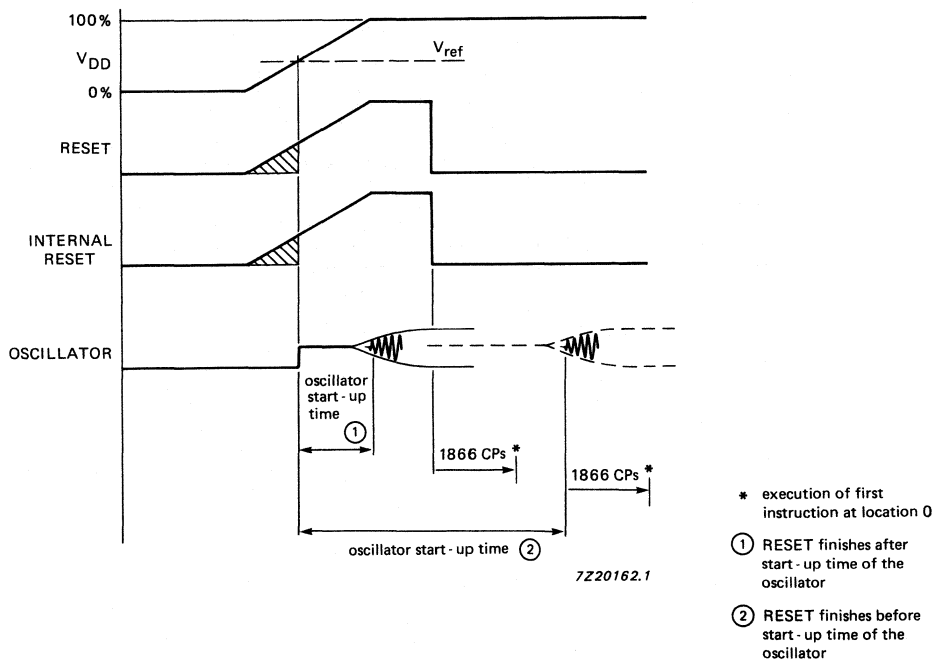


Fig. 26 Timing of external power-on-reset.

FUNCTIONAL DESCRIPTION (continued)

Liquid crystal display driver

The PCF84C430 has a display driver which interfaces to almost any liquid crystal display (LCD) which has a low multiplex rate. The interface delivers drive signals for any static or multiplexed LCD panel that contains up to four backplanes and up to 24 segments. Fig. 27 shows a block diagram of the LCD driver.

The following features are incorporated:

- Selectable backplane drive configuration; static or 2/3/4 backplane multiplexing
- Selectable display bias configuration; 1/2 or 1/3 internal LCD bias generation
- 24 individual segment drivers can be used to provide
  - up to twelve 8-segment numeric characters
  - up to six 15+1 segment alphanumeric characters
  - graphics using up to 96 elements
  - twelve 8-bit derivative registers for display data bits
- LCD and logic voltage supplies may be separated
- An LCD operating voltage range of between V_{SS} to V_{DD} −2,5 V ($V_{SS} \leqslant V_{LCD} < V_{DD}$)
- A low-power zero-component oscillator keeps the LCD display running in the STOP mode

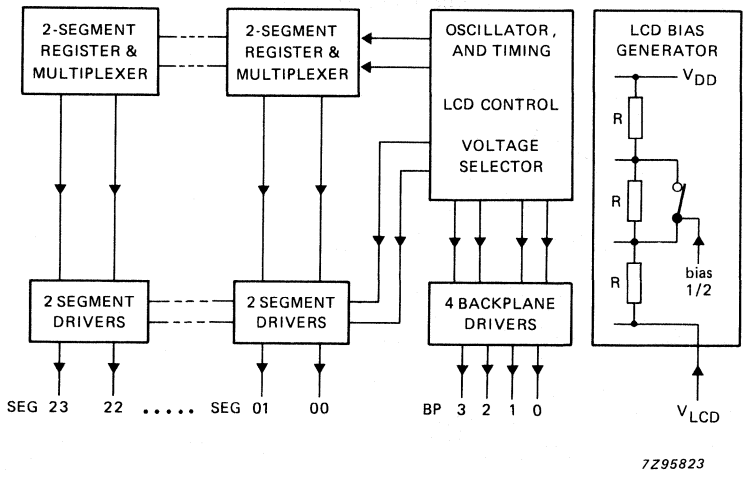


Fig. 27 Block diagram of the LCD driver.

The display configurations possible with the PCF84C430 depend upon the number of active backplane outputs required. A selection of display configurations is given in Table 6.

Table 6 Selection of display configurations

number of backplanes	number of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	96	12 digits + 12 indicator symbols	6 characters + 12 indicator symbols	96 dots (4 x 24)
3	72	9 digits + 9 indicator symbols	5 characters + 2 indicator symbols	72 dots (3 x 24)
2	48	6 digits + 6 indicator symbols	3 characters + 6 indicator symbols	48 dots (2 x 24)
1	24	3 digits + 3 indicator symbols	1 character + 10 indicator symbols	24 dots (1 x 24)

DEVELOPMENT DATA

All of the display configurations given in Table 6 can be implemented in the typical system shown in Fig. 28. The appropriate biasing voltages for the multiplexed LCD wave forms are generated internally.

At power-on all the LCD driver control register bits are cleared. The LCD display is not affected by executing a STOP instruction.

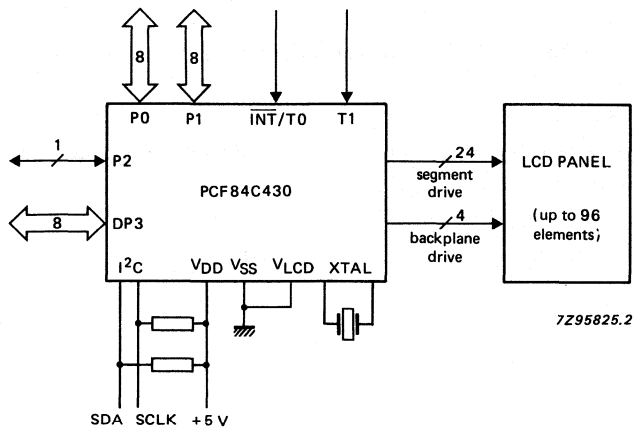


Fig. 28 Typical system configuration.

FUNCTIONAL DESCRIPTION (continued)

LCD bias generation

The LCD operating voltage (V_{op}) is the result of V_{DD} - V_{LCD}. V_{op} should be chosen so that the off voltage ($V_{off(rms)}$) is just below the threshold voltage (V_{th}), typically when the LCD exhibits 10% contrast. The LCD voltage may be temperature compensated externally through the LCD supply. Fractional LCD biasing voltages are obtained from an internal voltage divider of three resistors connected between V_{DD} and V_{LCD}. The centre resistor may be switched out of circuit to provide a ½ bias voltage level for a 1:2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected drive configuration. The operation of the voltage selector is controlled by the MODE bits in the LCD control byte. The biasing configurations that apply to the preferred mode of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and resulting discrimination ratios (D), are given in Table 7.

Table 7 LCD drive modes and characteristics

LCD drive mode	number of backplanes	LCD bias configuration	number of levels	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on(rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static	1	static	2	0	1	∞
1:2	2	1/2	3	0,354	0,791	2,236
1:2	2	1/3	4	0,333	0,745	2,236
1:3	3	1/3	4	0,333	0,638	1,915
1:4	4	1/3	4	0,333	0,577	1,7321

Multiplex drive ratios of 1:3 and 1:4 with ½ bias are possible, but the discrimination and contrast ratios are reduced thus;

(1,732 for 1:3 or 1,528 for 1:4)

There is an advantage however, that these modes lead to a reduction in V_{op} as follows:

1:3 multiplex (½ bias). $V_{op} = 2{,}449\ V_{off(rms)}$

1:4 multiplex (½ bias). $V_{op} = 2{,}309\ V_{off(rms)}$

This compares with $V_{op} = 3\ V_{off(rms)}$ when 1/3 bias is used.

LCD driver (continued)

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms are shown in Fig. 29.

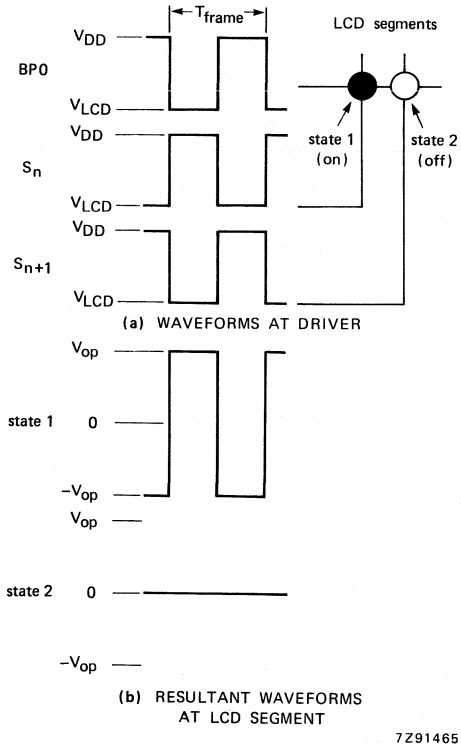


Fig. 29 Static drive mode waveforms.

FUNCTIONAL DESCRIPTION (continued)

When two backplanes are provided in the LCD; the 1:2 multiplex drive mode applies. The PCF84C430 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 30 and 31.

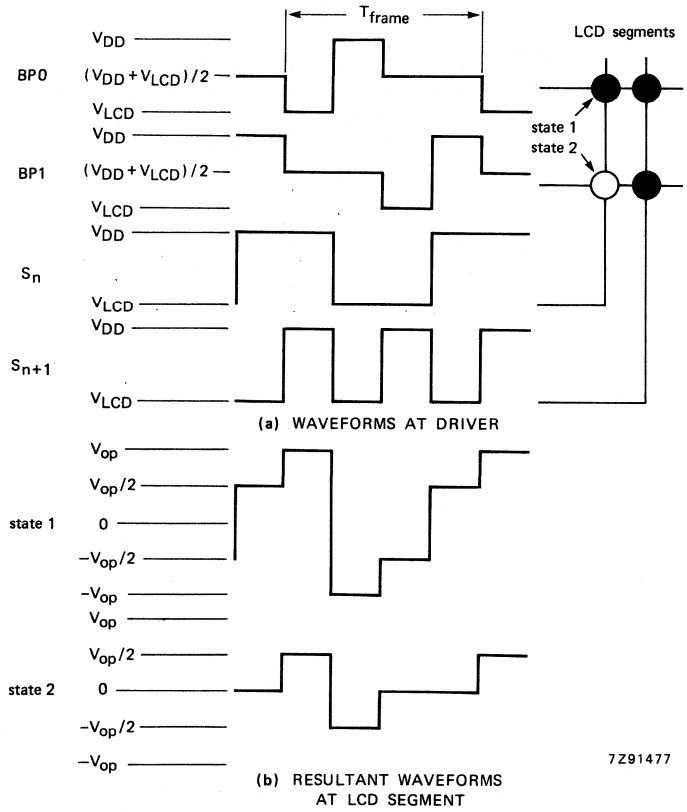


Fig. 30 Waveforms for the 1:2 multiplex drive mode with 1/2 bias.

LCD driver (continued)

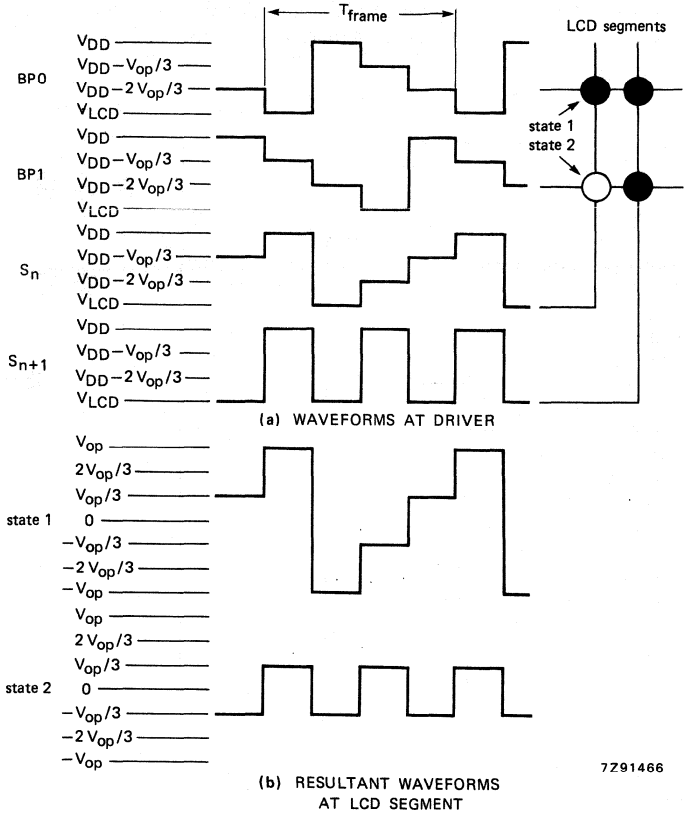


Fig. 31 Waveforms for the 1:2 multiplex drive mode with 1/3 bias.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

The backplane and segment drive waveforms for the 1:3 multiplex drive mode (three LCD backplanes) and for the 1:4 multiplex drive mode (four LCD backplanes) are shown in Figs 32 and 33 respectively.

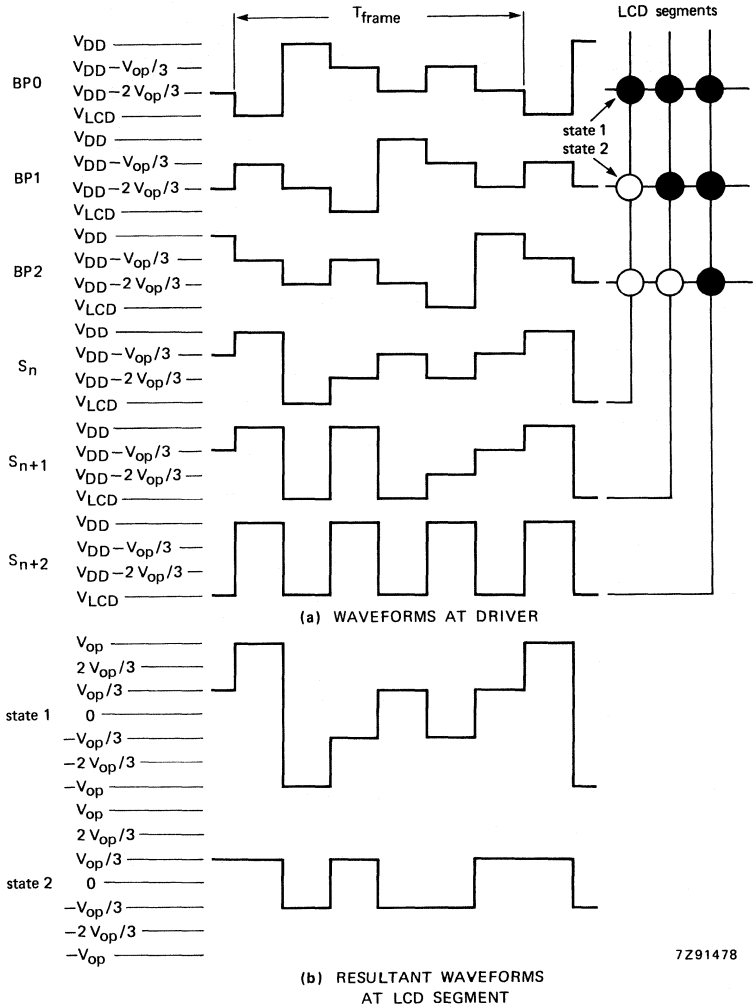


Fig. 32 Waveforms for the 1:3 multiplex drive mode.

LCD driver (continued)

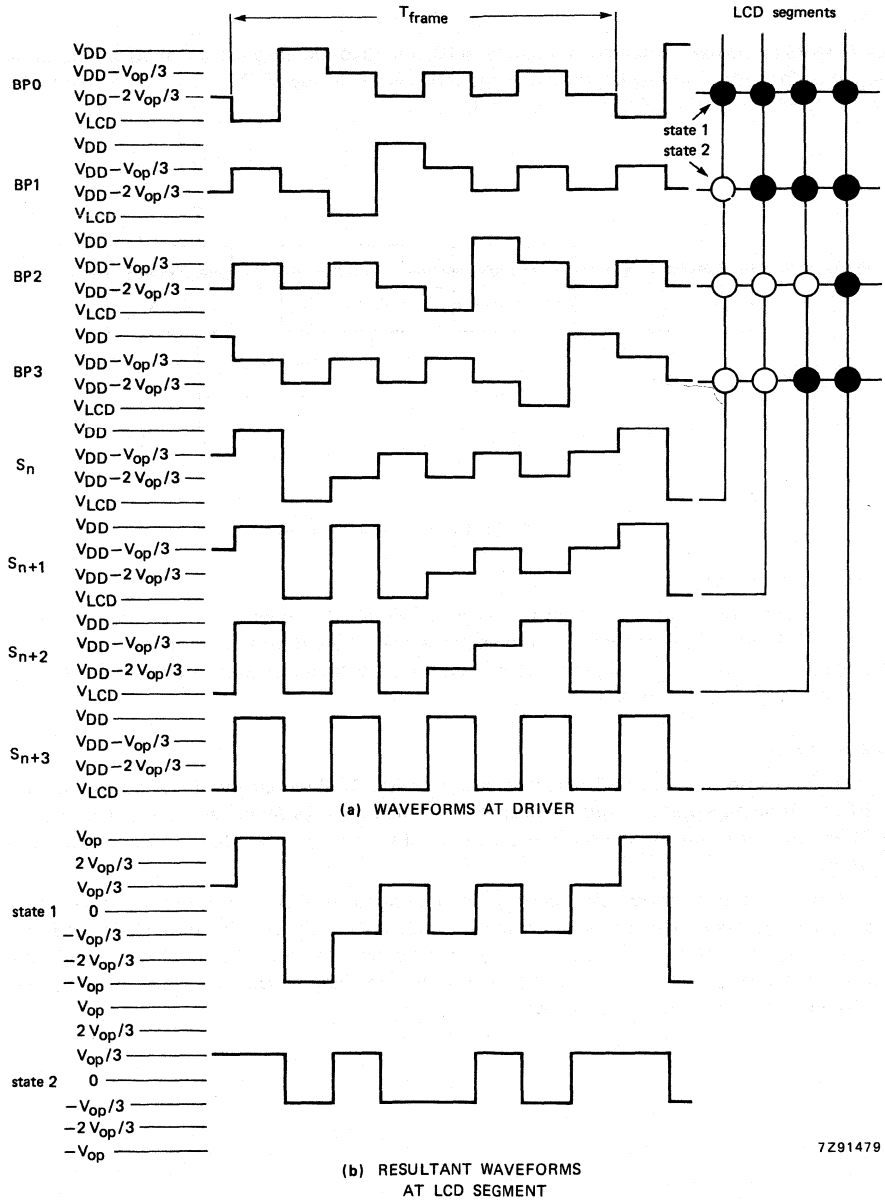


Fig. 33 Waveforms for the 1:4 multiplex drive mode.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

LCD timing

The LCD clocking is performed by a separate, self-contained, on-chip oscillator with a nominal frequency of 30 kHz. The display may be kept active while in the STOP mode using a very low supply current. Fig. 34 shows the LCD timing control.

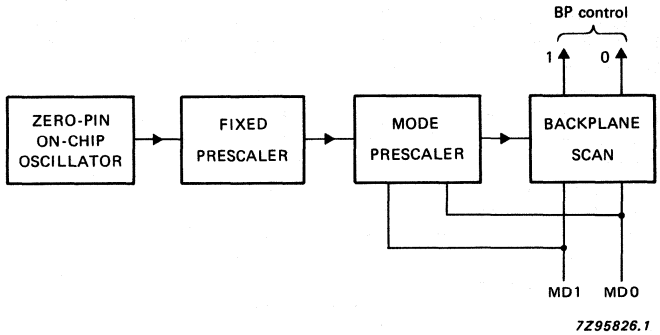


Fig. 34 LCD timing control.

LCD segment driver outputs

The LCD drive section includes 24 segment outputs (S0 to S23) which should be connected directly to the LCD. The segment data bits (one nibble per segment) are multiplexed to the outputs in accordance with the backplane signals. If less than the 24 segment outputs are required then the unused driver outputs should be left open.

Backplane outputs

The LCD drive section includes 4 backplane outputs (BP0-BP3) which should be connected directly to the LCD. These backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required then the unused driver outputs should be left open-circuit.

In the 1:3 multiplex drive mode, BP3 carries the same signal as BP0, therefore these two outputs can be tied together to give enhanced drive capabilities. In the 1:2 multiplex drive mode, BP0 and BP3, BP1 and BP2 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and may be connected in parallel to give a very high drive capability.

LCD driver (continued)

LCD segment display registers

The 12 segment display registers are 8-bit derivative (read/write) registers which store LCD segment data. A segment register bit which is set to a logic 1 indicates the 'on' state of the corresponding LCD segment, similarly, a logic 0 indicates the 'off' state. There is a one-to-one relationship between the LCD segment register bits and the segment outputs. Every byte is divided into two nibbles. Each nibble corresponds to a segment driver; the first byte contains the bits earmarked for segment 1 and 2 etc. The first bit of a nibble will correspond to backplane 0, and the second to backplane 1 and so on. Fig. 35 shows the display register bit map. Each bit is shown in the form Sxx.n, where (xx) is the segment output and (n) the backplane output.

LCDD : LCD display data

17	R/W	S 0.0	S 0.1	S 0.2	S 0.3	S 1.0	S 1.1	S 1.2	S 1.3
18	R/W	S 2.0	S 2.1	S 2.2	S 2.3	S 3.0	S 3.1	S 3.2	S 3.3
19	R/W	S 4.0	S 4.1	S 4.2	S 4.3	S 5.0	S 5.1	S 5.2	S 5.3
20	R/W	S 6.0	S 6.1	S 6.2	S 6.3	S 7.0	S 7.1	S 7.2	S 7.3
21	R/W	S 8.0	S 8.1	S 8.2	S 8.3	S 9.0	S 9.1	S 9.2	S 9.3
22	R/W	S10.0	S10.1	S10.2	S10.3	S11.0	S11.1	S11.2	S11.3
23	R/W	S12.0	S12.1	S12.2	S12.3	S13.0	S13.1	S13.2	S13.3
24	R/W	S14.0	S14.1	S14.2	S14.3	S15.0	S15.1	S15.2	S15.3
25	R/W	S16.0	S16.1	S16.2	S16.3	S17.0	S17.1	S17.2	S17.3
26	R/W	S18.0	S18.1	S18.2	S18.3	S19.0	S19.1	S19.2	S19.3
27	R/W	S20.0	S20.1	S20.2	S20.3	S21.0	S21.1	S21.2	S21.3
28	R/W	S22.0	S22.1	S22.2	S22.3	S23.0	S23.1	S23.2	S23.3

Fig. 35 Display register bit map.

In the static drive mode the eight display data bits are placed in bit 0 of the nibbles of four successive derivative display registers. In the 1:2 multiplex drive mode, these eight bits are placed in bits 0 and 1 of the nibbles of two successive registers. In the 1:3 multplex drive mode the eight bits are placed in

FUNCTIONAL DESCRIPTION (continued)

bits 0, 1 and 2 of three successive nibbles. In the 1:4 multiplex drive mode the eight bits are placed in bits 0, 1, 2 and 3 of the nibbles of the first display register. Fig. 36 shows the relationship between LCD segment layout, drive mode and the LCD segment derivative register bit pattern.

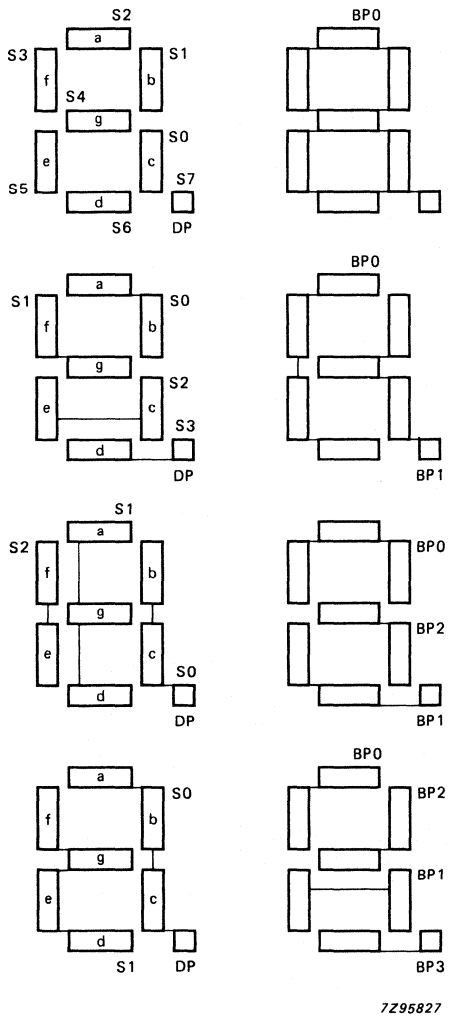


Fig. 36 LCD segment layout and register bit pattern.

LCD derivative register bit map

byte

17	c	–	–	–	b	–	–	–
18	a	–	–	–	f	–	–	–
19	g	–	–	–	e	–	–	–
20	d	–	–	–	Dp	–	–	–

static mode

byte

17	a	b	–	–	f	g	–	–
18	e	c	–	–	d	Dp	–	–
19	–	–	–	–	–	–	–	–
20	–	–	–	–	–	–	–	–

1:2 multiplex mode

byte

17	b	Dp	c	–	a	d	g	–
18	f	e	–	–	–	–	–	–
19	–	–	–	–	–	–	–	–
20	–	–	–	–	–	–	–	–

1:3 multiplex mode

byte

17	a	c	b	Dp	f	e	g	d
18	–	–	–	–	–	–	–	–
19	–	–	–	–	–	–	–	–
20	–	–	–	–	–	–	–	–

1:4 multiplex mode

LCD driver (continued)

LCD control register

The LCD operating mode is governed by four bits of the LCD control register (address 16 D). The LCD control register is an 8-bit derivative read/write register. The function of each bit is given in Table 8.

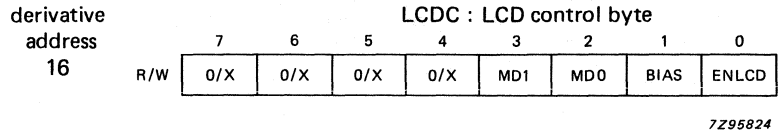


Table 8 Control register bit definition

bit	name	function		
0	ENLCD	0 = LCD display disabled 1 = LCD display enabled		
1	BIAS	0 = 1/3 V_{DD} 1 = 1/2 V_{DD}		
2, 3	MD0/MD1	MD1	MD0	multiplex mode
		0 0 1 1	0 1 0 1	static 1:2 1:3 1:4
4-7	unused			

ENLCD: When ENLCD is reset to 0, the LCD is disabled. Consequently all segment and backplane drivers are set to the V_{DD} level. When ENLCD is set to a 1, the LCD is enabled and character display is possible.

BIAS: The BIAS bit sets the LCD voltage bias generator to either 1/2 or 1/3 of V_{DD}, see Fig. 27.

MD0/MD1: Mode bits MD0 and MD1 determine the multiplex rate. Four multiplex rates are available; static, 1:2, 1:3 and 1:4.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

LCD control byte after RESET

After an external or power-on reset the LCD control register is set with 0C H.

	7	6	5	4	3	2	1	0
	0/X	0/X	0/X	0/X	MD1	MD0	BIAS	ENLCD
reset value	0	0	0	0	1	1	0	0

7Z97990

- The LCD is disabled and segment and backplane drives are switched to the V_{DD} level.
- BIAS is set to generate 1/3 V_{DD}.
- Bits MD0 and MD1 reset the multiplex mode to the 1:4 mode.

INSTRUCTION SET

The PCF84C430 instruction set consists of over 80 one and two byte instructions. Program code efficiency is high because all RAM locations and all ROM locations on a 256 byte page require only a single byte address.

Table 11 gives the instruction set of the PCF84C430. Table 10 shows the instruction map and Table 9 details the symbols and definition descriptions that are used.

Table 9 Symbols and definitions used in Table 11

symbol	definition description
A	accumulator
addr	program memory address
Bb	bit designation (b = 0-7)
RBS	register bank select
C	carry bit (bit CY)
CNT	event counter
Dx	Derivative register designation (x = 4,5,16,17-28)
data	8-bit number or expression
I	interrupt
MB	memory bank
MBFF	memory bank flip-flop
P	mnemonic for 'in-page' operation
PC	program counter
Pp	port designation (p = 0, 1 or 2)
PSW	program status word
RB	register bank
Rr	register designation (r = 0-7)
Sn	serial I/O register
SP	stack pointer
T	timer
TF	timer flag
T0, T1	test 0 and 1 inputs
#	immediate data prefix
@	indirect address prefix
(X)	contents of X
((X))	contents of location addressed by X
←	is replaced by
↔	is exchanged with

INSTRUCTION SET (continued)

Table 10 PCF84C430 instruction map

first hexadecimal character of opcode

second hexadecimal character of opcode

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	IDLE		ADD A,#data	JMP page 0	EN I	JNTF addr	DEC A	IN A,Pp 0 1 2				MOV A,Sn 0	1		
1	INC @Rr 0 1		JB0 addr	ADDC A,#data	CALL page 0	DIS I	JTF addr	INC A	INC Rr 0 1 2 3 4 5 6 7							
2	XCH A,@Rr 0 1		STOP	MOV A,#data	JMP page 1	EN TCNTI	JNTO addr	CLR A	XCH A,Rr 0 1 2 3 4 5 6 7							
3	XCHD A,@Rr 0 1		JB1 addr		CALL page 1	DIS TCNTI	JTO addr	CPL A	OUTL Pp,A 0 1 2				MOV Sn,A 0	1	2	
4	ORL A,@Rr 0 1		MOV A,T	ORL A,#data	JMP page 2	STRT CNT	JNT1 addr	SWAP A	ORL A,Rr 0 1 2 3 4 5 6 7							
5	ANL A,@Rr 0 1		JB2 addr	ANL A,#data	CALL page 2	STRT T	JT1 addr	DA A	ANL A,Rr 0 1 2 3 4 5 6 7							
6	ADD A,@Rr 0 1		MOV T,A		JMP page 3	STOP TCNT		RRC A	ADD A,Rr 0 1 2 3 4 5 6 7							
7	ADDC A,@Rr 0 1		JB3 addr		CALL page 3			RR A	ADDC A,Rr 0 1 2 3 4 5 6 7							
8				RET	JMP page 4	EN SI			ORL Pp,#data 0 1 2				MOV A,Dx	MOV Dx,A	ANL Dx,A	ORL Dx,A
9			JB4 addr	RETR	CALL page 4	DIS SI	JNZ addr	CLR C	ANL Pp,#data 0 1 2				MOV Sn,#data 0	1	2	
A	MOV @Rr,A 0 1			MOVP A,@A	JMP page 5			CPL C	MOV Rr,A 0 1 2 3 4 5 6 7							
B	MOV @Rr,#data 0 1		JB5 addr	JMPP @A	CALL page 5				MOV Rr,#data 0 1 2 3 4 5 6 7							
C	DEC @Rr 0 1				JMP page 6	SEL RB0	JZ addr	MOV A,PSW	DEC Rr 0 1 2 3 4 5 6 7							
D	XRL A,@Rr 0 1		JB6 addr	XRL A,#data	CALL page 6	SEL RB1		MOV PSW,A	XRL A,Rr 0 1 2 3 4 5 6 7							
E	DJNZ @Rr,addr 0 1				JMP page 7	SEL MB0	JNC addr	RL A	DJNZ Rr, addr 0 1 2 3 4 5 6 7							
F	MOV A,@Rr 0 1		JB7 addr		CALL page 7	SEL MB1	JC addr	RLC A	MOV A,Rr 0 1 2 3 4 5 6 7							

Table 11 Instruction set

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
ACCUMULATOR	ADD A, Rr	6*	1/1	Add register contents to A	(A)←(A) + (Rr)	r = 0–7	1
	ADD A, @Rr	60 61	1/1	Add RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) (A)←(A) + ((R1))		1
	ADD A, #data	03 data	2/2	Add immediate data to A	(A)←(A) + data		1
	ADDC A, Rr	7*	1/1	Add carry and register contents to A	(A)←(A) + (Rr) + (C)	r = 0–7	1
	ADDC A, @Rr	70 71	1/1	Add carry and RAM data, addressed by Rr, to A	(A)←(A) + ((R0)) + (C) (A)←(A) + ((R1)) + (C)		1
	ADDC A, #data	13 data	2/2	Add carry and immediate data to A	(A)←(A) + data + (C)		1
	ANL A, Rr	5*	1/1	'AND' Rr with A	(A)←(A) AND (Rr)	r = 0–7	
	ANL A, @Rr	50 51	1/1	'AND' RAM data, addressed by Rr, with A	(A)←(A) AND ((R0)) (A)←(A) AND ((R1))		
	ANL A, #data	53 data	2/2	'AND' immediate data with A	(A)←(A) AND data		
	ORL A, Rr	4*	1/1	'OR' Rr with A	(A)←(A) OR (Rr)	r = 0–7	
	ORL A, @Rr	40 41	1/1	'OR' RAM data, addressed by Rr, with A	(A)←(A) OR ((R0)) (A)←(A) OR ((R1))		
	ORL A, #data	43 data	2/2	'OR' immediate data with A	(A)←(A) OR data		
	XRL A, Rr	D*	1/1	'XOR' Rr with A	(A)←(A) XOR (Rr)	r = 0–7	
	XRL A, @Rr	D0 D1	1/1	'XOR' RAM, addressed by Rr, with A	(A)←(A) XOR ((R0)) (A)←(A) XOR ((R1))		
	XRL A, #data	D3 data	2/2	'XOR' immediate data with A	(A)←(A) XOR data		
	INC A	17	1/1	increment A by 1	(A)←(A) + 1		
	DEC A	07	1/1	decrement A by 1	(A)←(A) −1		
	CLR A	27	1/1	clear A to zero	(A)←0		
	CPL A	37	1/1	one's complement A	(A)←NOT(A)		
	RL A	E7	1/1	rotate A left	$(A_{n+1})\leftarrow(A_n)$ $(A_0)\leftarrow(A_7)$	n = 0–6	

INSTRUCTION SET (continued)

ACCUMULATOR (cont.)	RLC A	F7	1/1	rotate A left through carry	$(A_{n+1})\leftarrow A_n$ $(A_0)\leftarrow(C)$, $(C)\leftarrow(A_7)$	n = 0–6	2
	RR A	77	1/1	rotate A right	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(A_0)$	n = 0–6	
	RRC A	67	1/1	rotate A right through carry	$(A_n)\leftarrow(A_{n+1})$ $(A_7)\leftarrow(C)$, $(C)\leftarrow(A_0)$	n = 0–6	2
	DA A	57	1/1	decimal adjust A			2
	SWAP A	47	1/1	swap nibbles of A	$(A_{4-7})\leftrightarrow(A_{0-3})$		
DATA MOVES	MOV A, Rr	F*	1/1	move register contents to A	(A)←(Rr)	r = 0–7	
	MOV A, @Rr	F0 F1	1/1	move RAM data, addressed by Rr, to A	(A)←((R0)) (A)←((R1))		
	MOV A, #data	23 data	2/2	move immediate data to A	(A)←data		
	MOV Rr, A	A*	1/1	move accumulator contents to register	(Rr)←(A)	r = 0–7	
	MOV @Rr, A	A0 A1	1/1	move accumulator contents to RAM location addressed by Rr	((R0))←(A) ((R1))←(A)		
	MOV Rr, #data	B* data	2/2	move immediate data to Rr	(Rr)←data		
	MOV @Rr, #data	B0 data B1 data	2/2	move immediate data to RAM location addressed by Rr	((R0))←data ((R1))←data		
	XCH A, Rr	2*	1/1	exchange accumulator contents with Rr	(A)↔(Rr)	r = 0–7	
	XCH A, @Rr	20 21	1/1	exchange accumulator contents with RAM data addressed by Rr	(A)↔((R0)) (A)↔((R1))		
	XCHD A, @Rr	30 31	1/1	exchange lower nibbles of A and RAM data addressed by Rr	$(A_{0-3})\leftrightarrow((R0_{0-3}))$ $(A_{0-3})\leftrightarrow((R1_{0-3}))$		
	MOV A, PSW	C7	1/1	move PSW contents to accumulator	(A)←(PSW)		
	MOV PSW, A	D7	1/1	move accumulator bit 3 to PSW_3	$(PSW_3)\leftarrow(A_3)$		3
	MOVP A, @A	A3	1/2	move indirectly addressed data in current page to A	$(PC_{0-7})\leftarrow(A)$, (A)←((PC))		
FLAGS	CLR C	97	1/1	clear carry bit	(C)←0		2
	CPL C	A7	1/1	complement carry bit	(C)←NOT(C)		2

DEVELOPMENT DATA

	mnemonic	opcode (hex.)	bytes/ cycles	description	function		notes
REGISTER	INC Rr	1*	1/1	increment register by 1	(Rr)←(Rr) + 1	r = 0–7	
	INC @Rr	10 11	1/1	increment RAM data, addressed by Rr, by 1	((R0))←((R0)) + 1 ((R1))←((R1)) + 1		
	DEC Rr	C*	1/1	decrement register by 1	(Rr)←(Rr) – 1	r = 0–7	
	DEC @Rr	C0 C1	1/1	decrement RAM data, addressed by Rr, by 1	((R0))←((R0)) – 1 ((R1))←((R1)) – 1		
BRANCH	JMP addr	• 4 addr	2/2	unconditional jump within a 2 K bank	(PC_{8-10})←$addr_{8-10}$ (PC_{0-7})←$addr_{0-7}$ (PC_{11-12})←MBFF 0–1		
	JMPP @A	B3	1/2	indirect jump within a page	(PC_{0-7})←((A))		
	DJNZ Rr, addr	E* addr	2/2	decrement Rr by 1 and jump if not zero to addr	(Rr)←(Rr) – 1 if (Rr) not zero (PC_{0-7})←addr	r = 0–7	
	DJNZ @Rr, addr	E0 addr	2/2	decrement RAM data, addressed by Rr by 1 and jump if not zero to addr	((R0))←((R0)) – 1 if ((R0)) not zero (PC_{0-7})←addr		
		E1 addr			((R1))←((R1)) – 1 if ((R1)) not zero (PC_{0-7})←addr		
	JBb addr	▲ 2 addr	2/2	jump to addr if Acc. bit b = 1	if b = 1 : (PC_{0-7})←addr	b = 0–7	
	JC addr	F6 addr	2/2	jump to addr if C = 1	if C = 1 : (PC_{0-7})←addr		
	JNC addr	E6 addr	2/2	jump to addr if C = 0	if C = 0 : (PC_{0-7})←addr		
	JZ addr	C6 addr	2/2	jump to addr if A = 0	if A = 0 : (PC_{0-7})←addr		
	JNZ addr	96 addr	2/2	jump to addr if A is NOT zero	if A ≠ 0 : (PC_{0-7})←addr		
	JT0 addr	36 addr	2/2	jump to addr if T0 = 1	if T0 = 1: (PC_{0-7})←addr		
	JNT0 addr	26 addr	2/2	jump to addr if T0 = 0	if T0 = 0: (PC_{0-7})←addr		
	JT1 addr	56 addr	2/2	jump to addr if T1 = 1	if T1 = 1: (PC_{0-7})←addr		
	JNT1 addr	46 addr	2/2	jump to addr if T1 = 0	if T1 = 0: (PC_{0-7})←addr		
	JTF addr	16 addr	2/2	jump to addr if Timer Flag = 1	if TF = 1: (PC_{0-7})←addr		4
	JNTF addr	06 addr	2/2	jump to addr if Timer Flag = 0	if TF = 0: (PC_{0-7})←addr		

INSTRUCTION SET (continued)

TIMER/EVENT COUNTER	MOV A, T	42	1/1	move timer/event counter contents to accumulator	(A)←(T)	
	MOV T, A	62	1/1	move accumulator contents to timer/event counter	(T)←(A)	
	STRT CNT	45	1/1	start event counter		
	STRT T	55	1/1	start timer		
	STOP TCNT	65	1/1	stop timer/event counter		
	EN TCNTI	25	1/1	enable timer/event counter interrupt		
	DIS TCNTI	35	1/1	disable timer/event counter interrupt		
CONTROL	EN I	05	1/1	enable external interrupt		
	DIS I	15	1/1	disable external interrupt		
	SEL RB0	C5	1/1	select register bank 0	(RBS)←0	5
	SEL RB1	D5	1/1	select register bank 1	(RBS)←1	5
	SEL MB0	E5	1/1	select program memory bank 0	(MBFF0)←0, (MBFF1)←0	10
	SEL MB1	F5	1/1	select program memory bank 1	(MBFF0)←1, (MBFF1)←0	10
	STOP	22	1/1	enter STOP mode		
	IDLE	01	1/1	enter IDLE mode		
SUBROUTINE	CALL addr	▲ 4 addr	2/2	jump to subroutine	$((SP))\leftarrow(PC), (PSW_{4,6,7})$ 6 $(SP)\leftarrow(SP)+1$ $(PC_{8-10})\leftarrow addr_{8-10}$ $(PC_{0-7})\leftarrow addr_{0-7}$ $(PC_{11-12})\leftarrow$MBFF 0–1	6
	RET	83	1/2	return from subroutine	$(SP)\leftarrow(SP)-1$ $(PC)\leftarrow((SP))$	6
	RETR	93	1/2	return from interrupt and restore bits 4, 6, 7 of PSW	$(SP)\leftarrow(SP)-1$ $(PSW_{4,6,7}) + (PC)\leftarrow((SP))$	6

DEVELOPMENT DATA

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
PARALLEL INPUT/OUTPUT	IN A, Pp	08 09 0A	1/2	input port p data to accumulator	(A)←(P0) (A)←(P1) (A)←(P2)	7
	OUTL Pp, A	38 39 3A	1/2	output accumulator data to port p	(P0)←(A) (P1)←(A) (P2)←(A)	
	ANL Pp, #data	98 data 99 data 9A data	2/2	AND port p data with immediate data	(P0)←(P0) AND data (P1)←(P1) AND data (P2)←(P2) AND data	
	ORL Pp, #data	88 data 89 data 8A data	2/2	OR port p data with immediate data	(P0)←(P0) OR data (P1)←(P1) OR data (P2)←(P2) OR data	
DERIVATIVE INPUT/OUTPUT	MOV A, Dx	8C Dx	2/2	Move derivative register/port contents addressed by Dx to accumulator	(A)←(Dx) x = 4,5,16,17-28	8
	MOV Dx, A	8D Dx	2/2	Move contents of accumulator to derivative register addressed by Dx	(Dx)←(A) x = 4,16,17-28	8
	ANL Dx, A	8E Dx	2/2	AND contents of accumulator with derivative register addressed by Dx	(Dx)←(Dx) AND (A) x = 4,16,17-28	8
	ORL Dx, A	8F Dx	2/2	OR contents of accumulator with derivative register addressed by Dx	(Dx)←(Dx) OR (A) x = 4,16,17-28	8

INSTRUCTION SET (continued)

	mnemonic	opcode (hex.)	bytes/ cycles	description	function	notes
SERIAL INPUT/OUTPUT	MOV A, S_n	0C 0D	1/2	move serial I/O register contents to accumulator	(A)←(S0) (A)←(S1)	9
	MOV S_n, A	3C 3D 3E	1/2	move accumulator contents to serial I/O register	(S0)←(A) (S1)←(A) (S2)←(A)	
	MOV S_n, #data	9C data 9D data 9E data	2/2	move immediate data to serial I/O register	(S0)←data (S1)←data (S2)←data	
	EN SI	85	1/1	enable serial I/O interrupt		
	DIS SI	95	1/1	disable serial I/O interrupt		
	NOP	00	1/1	no operation		

Notes to Table 8

1. PSW CY, AC affected
2. PSW CY affected
3 PSW PS affected
4. Execution of JTF and JNTF instructions resets the Timer Flag (TF).

* : 8,9,A,B,C,D,E,F
● : 0,2,4,6,8,A,C,E
▲ : 0,3,5,7,9,B,D,F

5. PSW RBS affected
6. PSW SP_0, SP_1, SP_2 affected
7. (A) = 0000 (P23) 111
8. Dx = 04, 05, 16, 17-28
9. (S1) has a different function in read and write operations, see serial I/O interface.
10. SEL MB0 and SEL MB1 must not be used within interrupt routines.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 26)	V_{DD}	−0,8	+ 8	V
All input voltages	V_I	−0,8	V_{DD} + 0,8	V
DC current into input or output	$\pm I_I \pm I_O$	–	10	mA
Power dissipation per output	P_O	–	50	mW
Storage temperature	T_{stg}	−65	+ 150	°C
Ambient operating temperature range (if $P_{totmax.}$ = 100 mW)	T_{amb}	−40	+ 70	°C
Ambient operating temperature range (if $P_{totmax.}$ = 30 mW)	T_{amb}	−40	+ 85	°C
Operating junction temperature	T_j	–	90	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DEVELOPMENT DATA

LCD DRIVER CHARACTERISTICS

V_{DD} = 2,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C. All voltages with respect to V_{SS} unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
LCD supply voltage (note 1)	V_{LCD}	V_{SS}	–	$V_{DD}-2,5$	V
DC voltage component (BP0 to BP3) at V_{DD} = 5 V	$+/-V_{BP}$	0	20	–	mV
DC voltage component (S0 to S23) at V_{DD} = 5 V	$+/-V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{SS}$ (note 2)	R_{BP}	–	–	5	kΩ
Output impedance (S0 to S23) at $V_{LCD} = V_{SS}$ (note 2)	R_S	–	–	7,0	kΩ
Driver delays with test loads at $V_{LCD} = V_{SS}$, I_{OS} = 15 μA, I_{OB} = 25 μA	tp_{LCD}	–	–	30	μs
LCD scan frame frequency	f_{LCD}	–	60	–	Hz

Notes to the LCD driver characteristics

1. $V_{LCD} < V_{DD}-3$ V for 1/3 bias.
2. Outputs measured one at a time.

DC CHARACTERISTICS

V_{DD} = 2,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C; all voltages with respect to V_{SS}; unless otherwise specified.

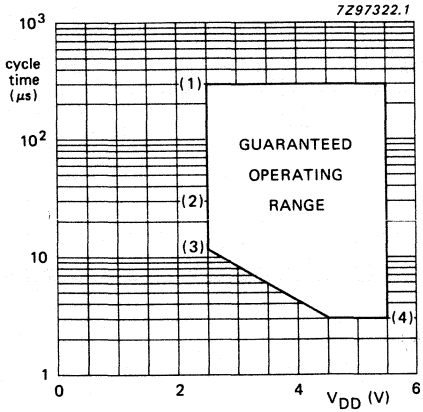
parameter	symbol	min.	typ.	max.	unit
Supply voltage					
operating (see Fig. 37)	V_{DD}	2,5	–	5,5	V
Supply current (note 1)					
operating mode (see Figs 41 and 42)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	2,2	4,5	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	1,3	2,6	mA
at V_{DD} = 3 V; f_{XTAL} = 3,58 MHz	I_{DD}	–	0,4	0,8	mA
IDLE mode (see Figs 39 and 40)					
at V_{DD} = 5 V; f_{XTAL} = 10 MHz	I_{DD}	–	0,8	1,6	mA
at V_{DD} = 5 V; f_{XTAL} = 6 MHz	I_{DD}	–	0,5	1	mA
at V_{DD} = 3 V; f_{XTAL} = 3,58 MHz	I_{DD}	–	0,15	0,4	mA
STOP mode (see Fig.38 and note 2)					
at V_{DD} = 2,5 V	I_{DD}	–	26	60	μA
at V_{DD} = 5 V	I_{DD}	–	30	80	μA
Inputs					
Input voltage LOW	V_{IL}	0	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD}	V
Input leakage current					
at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	–	–	1	μA
Outputs					
Output sink current LOW					
at V_{DD} = 5 V ± 10%; V_O = 0,4 V					
except P2.3/SDA, SCLK (see Fig.43)	I_{OL}	1,6	3	–	mA
P2.3/SDA, SCLK (see Fig.44)	I_{OL}	3	–	–	mA
Pull-up output source current HIGH (see Fig.45)					
at V_{DD} = 5 V ± 10%; V_O = $0{,}7V_{DD}$	$-I_{OH}$	40	–	–	μA
at V_{DD} = 5 V ± 10%; V_O = V_{SS}	$-I_{OH}$	–	–	400	μA
Push-pull output source current HIGH					
at V_{DD} = 5 V ± 10%; V_O = V_{DD}−0,4 V	$-I_{OH}$	1,6	3	–	mA

Notes to the DC characteristics

1. V_{IL} = V_{SS}, V_{IH} = V_{DD}; all outputs unloaded; all open drain outputs connected to V_{SS}.
2. Crystal connected between XTAL 1 and XTAL 2; SCLK and SDA pulled to V_{DD} via a 5,6 kΩ resistor; T1 at V_{SS}, $\overline{INT}$ at V_{DD}.

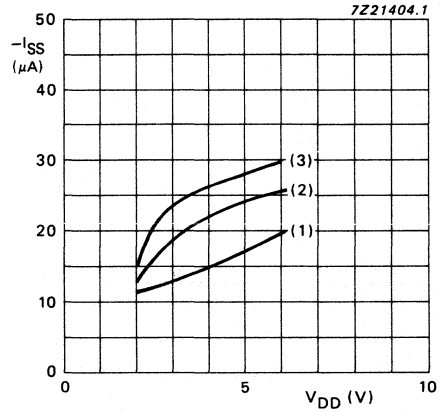
DEVELOPMENT DATA

AC CHARACTERISTICS



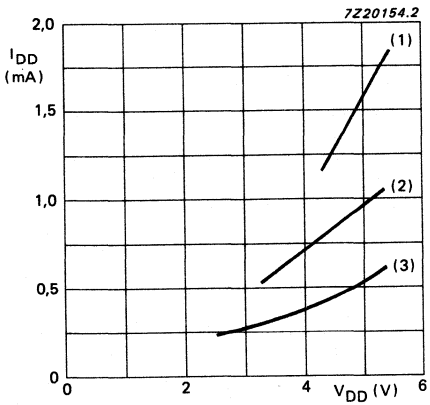
(1) clock frequency = 100 kHz
(2) clock frequency = 1 MHz
(3) clock frequency = 3 MHz
(4) clock frequency = 10 MHz

Fig. 37 Maximum clock frequency (f_{XTAL}) as a function of the supply voltage (V_{DD}).



$f_{CLK} \triangleq 30$ kHz (1) $T_{amb} = +85$ °C
(2) $T_{amb} = +25$ °C
(3) $T_{amb} = -40$ °C

Fig. 38 Typical supply current ($-I_{SS}$) in STOP mode as a function of the supply voltage (V_{DD}).



(1) clock frequency = 10 MHz
(2) clock frequency = 6 MHz
(3) clock frequency = 3,58 MHz

Fig. 39 Maximum supply current (I_{DD}) in IDLE mode as a function of the supply voltage (V_{DD}).

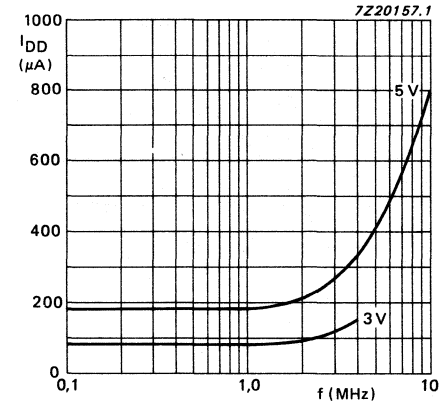
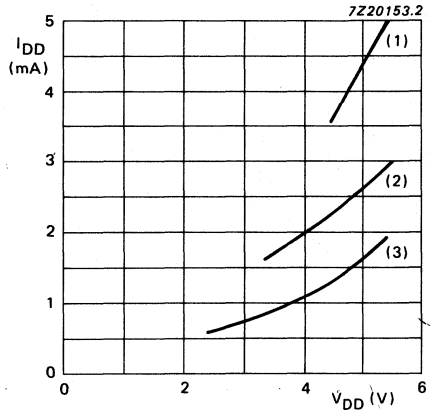


Fig. 40 Typical supply current during IDLE mode as a function of frequency at $V_{DD} = 3$ V and $V_{DD} = 5$ V.

AC CHARACTERISTICS (continued)



(1) clock frequency = 10 MHz
(2) clock frequency = 6 MHz
(3) clock frequency = 3,58 MHz

Fig. 41 Maximum supply current (I_{DD}) in operating mode as a function of the supply voltage.

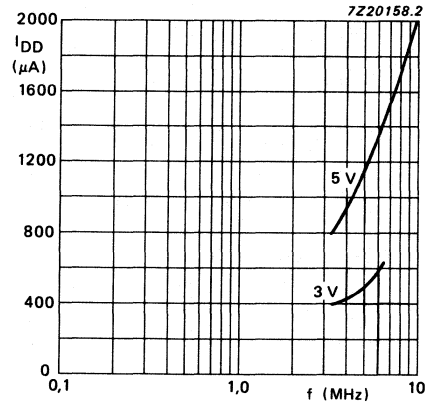


Fig. 42 Typical supply current during operating mode as a function of frequency at V_{DD} = 3 V and V_{DD} = 5 V.

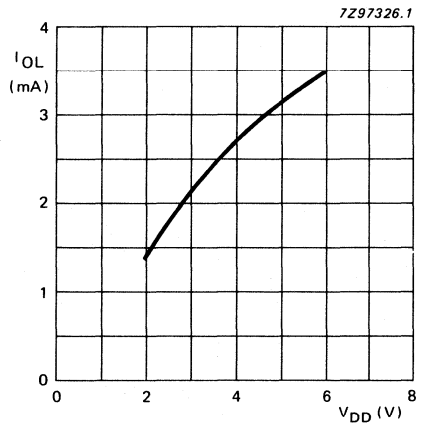


Fig. 43 Typical output sink current (I_{OL}), outputs P0.0 to P0.7, P1.0 to P1.7, DP3.0 to DP3.7, as a function of the supply voltage (V_{DD}); V_O = 0,4 V.

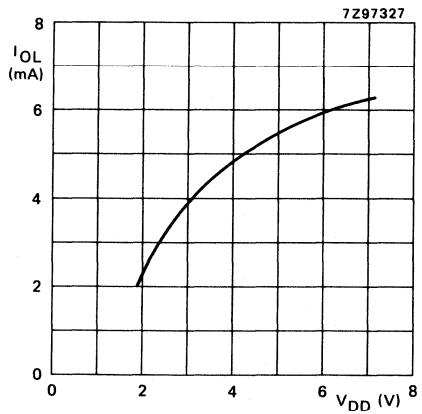
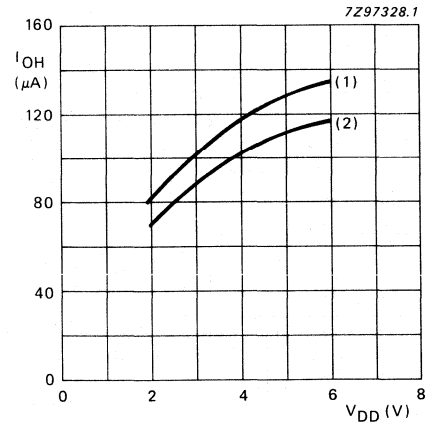
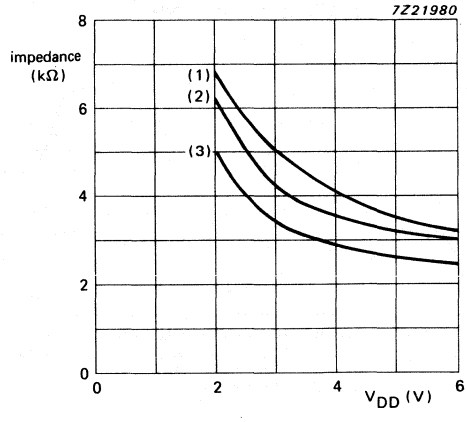


Fig. 44 Typical output sink current (I_{OL}), outputs P2.3/SDA and SCLK, as a function of the supply voltage (V_{DD}); V_O = 0,4 V.

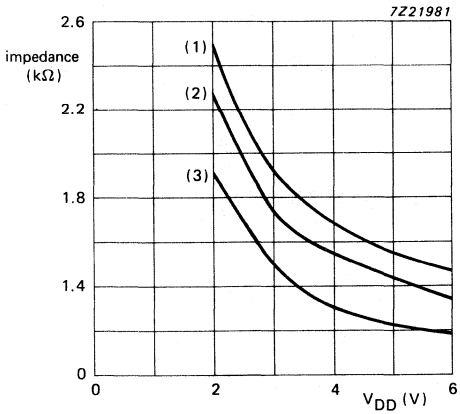


(1) $V_O = V_{SS}$
(2) $V_O = 0{,}7\ V_{DD}$
Fig. 45 Typical output source current ($-I_{OH}$) as a function of the supply voltage (V_{DD}).



(1) + 90 °C
(2) + 25 °C
(3) −50 °C
Fig. 46 Segment output impedance.

DEVELOPMENT DATA



(1) + 90 °C
(2) + 25 °C
(3) −50 °C
Fig. 47 Backplane output impedance.

Table 12 Input timing shown in Fig. 48.

symbol	timing
t_{BUF}	$\geqslant 14t_{XTAL}$
$t_{HD;STA}$	$\geqslant 14t_{XTAL}$
t_{HIGH}	$\geqslant 17t_{XTAL}$
t_{LOW}	$\geqslant 17t_{XTAL}$
$t_{SU;STO}$	$\geqslant 14t_{XTAL}$
$t_{HD;DAT}$	> 0
$t_{SU;DAT}$	$\geqslant 250$ ns
t_{RD}	$\leqslant 1\ \mu s$
t_{RC}	$\leqslant 1\ \mu s$
t_{FD}	$\leqslant 1\ \mu s$
t_{FC}	$\leqslant 0{,}3\ \mu s$

Notes to Table 12

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 167 ns for f_{XTAL} = 6 MHz.
These figures apply to all modes.

AC CHARACTERISTICS (continued)

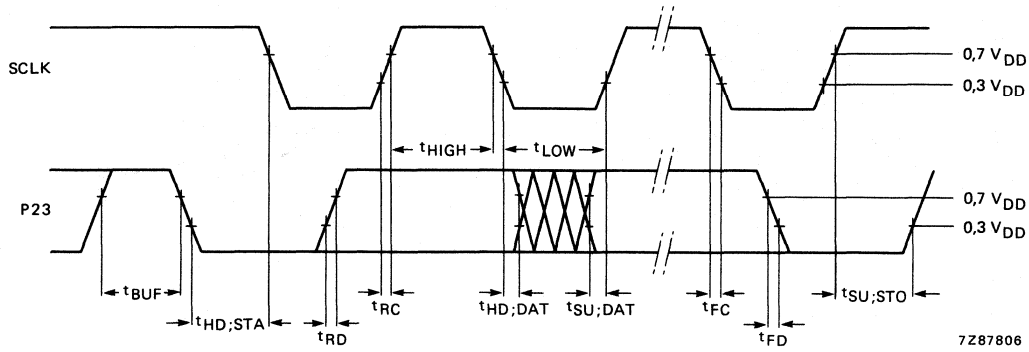


Fig. 48 PCF84C430 timing requirements for the P2.3 and SCLK *input* signals.

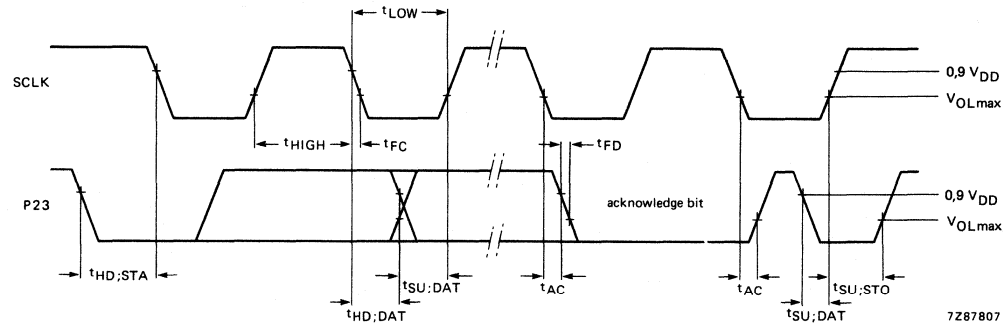


Fig. 49 PCF84C430 timing requirements for the P2.3 and SCLK *output* signals.

Table 13 Output timing shown in Fig. 49

symbol	timing	
	normal mode (ASC in S2 = 0)	low-speed mode (ASC in S2 = 1
$t_{HD;STA}$	$\frac{1}{2}$ (DF + 9) t_{XTAL}	$\frac{3}{4}$ (DF + 9) t_{XTAL}
t_{HIGH}	$\frac{1}{2}$ (DF) t_{XTAL}	$\frac{3}{4}$ (DF) t_{XTAL}
t_{LOW}	$\frac{1}{2}$ (DF) t_{XTAL}	$\frac{1}{4}$ (DF) t_{XTAL}
$t_{SU;STO}$	$\frac{1}{2}$ (DF − 3) t_{XTAL}	$\frac{1}{4}$ (DF − 3) t_{XTAL}
$t_{HD;DAT}$ (slave transmitter)		
any DF	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{HD;DAT}$ (master transmitter)		
for DF $\leqslant$ 51	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	–
for DF $\leqslant$ 99	–	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{SU;DAT}$ (master transmitter)		
for DF > 51	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$	–
for DF > 99	–	$\geqslant 15t_{XTAL}$ $\leqslant 24t_{XTAL}$
t_{AC}	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$	$\geqslant 9t_{XTAL}$ $\leqslant 12t_{XTAL}$
$t_{FD};t_{FC}$	$\leqslant$ 100 ns at C_b = 400 pF	$\leqslant$ 100 ns at C_b = 400 pF

DEVELOPMENT DATA

Notes to Table 13

t_{XTAL} = one period of the XTAL input frequency (f_{XTAL})
= 167 ns for f_{XTAL} = 6 MHz.
DF = divisor (see Table 3 Serial I/O section).
C_b = the maximum bus capacitance for each line.

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT129).
PCF8566T: 40-lead mini-pack (VSO40; SOT158A).

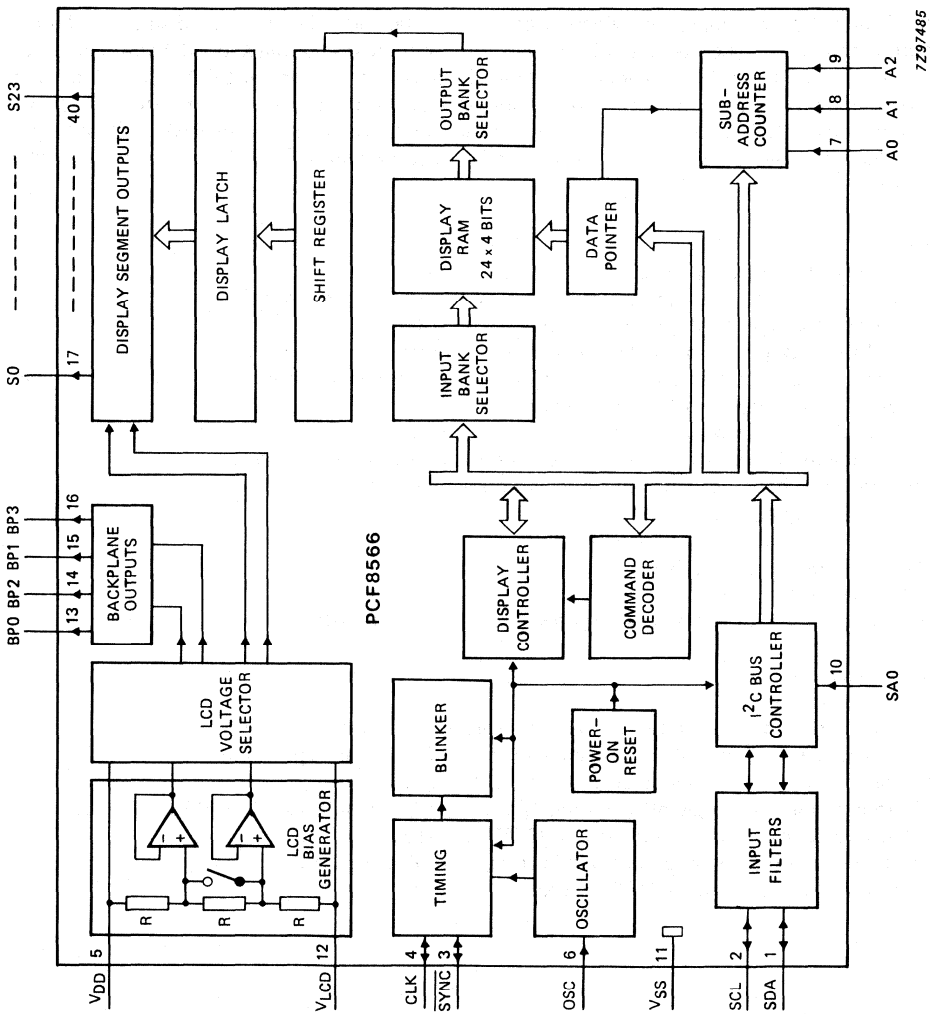


Fig. 1 Block diagram.

DEVELOPMENT DATA

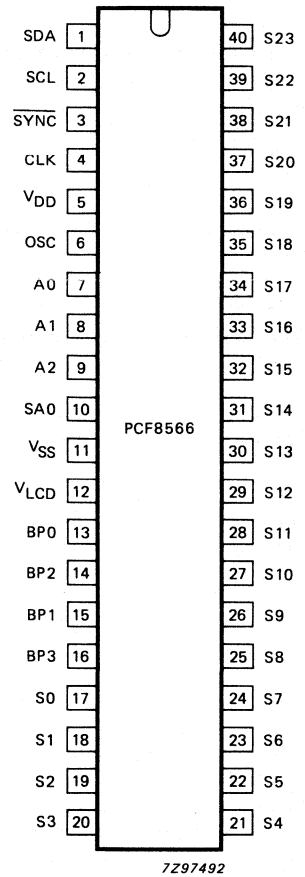


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17	S0	LCD segment outputs
to	to	
40	S23	

FUNCTIONAL DESCRIPTION

The PCF8566 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 24 segments. The display configurations possible with the PCF8566 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active back-plane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	96	12 digits + 12 indicator symbols	6 characters + 12 indicator symbols	96 dots (4 x 24)
3	72	9 digits + 9 indicator symbols	4 characters + 16 indicator symbols	72 dots (3 x 24)
2	48	6 digits + 6 indicator symbols	3 characters + 6 indicator symbols	48 dots (2 x 24)
1	24	3 digits + 3 indicator symbols	1 characters + 10 indicator symbols	24 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor/microcontroller maintains the two-line I^2C bus communication channel with the PCF8566. The internal oscillator is selected by tying OSC (pin 6) to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

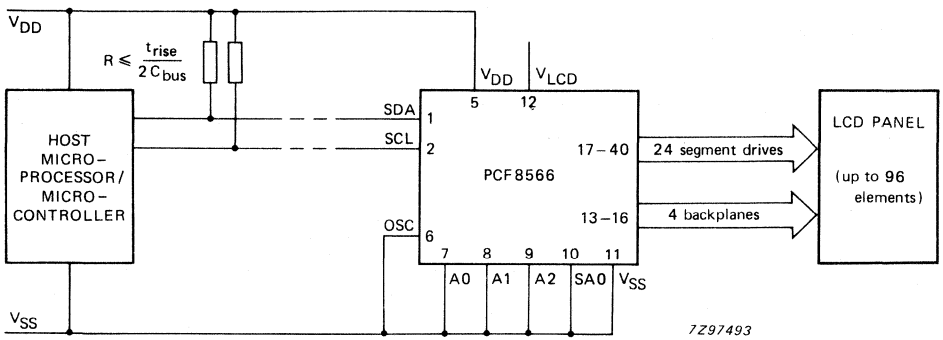


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8566 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\ V_{th}$.

Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex). The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

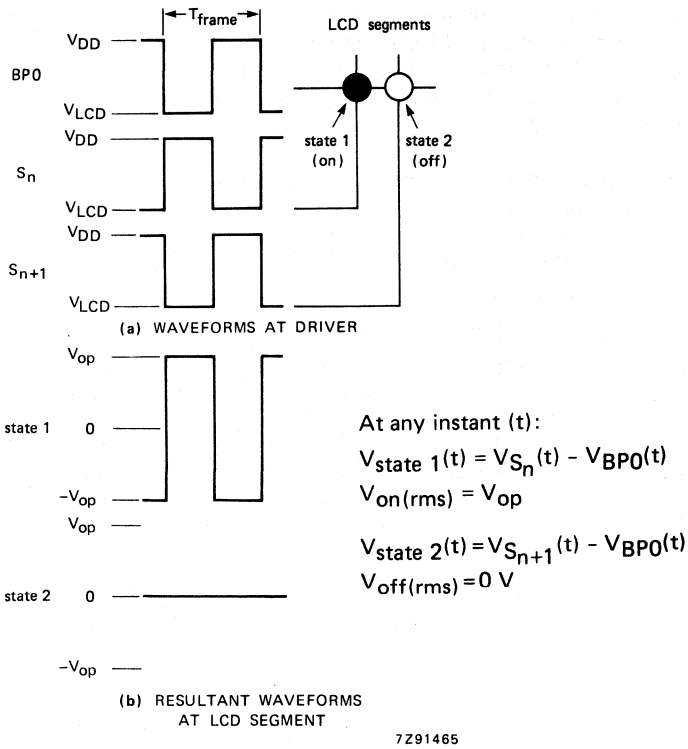
1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\ V_{off(rms)} = 2{,}449\ V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\ V_{off(rms)} = 2{,}309\ V_{off(rms)}$

These compare with $V_{op} = 3\ V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.



At any instant (t):

$V_{state\ 1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = V_{op}$

$V_{state\ 2}(t) = V_{S_{n+1}}(t) - V_{BP0}(t)$

$V_{off(rms)} = 0\ V$

Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8566 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

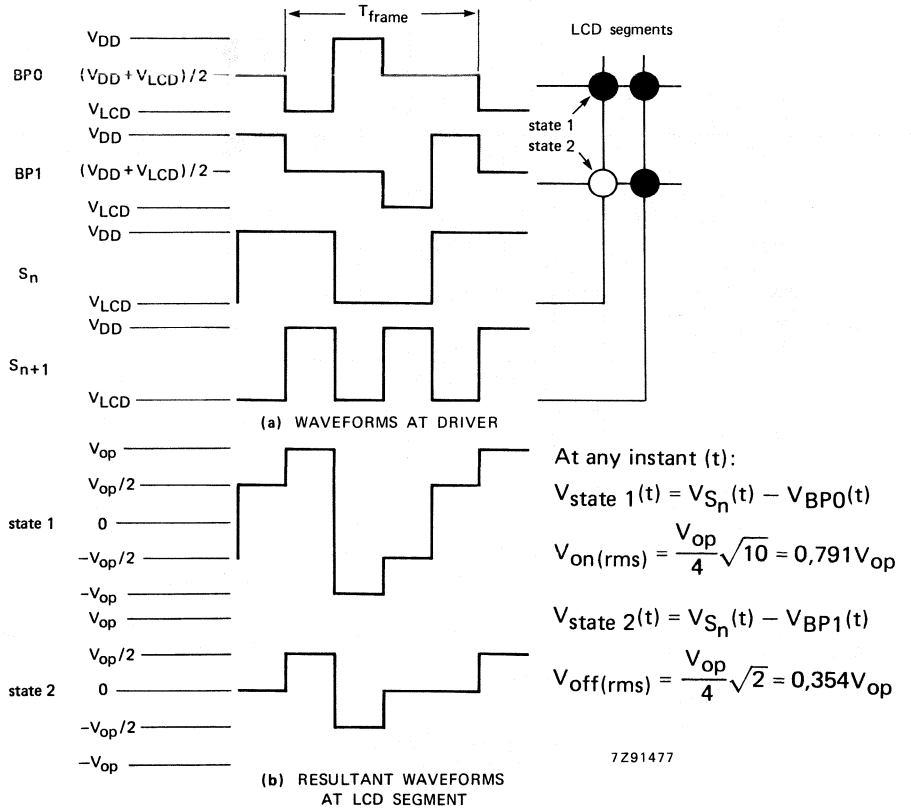


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

DEVELOPMENT DATA

LCD drive mode waveforms (continued)

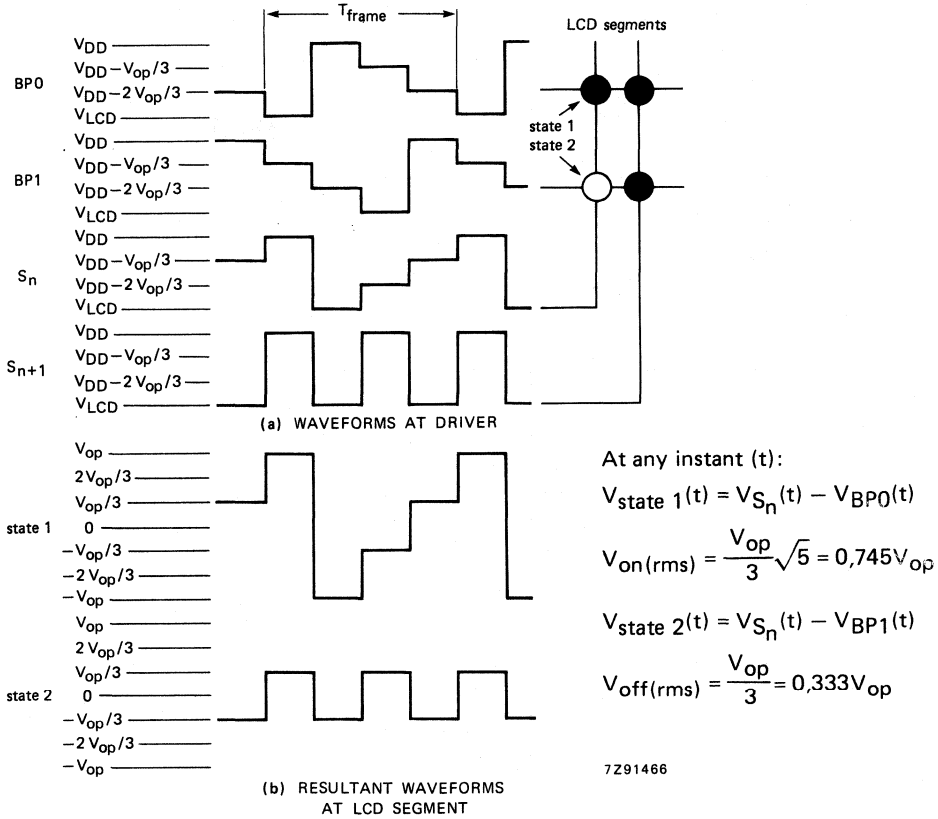


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive wavefront for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

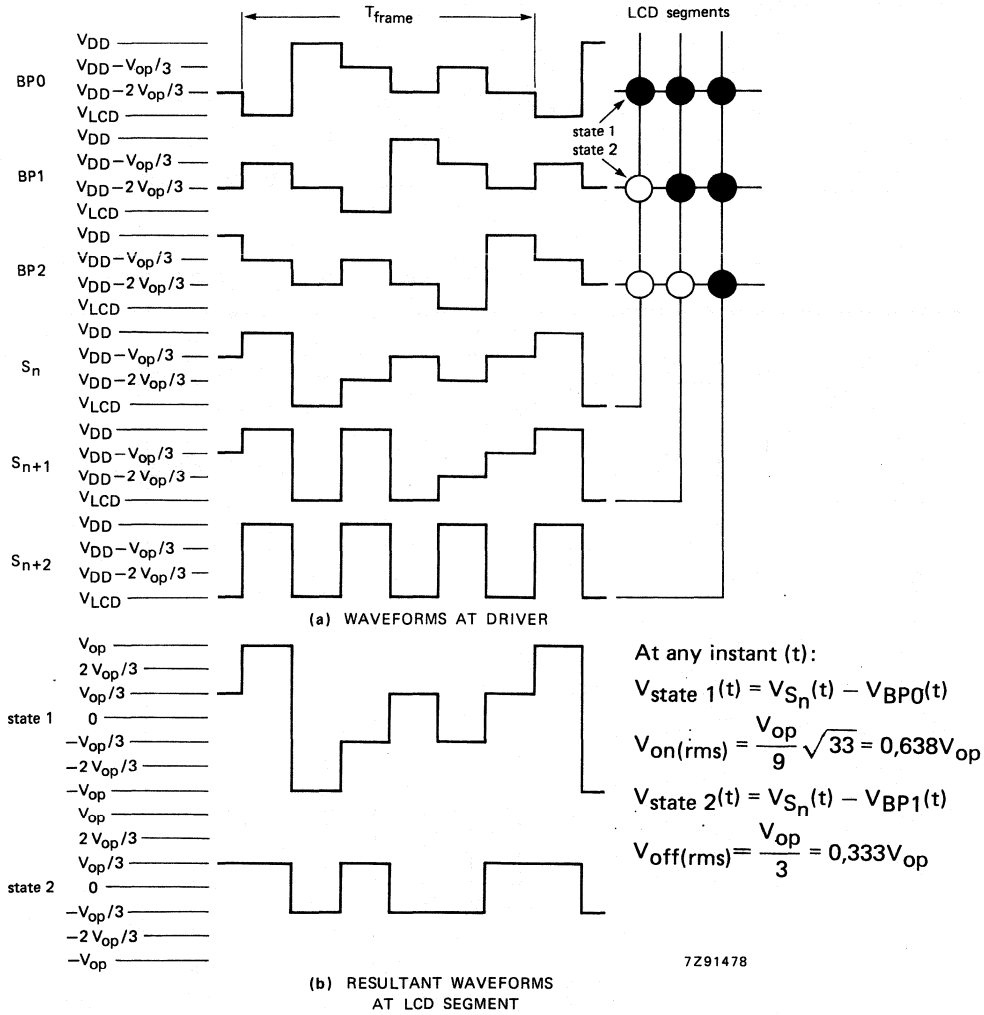
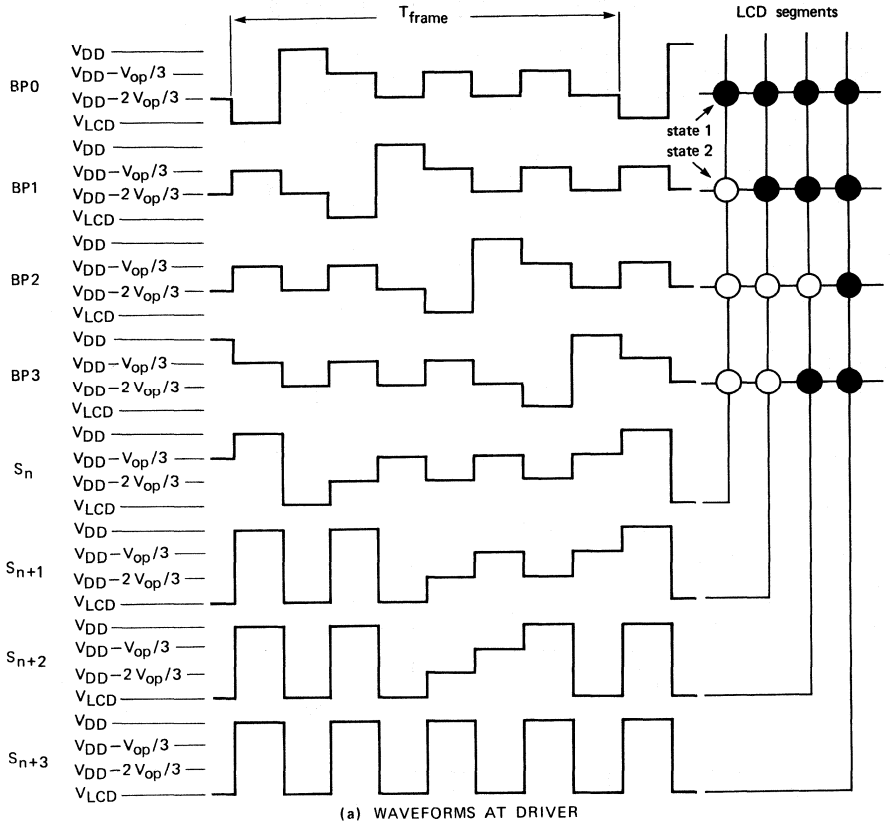


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)



At any instant (t):

$V_{state\ 1}(t) = V_{S_n}(t) - V_{BP0}(t)$

$V_{on(rms)} = \frac{V_{op}}{3}\sqrt{3} = 0{,}577V_{op}$

$V_{state\ 2}(t) = V_{S_n}(t) - V_{BP1}(t)$

$V_{off(rms)} = \frac{V_{op}}{3} = 0{,}333V_{op}$

Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

The internal logic and the LCD drive signals of the PCF8566 or PCF8576 are timed either by the built-in oscillator or from an external clock.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C bus. To allow I^2C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

Internal clock

When the internal oscillator is used, OSC (pin 6) should be tied to V_{SS}. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8566s and PCF8576s in the system.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

Timing

The timing of the PCF8566 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8566s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8566 mode	f_{frame}	nominal f_{frame} (Hz)
normal mode	$f_{CLK}/2880$	64
power-saving mode	$f_{CLK}/480$	64

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller, this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line low until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 24 segment outputs S0 to S23 (pins 17 to 40) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 24 segment outputs are required the unused segment outputs should be left open-circuit.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 24 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 24 segments operated with respect to backplane BP0 (Fig. 9). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

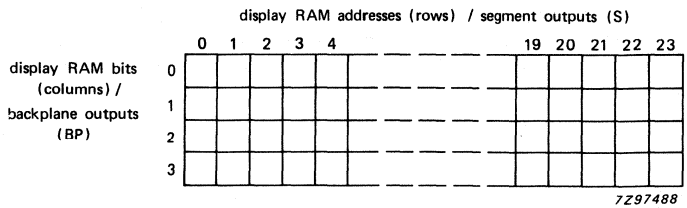


Fig. 9 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8566 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 10; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 10, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

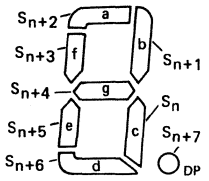
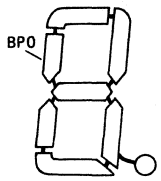
Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 10. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). A0, A1 and A2 should be tied to V_{SS} or V_{DD}. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8566 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

<table>
<tr><th>drive mode</th><th>LCD segments</th><th>LCD backplanes</th><th>display RAM filling order</th><th>transmitted display byte</th></tr>
<tr><td>static</td><td> 
</td><td> 
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<tr><td>bit/ 0</td><td>c</td><td>b</td><td>a</td><td>f</td><td>g</td><td>e</td><td>d</td><td>DP</td></tr>
<tr><td>BP 1</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
<tr><td>2</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
<tr><td>3</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
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</td><td>msb lsb
c b a f g e d DP</td></tr>
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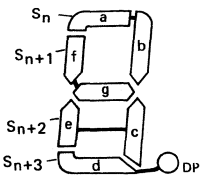
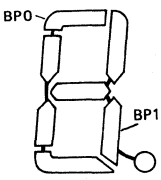
multiplex</td><td> 
</td><td> 
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<tr><td>2</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
<tr><td>3</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
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a b f g e c d DP</td></tr>
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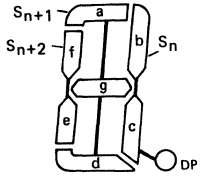
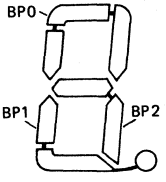
multiplex</td><td> 
</td><td> 
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<tr><td>2</td><td>c</td><td>g</td><td>x</td></tr>
<tr><td>3</td><td>x</td><td>x</td><td>x</td></tr>
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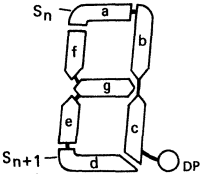
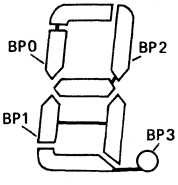
b DP c a d g f e</td></tr>
<tr><td>1 : 4
multiplex</td><td> 
</td><td> 
</td><td>
<table>
<tr><th></th><th>n</th><th>n + 1</th></tr>
<tr><td>bit/ 0</td><td>a</td><td>f</td></tr>
<tr><td>BP 1</td><td>c</td><td>e</td></tr>
<tr><td>2</td><td>b</td><td>g</td></tr>
<tr><td>3</td><td>DP</td><td>d</td></tr>
</table>
</td><td>msb lsb
a c b DP f e g d</td></tr>
</table>

Fig. 10 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

7Z91469

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8566 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8566 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

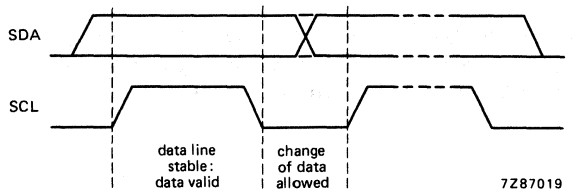


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

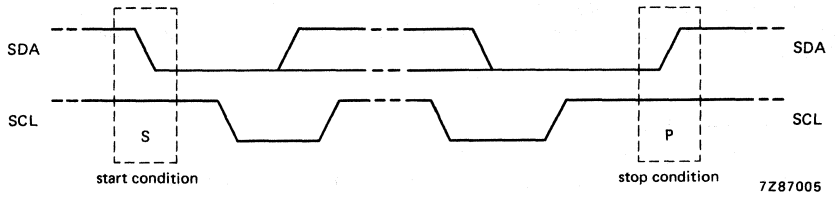


Fig. 12 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

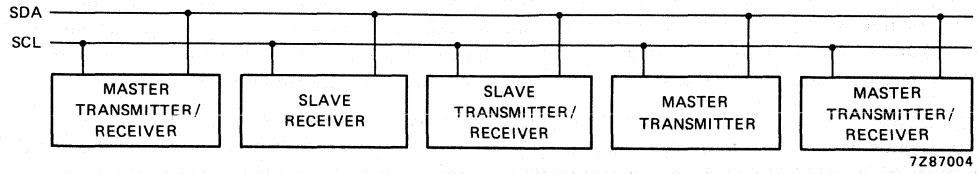


Fig. 13 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

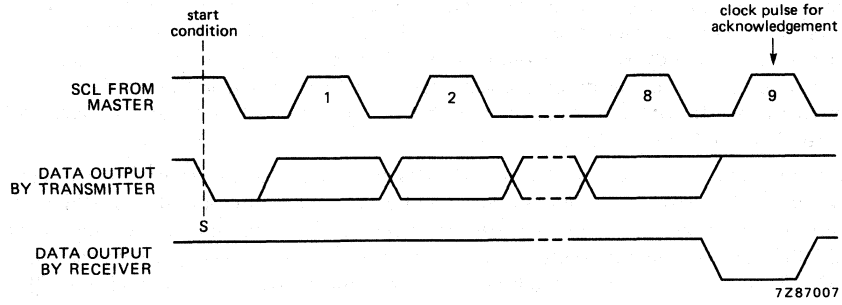


Fig. 14 Acknowledgement on the I^2C bus.

PCF8566 I²C bus controller

The PCF8566 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8566 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally left open-circuit or tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are left open-circuit or tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8566 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8566 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111110 and 0111111) are reserved for PCF8566. The least-significant bit of the slave address that a PCF8566 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8566 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8566s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 15. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8566 slave addresses available. All PCF8566s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8566s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8566s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8566s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8566 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8566. After the last display byte, the I²C bus master issues a stop condition (P).

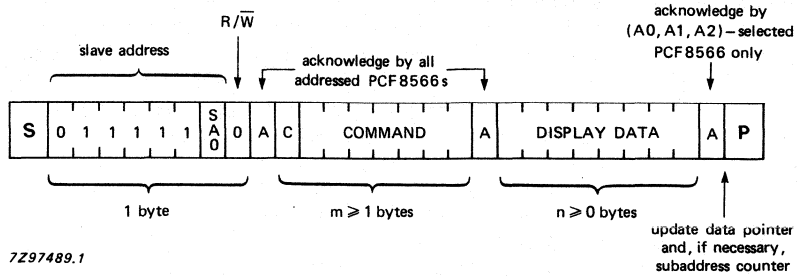


Fig. 15 I^2C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I^2C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 16). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

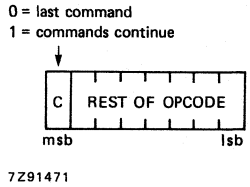


Fig. 16 General format of command byte.

The five commands available to the PCF8566 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8566 commands

command/opcode	options	description
MODE SET C 1 0 LP E B M1 M0	LCD drive mode: bits M1 M0 static (1 BP): 0 1 1 : 2 MUX (2 BP): 1 0 1 : 3 MUX (3 BP): 1 1 1 : 4 MUX (4 BP): 0 0 LCD bias: bit B 1/3 bias: 0 1/2 bias: 1 display status: bit E disabled (blank): 0 enabled: 1 mode: bit LP normal mode: 0 power-saving mode: 1	Defines LCD drive mode Defines LCD bias configuration Defines display status The possibility to disable the display allows implementation of blinking under external control Defines power dissipation mode
LOAD DATA POINTER C 0 0 P4 P3 P2 P1 P0	bits P4 P3 P2 P1 P0 5-bit binary value of 0 to 23	Five bits of immediate data, bits P4 to P0, are transferred to the data pointer to define one of twenty-four display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

command/opcode	options	description
BANK SELECT C 1 1 1 1 0 I O	static / 1 : 2 MUX / bit I RAM bit 0 / RAM bits 0, 1 / 0 RAM bit 2 / RAM bits 2, 3 / 1 static / 1 : 2 MUX / bit O RAM bit 0 / RAM bits 0, 1 / 0 RAM bit 2 / RAM bits 2, 3 / 1	Defines input bank selection (storage of arriving display data) Defines output bank selection (retrieval of LCD display data) The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes
BLINK C 1 1 1 0 A BF1 BF0	blink frequency / bits BF1 / BF0 off / 0 / 0 2 Hz / 0 / 1 1 Hz / 1 / 0 0,5 Hz / 1 / 1 blink mode / bit A normal blinking / 0 alternation blinking / 1	Defines the blinking frequency Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8566 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8566s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8566s. When cascaded, several PCF8566s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8566s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (Fig. 17).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8566s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8566s with differing SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8566 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8566 to assert $\overline{\text{SYNC}}$. The timing relationships between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8576 are shown in Fig. 18. The waveforms are identical with the parent device PCF8576. Casadability between PCF8566s and PCF8576s is possible, giving cost effective LCD applications.

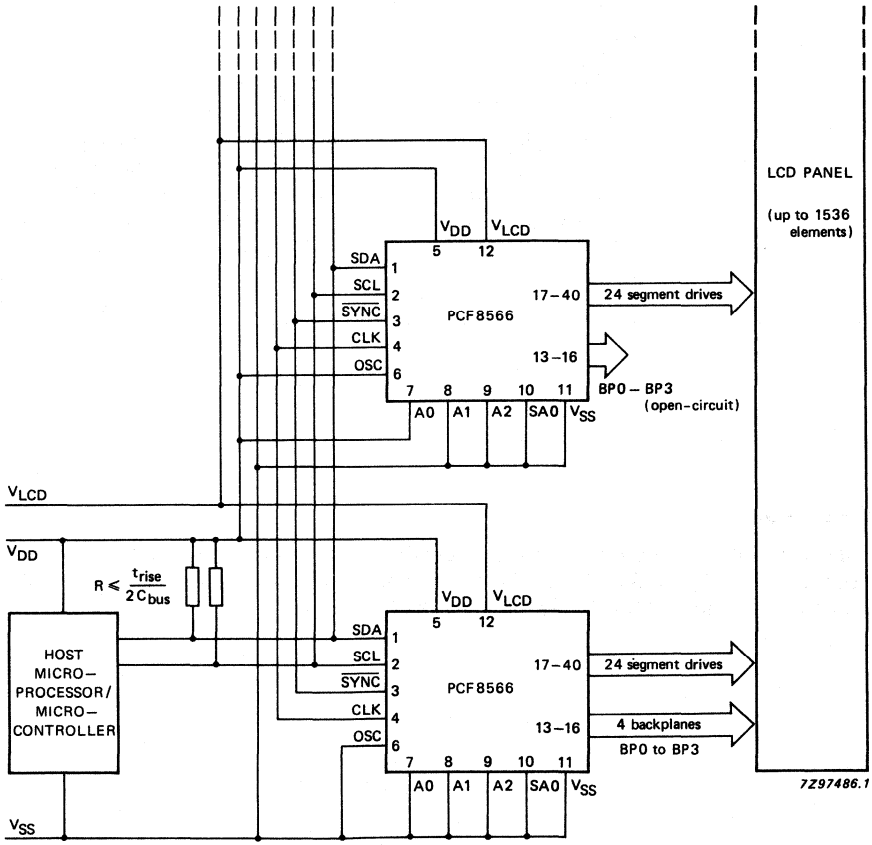


Fig. 17 Cascaded PCF8566 configuration.

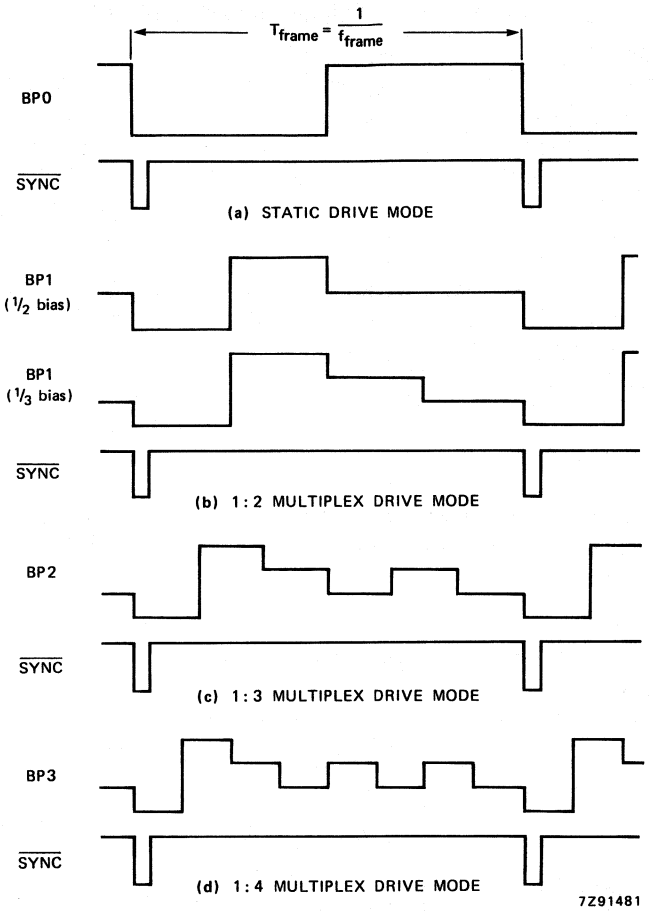


Fig. 18 Synchronization of the cascade for the various PCF8566 drive modes.

For single plane wiring of PCF8566s, see section "APPLICATION INFORMATION".

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range; see note	V_{DD}		−0,5 to + 7 V
LCD supply voltage range	V_{LCD}		V_{DD} −7 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S23; BP0 to BP3)	V_O		V_{LCD} −0,5 to V_{DD} + 0,5 V
DC input current	$\pm I_I$	max.	20 mA
DC output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

Note

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;
T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6	V
LCD supply voltage	V_{LCD}	V_{DD} −6	–	V_{DD} −2,5	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 1)	I_{DD}	–	30	90	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz; A0, A1 and A2 tied to V_{SS} (note 1)	I_{LP}	–	15	40	μA

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD} –0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	–1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0, CLK, OSC, A0, A1, A2, SCL, SDA) at $V_I = V_{SS}$ or V_{DD}	$\pm I_L$	–	–	1	μA
Pull-down current (A0; A1; A2; OSC) at V_I = 1 V and V_{DD} = 5 V	I_{pd}	15	50	150	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	15	25	60	kΩ
Power-on reset level (note 2)	V_{REF}	–	1,3	2,0	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 3)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S23) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}$ –5 V (note 4)	R_{BP}	–	1	5	kΩ
Output impedance (S0 to S23) at $V_{LCD} = V_{DD}$ –5 V (note 4)	R_S	–	3	7,0	kΩ

AC CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;

T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V (note 6)	f_{CLK}	125	200	315	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{\text{SYNC}}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{\text{SYNC}}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at V_{LCD} = V_{DD} −5 V	t_{PLCD}	–	–	30	μs
I²C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_r	–	–	1	μs
Fall time	t_f	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

Notes to characteristics

1. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
2. Resets all logic when $V_{DD} < V_{REF}$.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
6. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

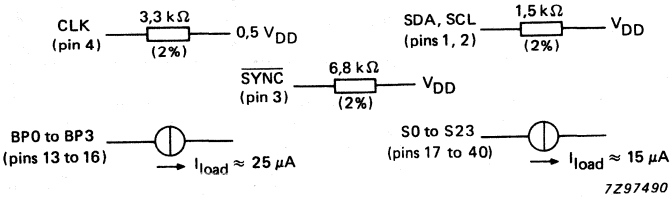


Fig. 19 Test loads.

DEVELOPMENT DATA

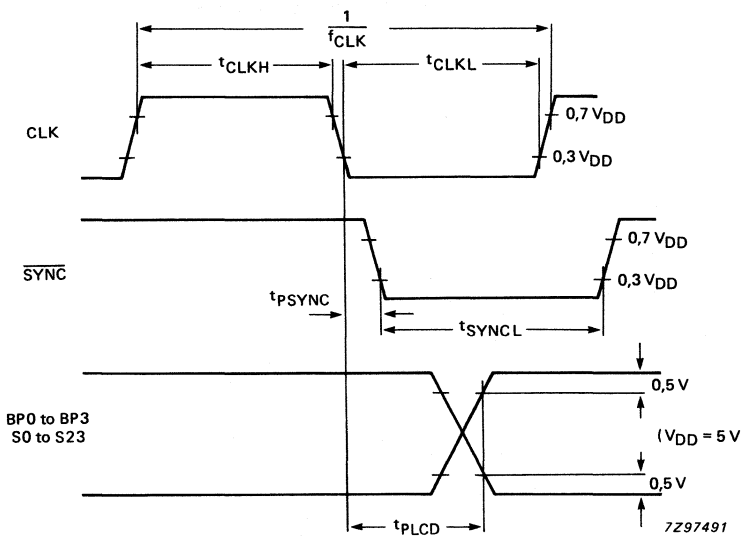


Fig. 20 Driver timing waveforms.

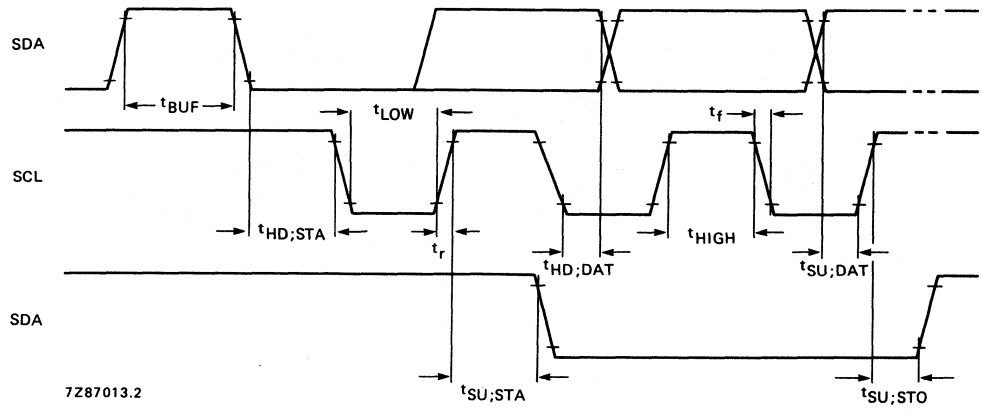
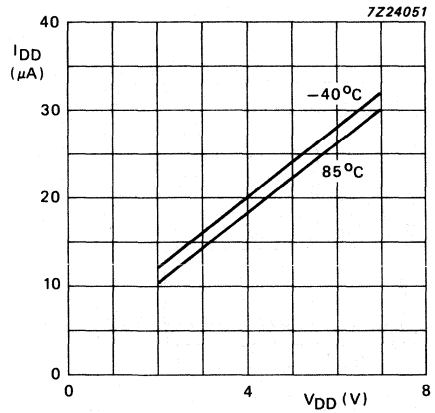
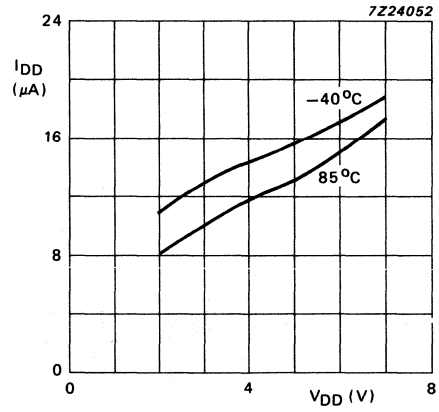


Fig. 21 I^2C bus timing waveforms.



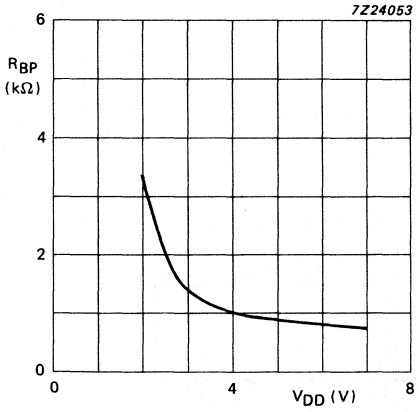
(a) Normal mode; V_{LCD} = 0 V; external clock = 200 kHz.



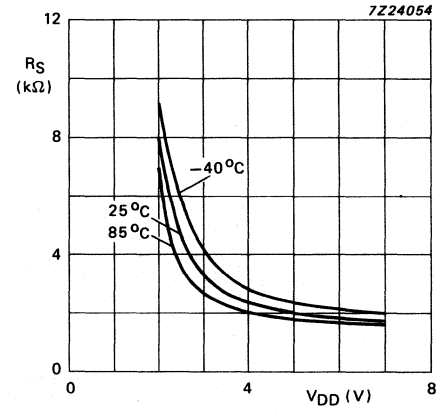
(b) Low power mode; V_{LCD} = 0 V; external clock = 35 kHz.

Fig. 22 Typical supply current characteristics.

DEVELOPMENT DATA



(a) Backplane output impedance BP0 to BP3 (R_{BP}); V_{DD} = 5 V; T_{amb} = −40 to + 85 °C.



(b) Segment output impedance S0 to S23 (R_S); V_{DD} = 5 V.

Fig. 23 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

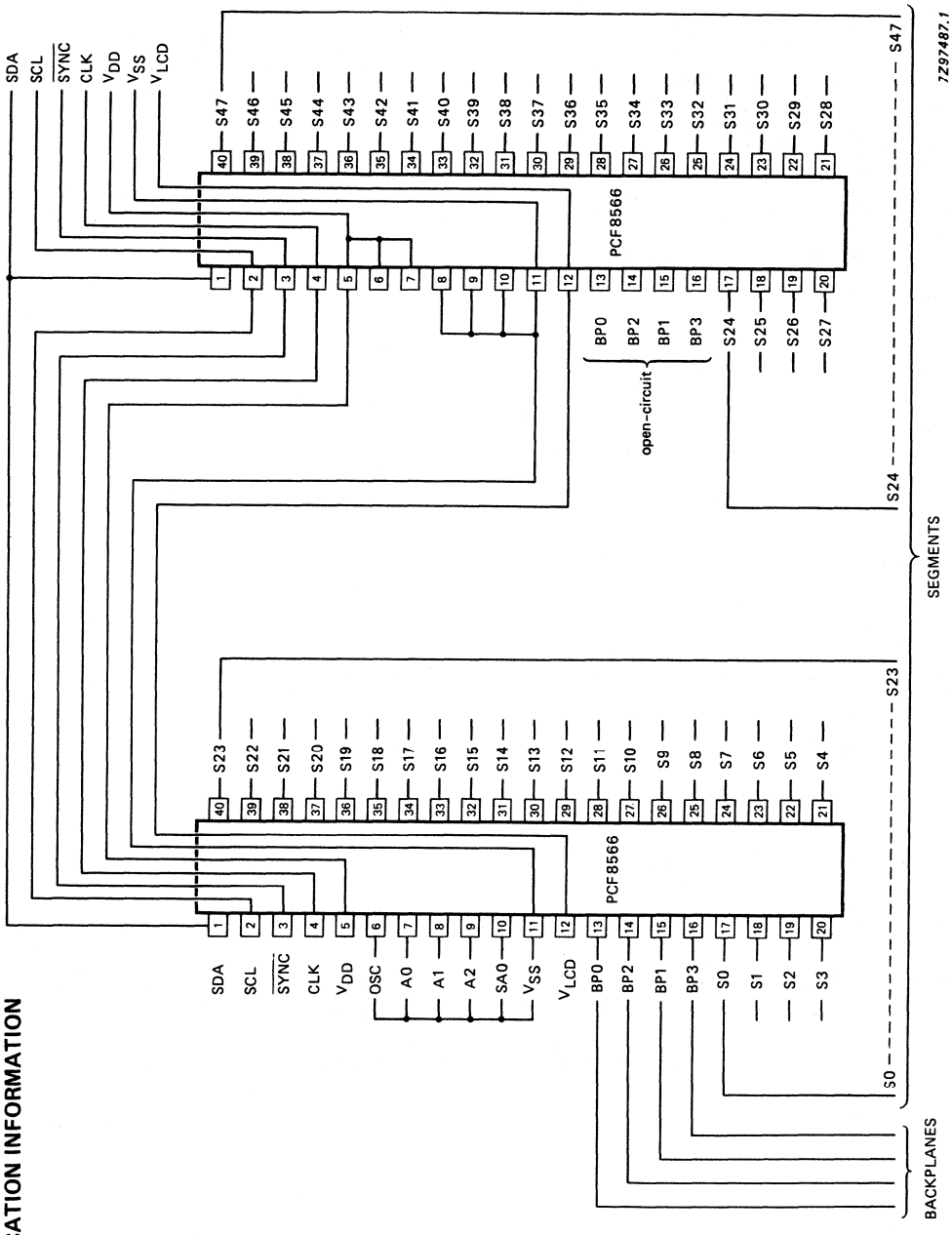


Fig. 24 Single plane wiring of packaged PCF8566s.

128 X 8-BIT/256 X 8-BIT STATIC RAMS WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8570, PCF8570C and PCF8571 are low-power static CMOS RAMs. The PCF8570 and PCF8570C are organized as 256 words by 8-bits and the PCF8571 is organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1 and A2 are used for hardware address, allowing the use of up to eight devices connected to the bus without additional hardware. For system expansion over 8 devices the PCF8570/71 can be used in conjunction with the PCF8750C which has an alternative slave address for memory extension up to 16 devices.

Features

- Operating supply voltage 2.5 V to 6 V
- Low data retention voltage min. 1.0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder — channel presets
- General purpose — RAM expansion for the microcontroller families MAB8400, PCF84CXX and most other microcontrollers

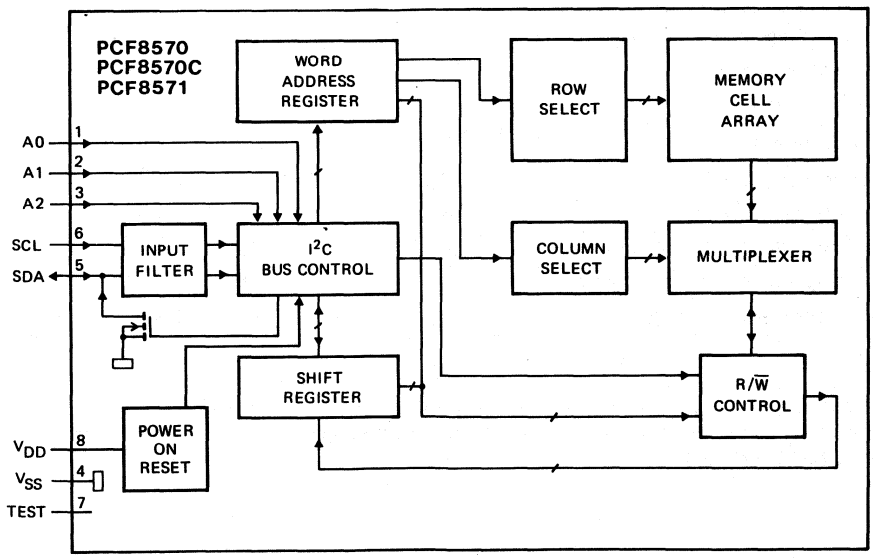


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8570/PCF8570C/PCF8571/P: 8-lead DIL; plastic (SOT97).
PCF8570/PCF8570C/PCF8571/T: 8-lead mini-pack (SO8L; SOT176C).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line } I^2C-bus
6	SCL	serial clock line } I^2C-bus
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 12 and 13)
8	V_{DD}	positive supply

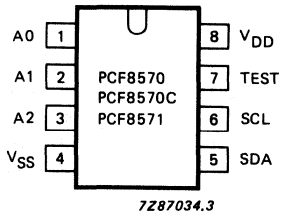


Fig.2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.8	+8.0	V
Input voltage range	V_I	−0.8	V_{DD} + 0.8	V
DC input current	$\pm I_I$	–	10	mA
DC output current	$\pm I_O$	–	10	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; $\pm I_{SS}$	–	50	mA
Total power dissipation	P_{tot}	–	300	mW
Power dissipation per output	P_O	–	50	mW
Operating ambient temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
Supply current	$V_I = V_{DD}$ or V_{SS}					
operating	f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
standby	f_{SCL} = 0 Hz	I_{DDO}	–	–	15	μA
	T_{amb} = −25 to +70 °C	I_{DDO}	–	–	5	μA
Power-on reset level	note 1	V_{POR}	1.5	1.9	2.3	V
Inputs, input/output SDA						
Input voltage LOW	note 2	V_{IL}	−0.8	–	0.3 V_{DD}	V
Input voltage HIGH	note 2	V_{IH}	0.7 V_{DD}	–	V_{DD} + 0.8	V
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
Inputs A0 to A2; TEST						
Input leakage current	$V_I = V_{DD}$ or V_{SS}	$\pm I_{LI}$	–	–	250	nA
Inputs SCL; SDA						
Input capacitance	$V_I = V_{SS}$	C_I	–	–	7	pF
LOW V_{DD} data retention						
Supply voltage for data retention		V_{DDR}	1	–	6	V
Supply current	V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current	V_{DDR} = 1 V; T_{amb} = −25 to +70 °C	I_{DDR}	–	–	2	μA
Power saving mode	see Figs 12 and 13					
Supply current	TEST = V_{DD}; T_{amb} = 25 °C					
PCF8570/PCF8570C		I_{DDR}	–	50	400	nA
PCF8571		I_{DDR}	–	50	200	nA
Recovery time		t_{HD2}	–	50	–	μs

Notes to the characteristics

1. The power-on reset circuit resets the I²C-bus logic when $V_{DD} < V_{POR}$. The status of the device after a power-on reset condition can be tested by sending the slave address and testing the acknowledge bit.
2. If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow: this current must not exceed ± 0.5 mA.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

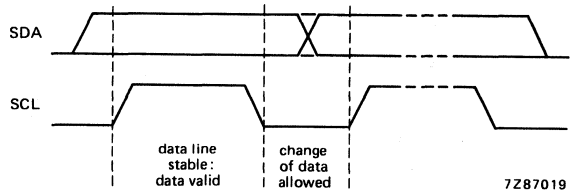


Fig.3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

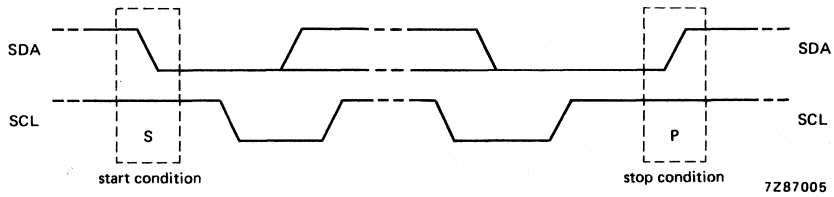


Fig.4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

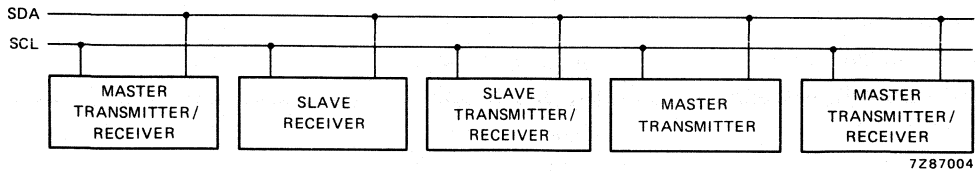


Fig.5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

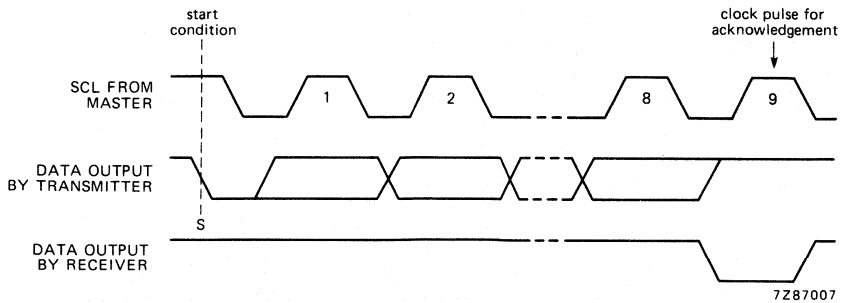


Fig.6 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

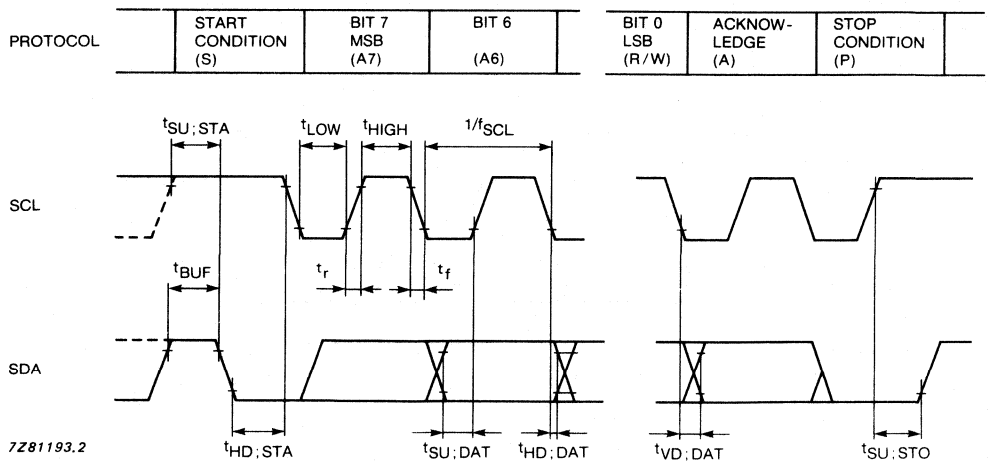


Fig.7 I²C-bus timing diagram.

Bus protocol

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C-bus configuration for different PCF8570/PCF8570C/PCF8571 READ and WRITE cycles is shown in Fig.8.

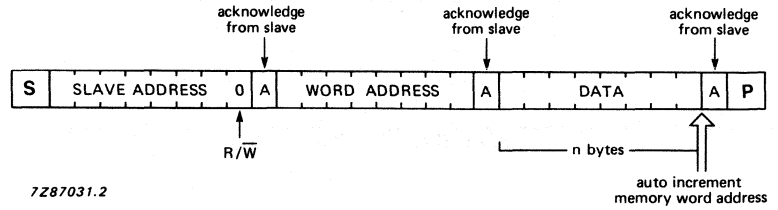


Fig.8(a) Master transmits to slave receiver (WRITE mode).

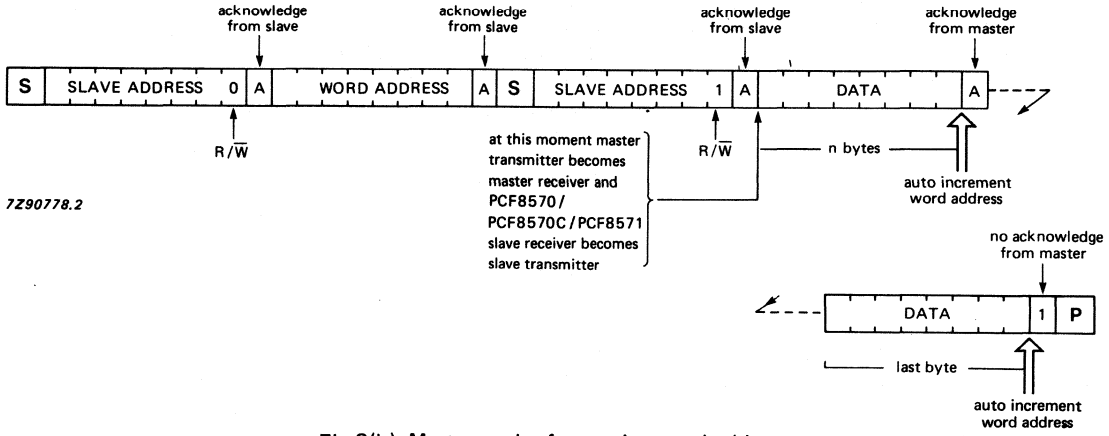


Fig.8(b) Master reads after setting word address (WRITE word address; READ data).

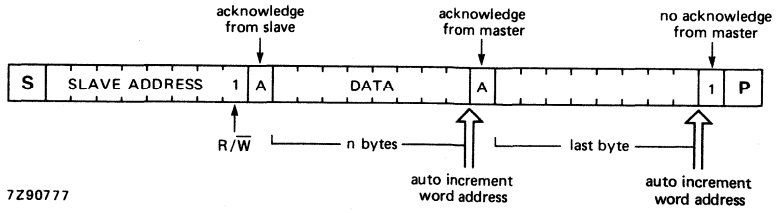


Fig.8(c) Master reads slave immediately after first byte (READ mode).

APPLICATION INFORMATION

The PCF8570/PCF8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig.9). The PCF8570C has slave address 1011 as group 1, while group 2 is fully programmable (see Fig.10).

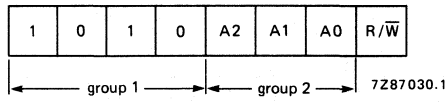


Fig.9 PCF8570 and PCF8571 address.

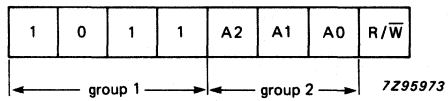
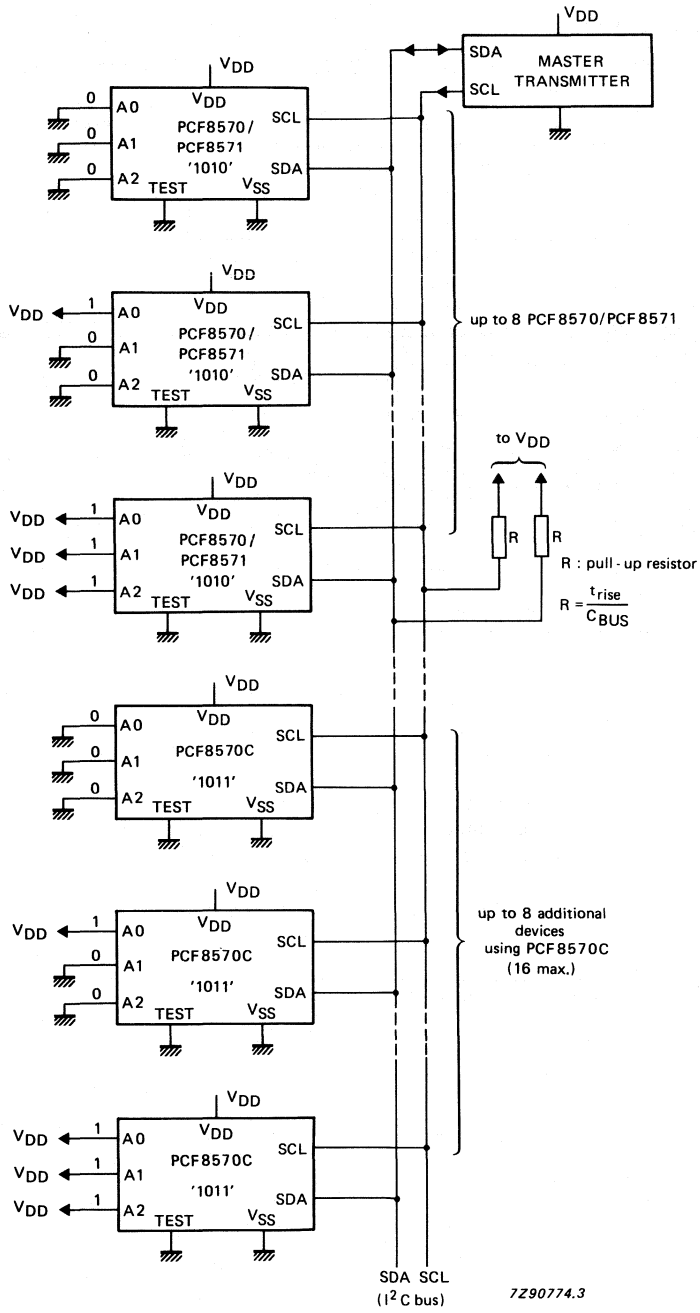


Fig.10 PCF8570C address.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open-circuit.

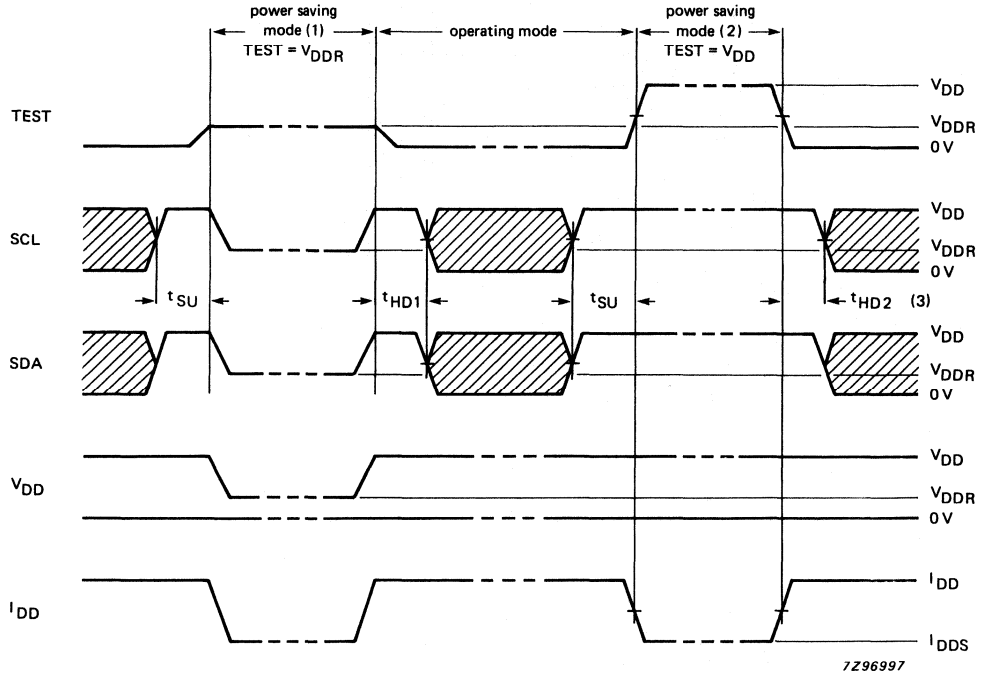


It is recommended that a 4.7 μF/10 V solid aluminium capacitor (SAL) be connected between V_{DD} and V_{SS}.

Fig.11 Application diagram.

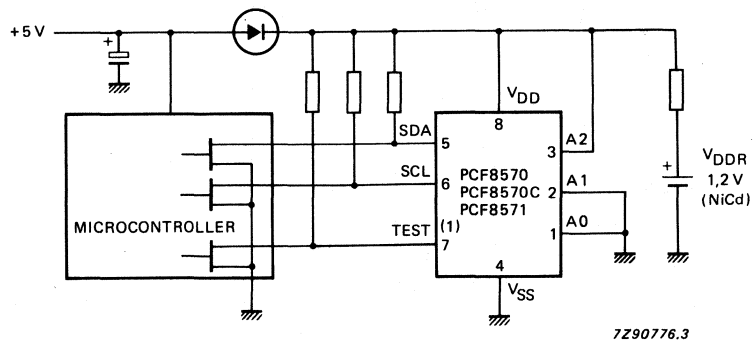
POWER SAVING MODE

With the condition **TEST** = V_{DD} or V_{DDR} the PCF8570/PCF8570C/PCF8571 goes into the power saving mode and I²C-bus logic is reset.



(1) Power saving mode without 5 V supply voltage.
(2) Power saving mode with 5 V supply voltage.
(3) t_{SU} and $t_{HD1} \geqslant 4\ \mu s$ and $t_{HD2} \geqslant 50\ \mu s$.

Fig.12 Timing for power saving mode.



(1) In the operating mode TEST = 0; In the power saving mode TEST = V_{DDR}.

It is recommended that a 4.7 μF/10 V solid aluminium capacitor (SAL) be connected between V_{DD} and V_{SS}.

Fig.13 Application example for power saving mode.

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, CMOS circuit that functions as a real time clock/calendar with an I^2C-bus interface.
The IC incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred via a serial two-line bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1.2 V nickel cadium battery. The time base is generated from a 32.768 kHz crystal-controlled oscillator.

Features

- Serial input/output I^2C-bus interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32.768 kHz)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range					
clock (pin 16 to pin 15)	$V_{DD}-V_{SS1}$	1.1	–	6.0	V
I^2C interface (pin 16 to pin 8)	$V_{DD}-V_{SS2}$	2.5	–	6.0	V
Crystal oscillator frequency	f_{osc}	–	32.768	–	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT38).
PCF8573T: 16-lead mini-pack; plastic (SO16L; SOT162A).

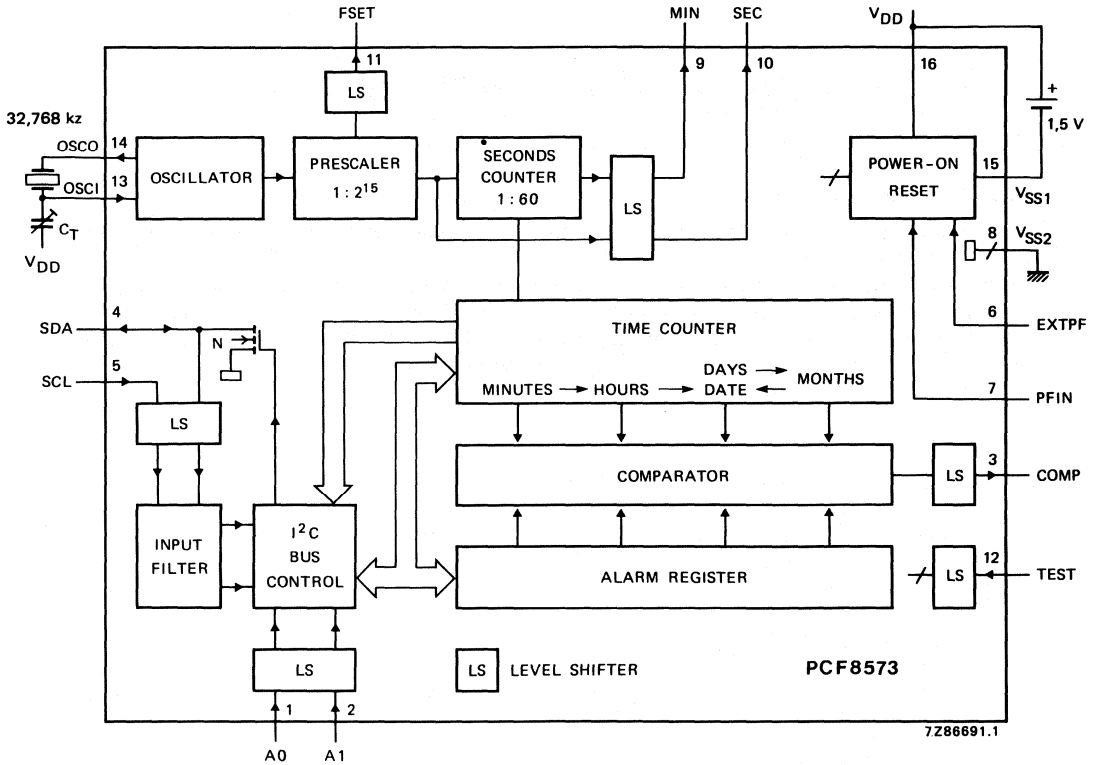


Fig.1 Block diagram.

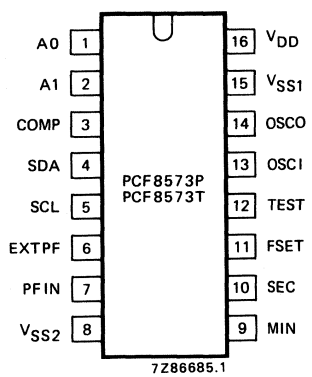


Fig.2 Pinning diagram.

PINNING

1	A0	address input
2	A1	address input
3	COMP	comparator output
4	SDA	serial data line (I^2C-bus)
5	SCL	serial clock line (I^2C-bus)
6	EXTPF	enable power fail flag input
7	PFIN	power fail flag input
8	V_{SS2}	negative supply 2 (I^2C interface)
9	MIN	one pulse per minute output
10	SEC	one pulse per second output
11	FSET	oscillator tuning output
12	TEST	test input; must be connected to V_{SS2} when not in use
13	OSCI	oscillator input
14	OSCO	oscillator input/output
15	V_{SS1}	negative supply 1 (clock)
16	V_{DD}	common positive supply

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32.768 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I²C-bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH-to-LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (note 1)
			or 29 → 01	2 (note 1)
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note to Table 1

1. Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I²C-bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I²C-bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I²C-bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I²C-bus.

FUNCTIONAL DESCRIPTION (continued)

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD}-V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD}-V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I²C-bus. A power on reset for the I²C-bus control is generated on-chip when the supply voltage $V_{DD}-V_{SS2}$ is less than V_{TH2}.

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{DD} = V_{SS2}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C-BUS

The I² C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig.3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

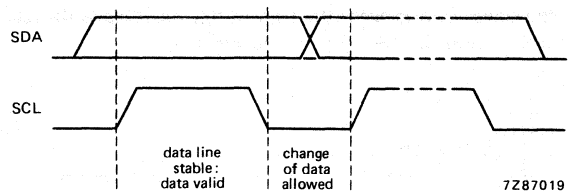


Fig.3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

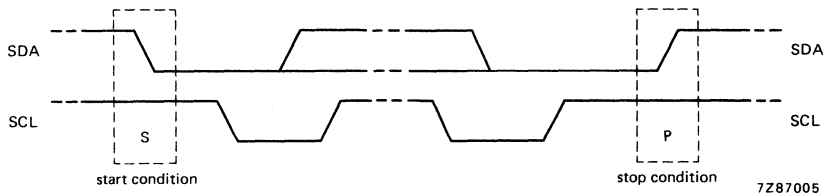


Fig.4 Definition of start and stop conditions.

System configuration (see Fig.5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

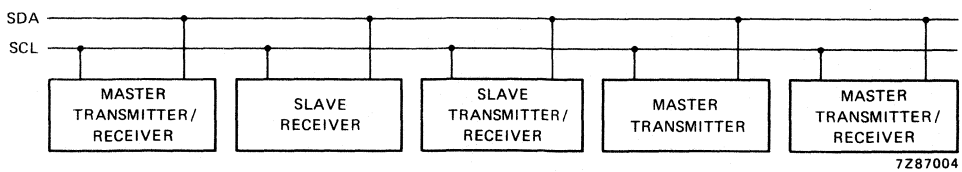


Fig.5 System configuration.

CHARACTERISTICS OF THE I²C-bus (continued)

Acknowledge (see Fig.6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig.10 and Fig.11).

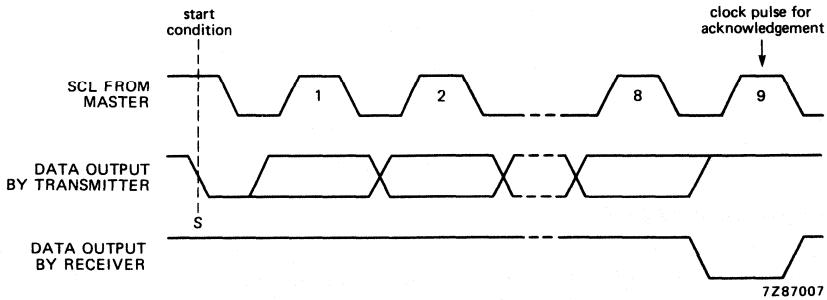


Fig.6 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

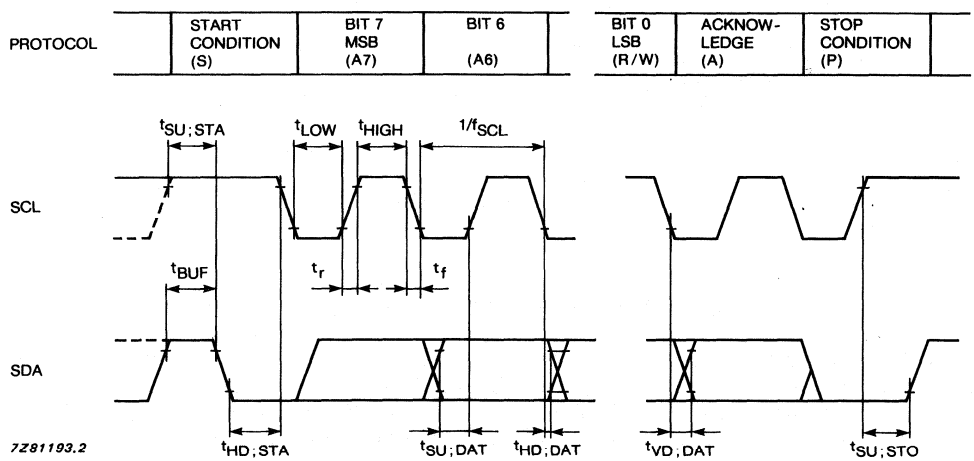


Fig.7 I²C-bus timing diagram.

ADDRESSING

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig.8.

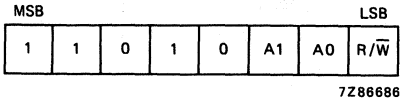


Fig.8 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I²C-bus configuration for different clock/calendar READ and WRITE cycles is shown in Figs 9, 10 and 11.

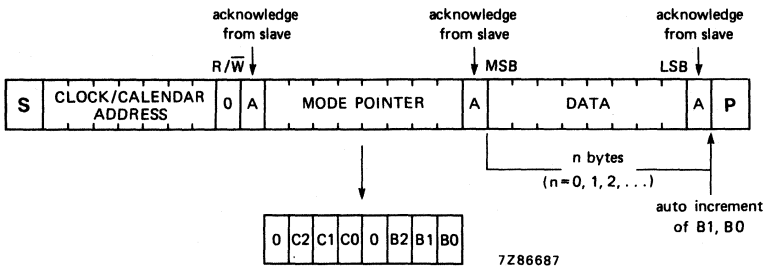


Fig.9 Master transmitter transmits to clock/calendar slave receiver.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nible is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB				DATA			LSB	
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where:

"X" is the don't care bit
"D" is the data bit
Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where:

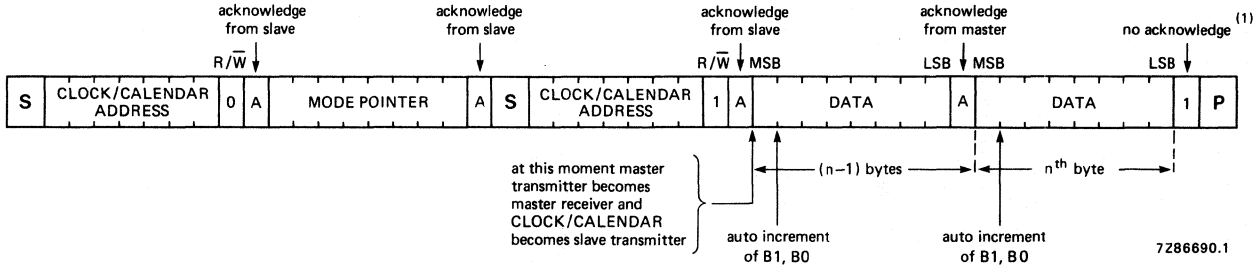
"X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where:

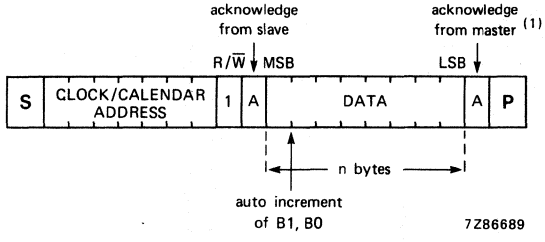
"D" is the data bit
* = minutes
** = seconds.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig.10 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig.11 Master reads clock/calendar immediately after first byte.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	condition	symbol	min.	max.	unit
Supply voltage range					
pin 16 to pin 15		$V_{DD}-V_{SS1}$	−0.3	8.0	V
pin 16 to pin 8		$V_{DD}-V_{SS2}$	−0.3	8.0	V
Voltage input					
pins 4 and 5	note 1	V_I	$V_{SS2}-0.8$	$V_{DD}+0.8$	V
pins 6, 7, 13 and 14		V_I	$V_{SS1}-0.6$	$V_{DD}+0.6$	V
any other pin		V_I	$V_{SS2}-0.6$	$V_{DD}+0.6$	V
Input current		I_I	–	10	mA
Output current		I_O	–	10	mA
Power dissipation per output		P_O	–	100	mW
Total power dissipation		P_{tot}	–	200	mW
Operating ambient temperature range		T_{amb}	−40	+85	°C
Storage temperature range		T_{stg}	−55	+125	°C

Note to the Ratings

1. With input impedance of minimum 500 Ω.

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified. Typical values at T_{amb} = +25 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage						
I^2C interface		$V_{DD}-V_{SS2}$	2.5	5.0	6.0	V
clock	$t_{HD;DAT} \geqslant$ 300 ns	$V_{DD}-V_{SS1}$	1.1	1.5	$V_{DD}-V_{SS2}$	V
Supply current						
V_{SS1} (pin 15)	$V_{DD}-V_{SS1}$ = 1.5 V	$-I_{SS1}$	–	3	10	μA
	$V_{DD}-V_{SS1}$ = 5 V	$-I_{SS1}$	–	12	50	μA
V_{SS2} (pin 8)	$V_{DD}-V_{SS2}$ = 5 V; I_O = 0 all outputs	$-I_{SS2}$	–	–	50	μA
Input SCL; input/output SDA						
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Leakage current	$V_I = V_{SS2}$ or V_{DD}	$\|I_L\|$	–	–	1	μA
Input capacitance		C_I	–	–	7	pF
Inputs A0, A1, TEST						
Input voltage LOW		V_{IL}	–	–	0.2 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Input leakage current	$V_I = V_{SS2}$ or V_{DD}	$\pm I_{LI}$	–	–	250	nA
Inputs EXTPF, PFIN						
Input voltage LOW		V_{IL}	0	–	0.2 $V_{DD}-V_{SS1}$	V
Input voltage HIGH		V_{IH}	0.7 $V_{DD}-V_{SS1}$	–	–	V
Input leakage current	$V_I = V_{SS1}$ to V_{DD} T_{amb} = 25 °C;	$\pm I_{LI}$	–	–	1.0	μA
	$V_I = V_{SS1}$ to V_{DD}	$\pm I_{LI}$	–	–	0.1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Output SDA						
(n channel open drain)						
Output "ON"	I_O = 3 mA; $V_{DD}-V_{SS2}$ = 2.5 to to 6 V	V_{OL}	–	–	0.4	V
Leakage current	$V_{DD}-V_{SS2}$ = 6 V; V_O = 6 V	$\|I_{LI}\|$	–	–	1	μA
Outputs						
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)						
Output voltage LOW	$V_{DD}-V_{SS2}$ = 2.5 V; I_O = 0.3 mA	V_{OL}	–	–	0.4	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; I_O = 1.6 mA	V_{OL}	–	–	0.4	V
Output voltage HIGH	$V_{DD}-V_{SS2}$ = 2.5 V; $-I_O$ = 0.1 mA	V_{OH}	$V_{DD}-0.4$	–	–	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; $-I_O$ = 0.5 mA	V_{OH}	$V_{DD}-0.4$	–	–	V
Internal threshold voltage						
Power failure detection		V_{TH1}	1	1.2	1.4	V
Power "ON" reset		V_{TH2}	1.5	2.0	2.5	V
Rise and fall times of input signals						
Input EXTPF		t_r, t_f	–	–	1	μs
Input PFIN		t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels						
rise time		t_r	–	–	1	μs
fall time		t_f	–	–	0.3	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator						
Integrated oscillator capacitance		C_{OUT}	–	40	–	pF
Oscillator feedback resistance		R_f	–	3	–	MΩ
Oscillator stability	$\Delta(V_{DD}-V_{SS1})$ = 100 mV; at $V_{DD}-V_{SS1}$ = 1.55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-7}	–	–
Quartz crystal parameters	f = 32.768 kHz					
Series resistance		R_S	–	–	40	kΩ
Parallel capacitance		C_L	–	10	–	pF
Trimmer capacitance		C_T	5	–	25	pF

APPLICATION INFORMATION

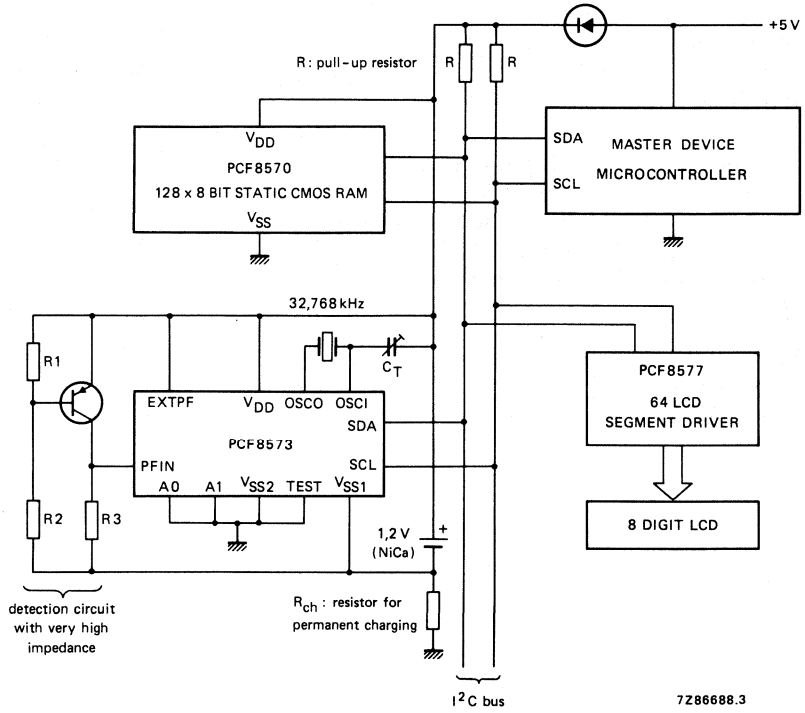


Fig.12 Application example of the PCF8573 clock/calendar.

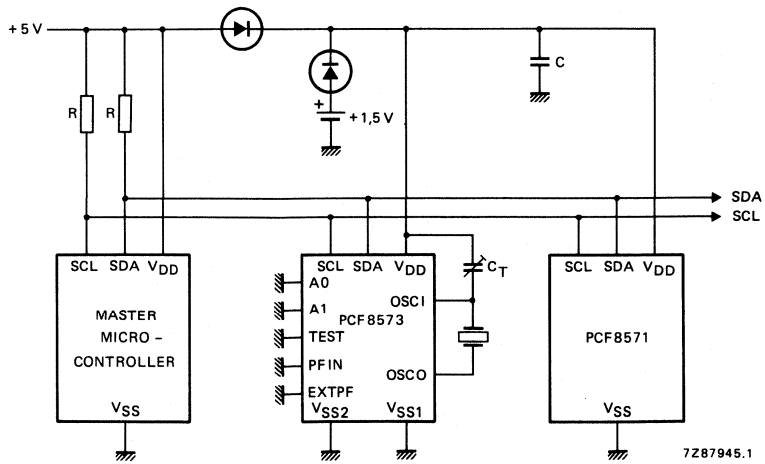


Fig.13 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

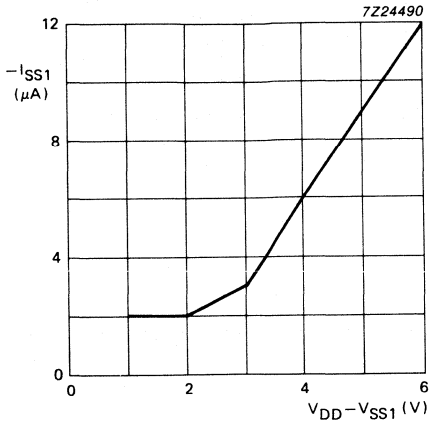


Fig. 14 Typical supply current ($-I_{SS1}$) as a function of clock supply voltage ($V_{DD}-V_{SS1}$) at $T_{amb} = -40$ to $+85$ °C.

REMOTE 8-BIT I/O EXPANDER FOR I²C-BUS

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF84CXX microcontroller families via the two-line serial bidirectional bus (I^2C).
It can also interface microcomputers without a serial interface to the I^2C-bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I^2C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I^2C-bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I^2C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and the PCF8574A versions differ only in their slave address as shown in Fig.9.

Features

- Operating supply voltage 2.5 V to 6 V
- Low stand-by current consumption max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I^2C-bus
- Peripheral for the MAB8400 and PCF84CXX microcontroller families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)

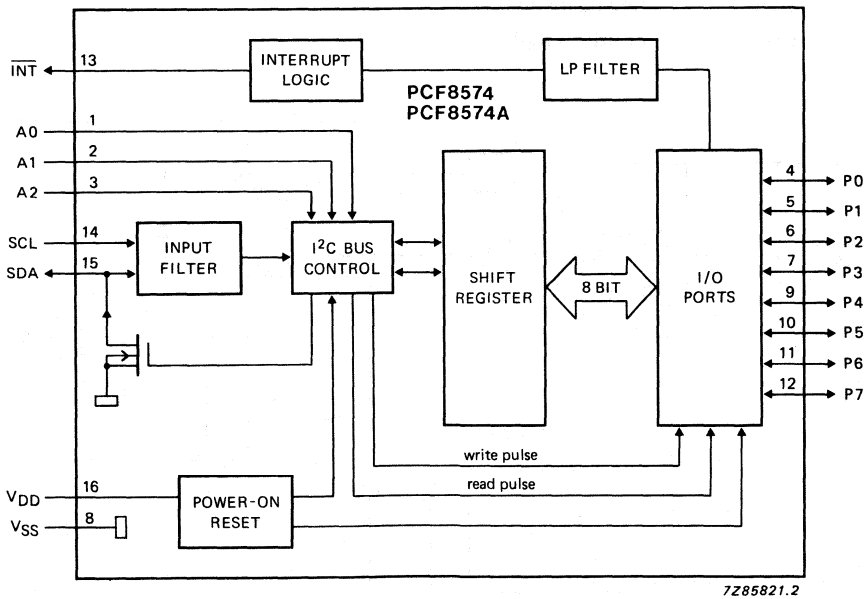


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8574P, PCF8574AP: 16-lead DIL; plastic (SOT38).
PCF8574T, PCF8574AT: 16-lead mini-pack; plastic (SO16L; SOT162A).

PINNING

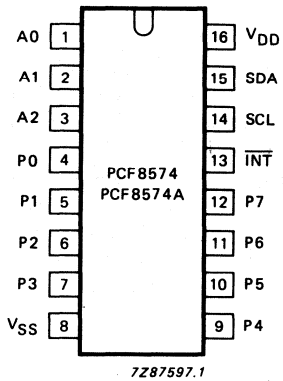


Fig.2 Pinning diagram.

1 to 3	A0 to A2	address inputs
4 to 7 9 to 12	P0 to P3 P4 to P7	8-bit quasi-bidirectional I/O port
8	V_{SS}	negative supply
13	$\overline{INT}$	interrupt output
14	SCL	serial clock line
15	SDA	serial data line
16	V_{DD}	positive supply

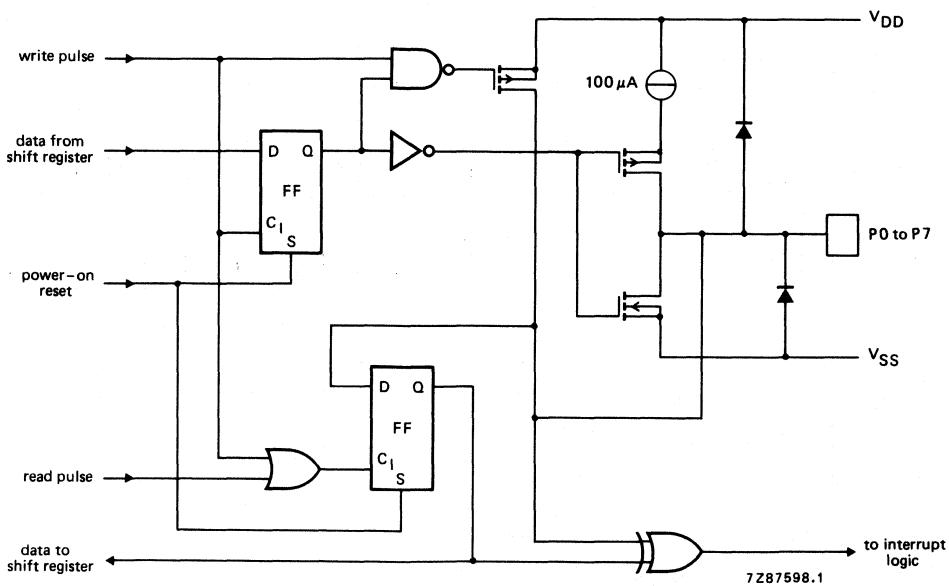


Fig.3 Simplified schematic diagram of each port.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

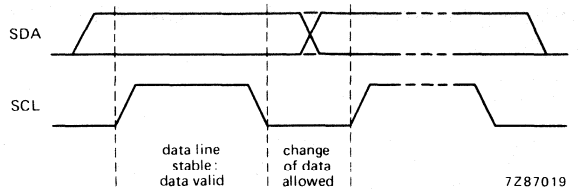


Fig.4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

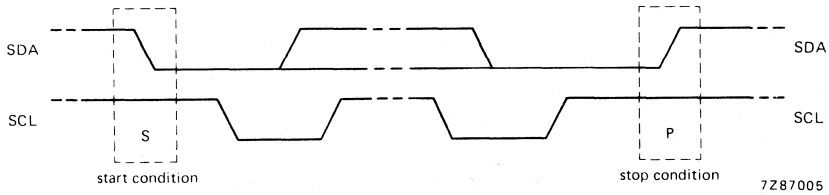


Fig.5 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

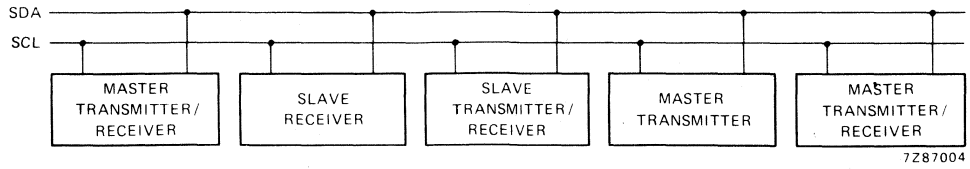


Fig.6 System configuration.

CHARACTERISTICS OF THE I²C-BUS (continued)

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

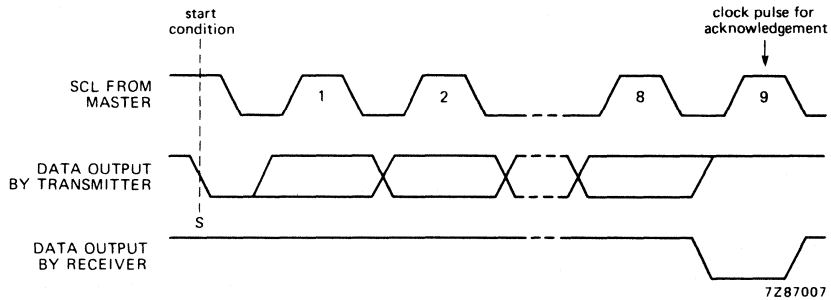


Fig.7 Acknowledgement on the I²C-bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4.7	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time	t_{LOW}	4.7	–	–	μs
SCL HIGH time	t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time	t_r	–	–	1.0	μs
SCL and SDA fall time	t_f	–	–	0.3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3.4	μs
Stop condition set-up time	$t_{SU;STO}$	4.0	–	–	μs

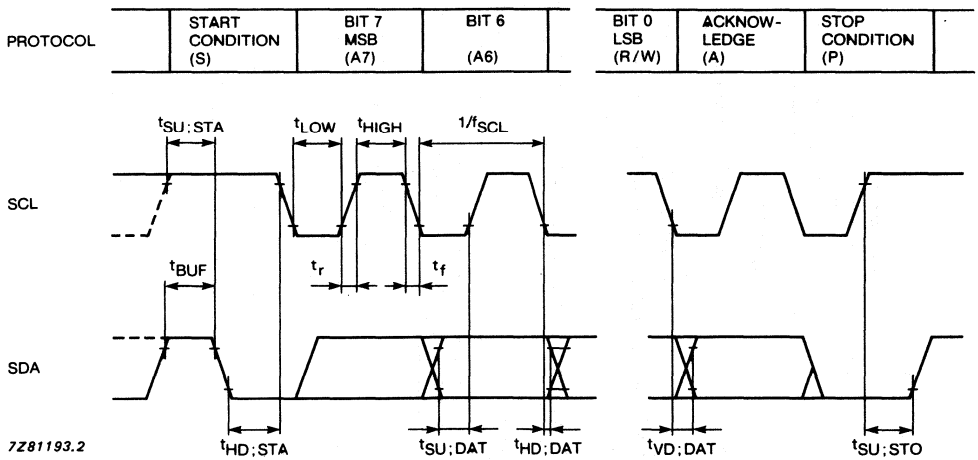
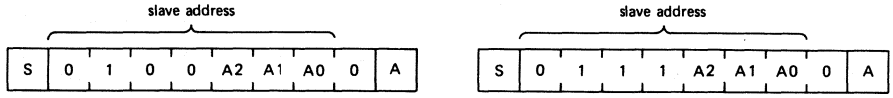


Fig.8 I²C-bus timing diagram.

FUNCTIONAL DESCRIPTION

Addressing (see Figs 9, 10 and 11)



(a) PCF8574. (b) PCF8574A.

Fig.9 PCF8574 and PCF8574A slave addresses.

Each bit of the PCF8574 I/O port can be independently used as an input or an output. Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

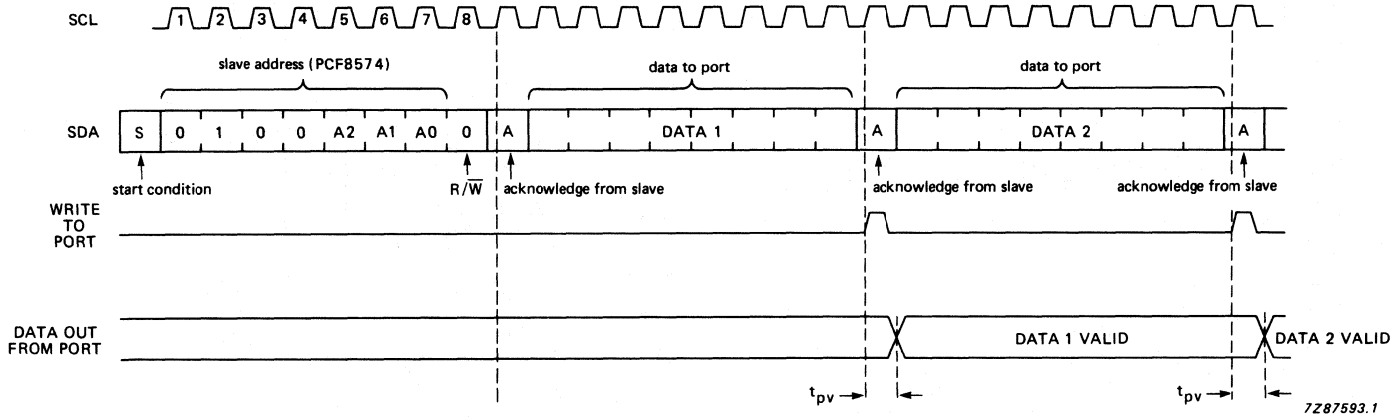


Fig.10 WRITE mode (output port).

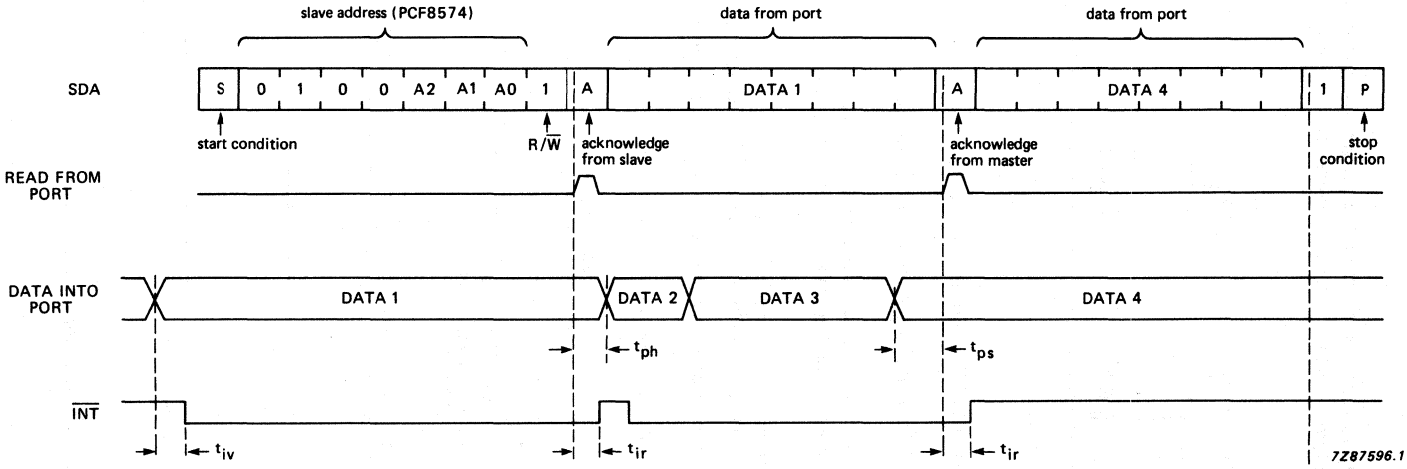


Fig.11 READ mode (input port).

Note

A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Interrupt (see Figs 12 and 13)

The PCF8574/PCF8574A provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

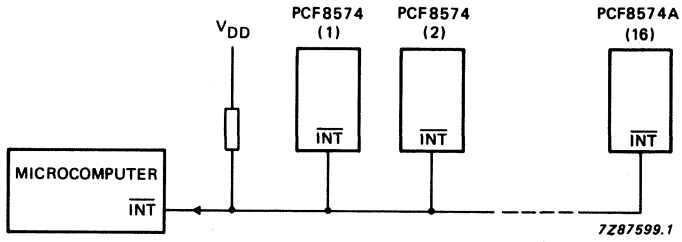


Fig.12 Application of multiple PCF8574s with interrupt.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.
Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.
Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.
Reading from or writing to another device does not affect the interrupt circuit.

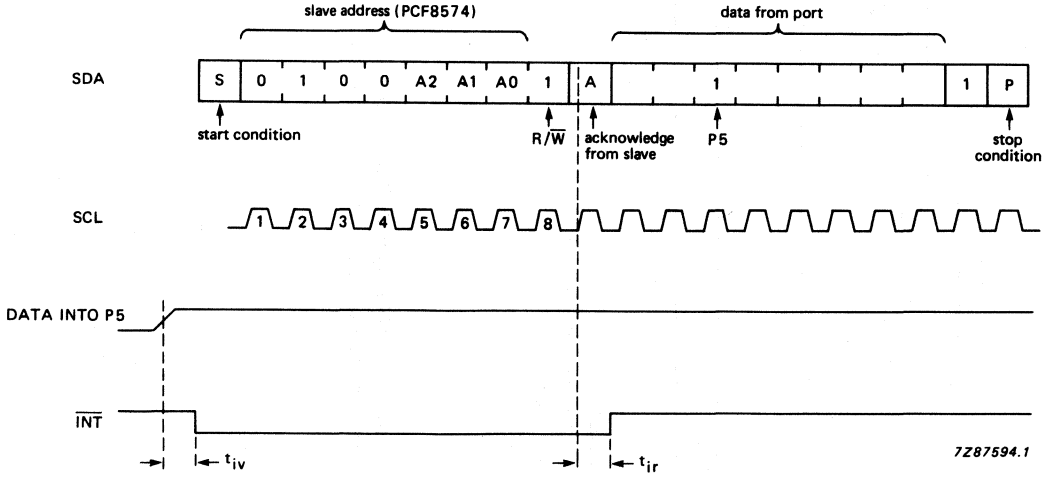


Fig.13 Interrupt generated by a change of input to port P5.

FUNCTIONAL DESCRIPTION (continued)

Quasi-bidirectional I/O ports (see Fig.14)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. At power-on the ports are HIGH. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The ports should be HIGH before being used as inputs.

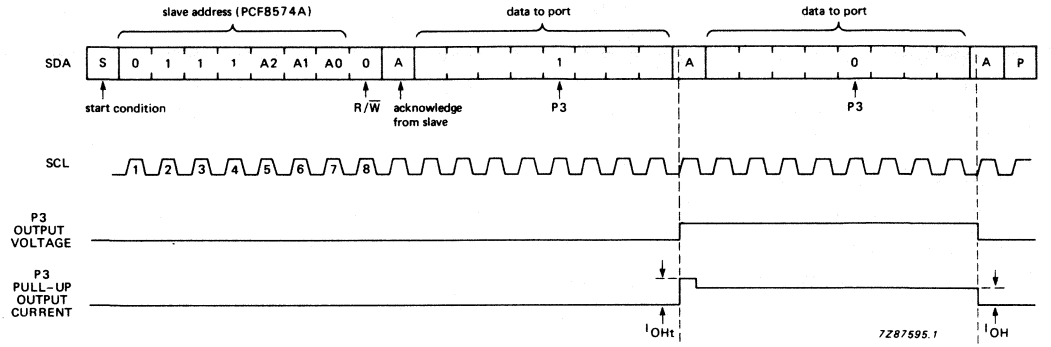


Fig.14 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+ 7.0	V
Input voltage range	V_I	V_{SS} −0.5	V_{DD} + 0.5	V
DC input current	$\pm I_I$	–	20	mA
DC output current	$\pm I_O$	–	25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; $\pm I_{SS}$	–	100	mA
Total power dissipation	P_{tot}	–	400	mW
Power dissipation per output	P_O	–	100	mW
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

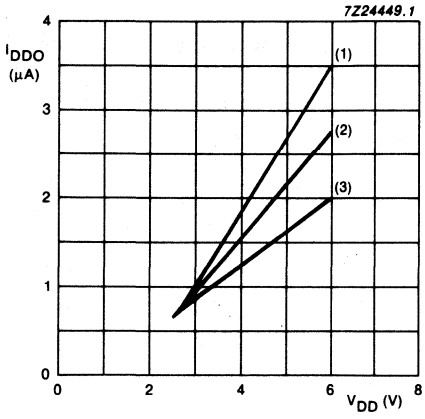
V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
Supply current	V_{DD} = 6 V; no load; $V_I = V_{DD}$ or V_{SS}					
operating	f_{SCL} = 100 kHz	I_{DD}	–	40	100	μA
standby		I_{DDO}	–	2.5	10	μA
Power-on reset level	note 1	V_{POR}	–	1.3	2.4	V
Input SCL; input/output SDA						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.5	V
Output current LOW	V_{OL} = 0.4 V	I_{OL}	3	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
Input capacitance (SCL, SDA)	$V_I = V_{SS}$	C_I	–	–	7	pF
I/O ports						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.5	V
Maximum allowed input current through protection diode	$V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$	$\pm I_{IHL}$	–	–	400	μA
Output current LOW	V_{OL} = 1 V; V_{DD} = 5 V	I_{OL}	10	25	–	mA
Output current HIGH	$V_{OH} = V_{SS}$	I_{OH}	30	–	300	μA
Transient pull-up current HIGH during acknowledge (see Fig.14)	$V_{OH} = V_{SS}$; V_{DD} = 2.5 V	$-I_{OHt}$	–	1	–	mA
Input/Output capacitance		$C_{I/O}$	–	–	10	pF
Port timing (see Figs 10 and 11)	$C_L = \leqslant 100$ pF					
Output data valid		t_{pv}	–	–	4	μs
Input data set-up		t_{ps}	0	–	–	μs
Input data hold		t_{ph}	4	–	–	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Interrupt $\overline{INT}$						
Output current LOW	V_{OL} = 0.4 V	I_{OL}	1.6	–	–	mA
Leakage current	$V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	1	μA
$\overline{INT}$ timing (see Figs 11 and 13)	$C_L \leqslant 100$ pF					
Input data valid		t_{iv}	–	–	4	μs
Reset delay		t_{ir}	–	–	4	μs
Select inputs A0, A1, A2						
Input voltage LOW		V_{IL}	−0.5	–	$0.3V_{DD}$	V
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	V_{DD} + 0.5	V
Input leakage current	pin at V_{DD} or V_{SS}	$\|I_L\|$	–	–	250	nA

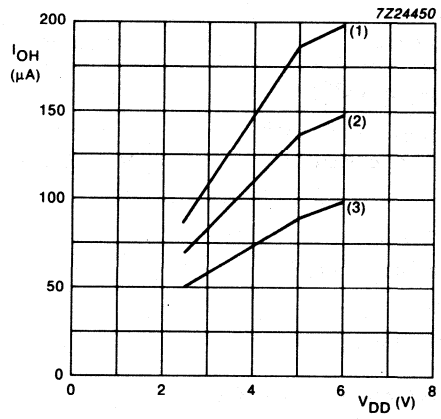
Note to the characteristics

1. The power-on reset circuit resets the I²C-bus logic with $V_{DD} < V_{POR}$ and sets all ports to logic 1 (with current source to V_{DD}).



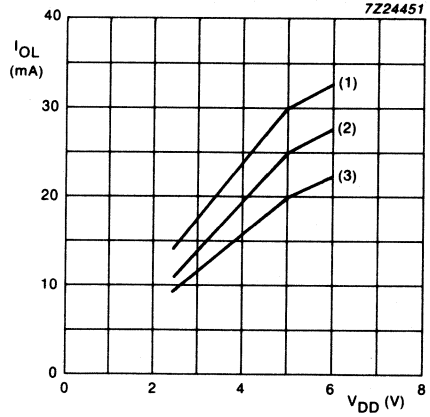
(1) $T_{amb} = -40\ ^{o}C$
(2) $T_{amb} = +25\ ^{o}C$
(3) $T_{amb} = +85\ ^{o}C$

Fig.15 Typical standby current (I_{DDO}) as a function of supply voltage (V_{DD}).



(1) $T_{amb} = -40\ ^{o}C$
(2) $T_{amb} = +25\ ^{o}C$
(3) $T_{amb} = +85\ ^{o}C$

Fig.16 Typical port output current HIGH (I_{OH}) as a function of supply voltage (V_{DD}); $V_{OH} = V_{SS}$.



(1) $T_{amb} = -40\ ^{o}C$
(2) $T_{amb} = +25\ ^{o}C$
(3) $T_{amb} = +85\ ^{o}C$

Fig.17 Typical port output current LOW (I_{OL}) as a function of supply voltage (V_{DD}); $V_{OL} = 1$ V.

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with the 24 segment LCD driver PCF8566
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO-56)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8576U: uncased chip in tray
PCF8576U/10: chip-on-film frame carrier (FFC)

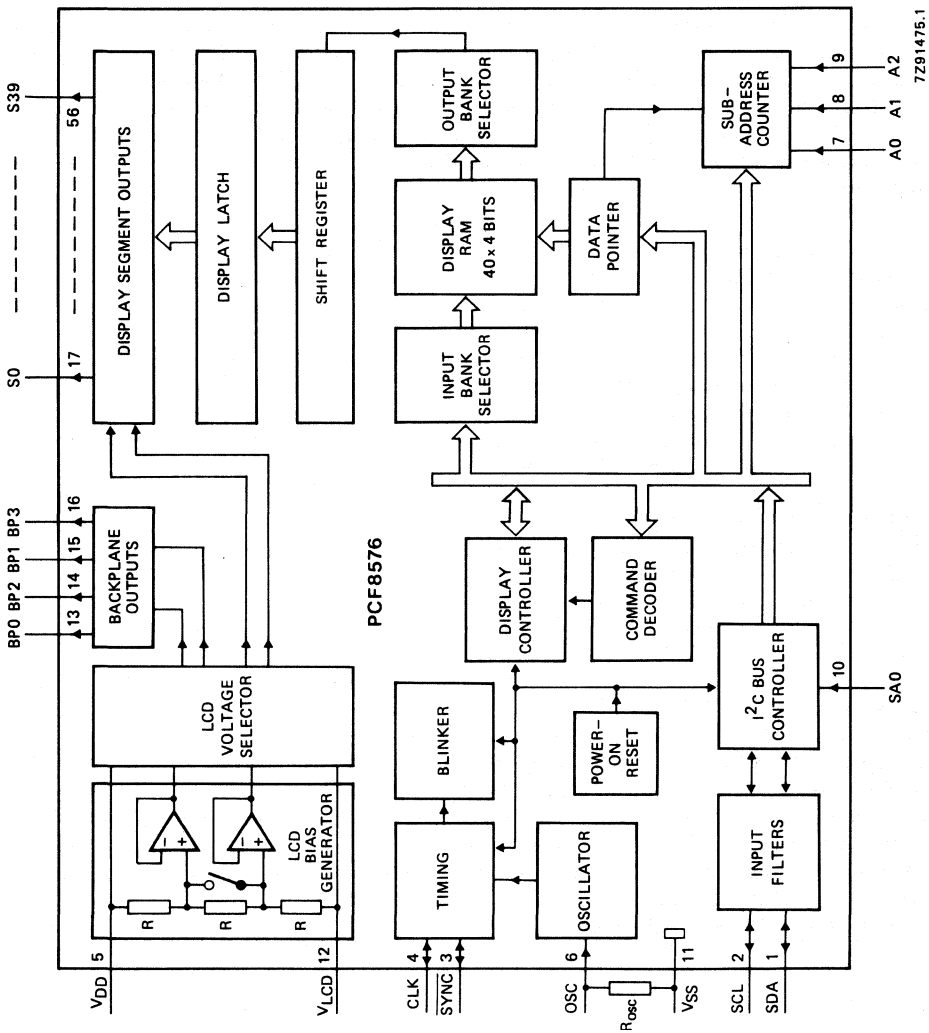


Fig. 1 Block diagram.

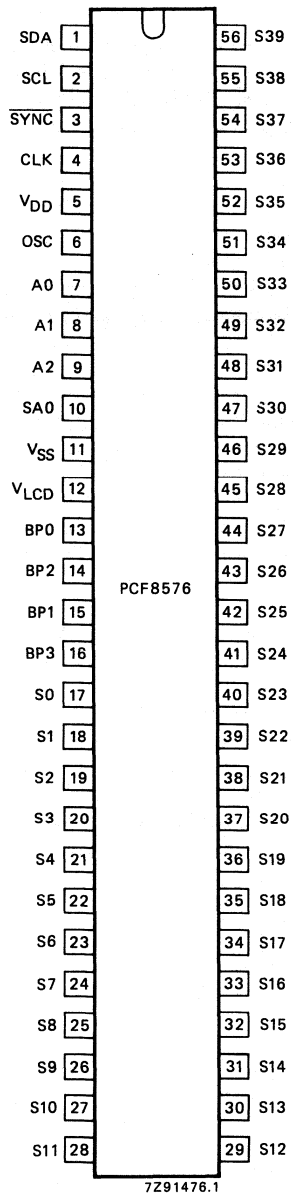


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17 to 56	S0 to S39	LCD segment outputs

FUNCTIONAL DESCRIPTION

The PCF8576 is a versatile peripheral device designed to interface any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active backplane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	160	20 digits + 20 indicator symbols	10 characters + 20 indicator symbols	160 dots (4 x 40)
3	120	15 digits + 15 indicator symbols	8 characters + 8 indicator symbols	120 dots (3 x 40)
2	80	10 digits + 10 indicator symbols	5 characters + 10 indicator symbols	80 dots (2 x 40)
1	40	5 digits + 5 indicator symbols	2 characters + 12 indicator symbols	40 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor/microcontroller maintains the 2-line I^2C bus communication channel with the PCF8576. A resistor connected between OSC (pin 6) and V_{SS} (pin 11) controls the device clock frequency. The appropiate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

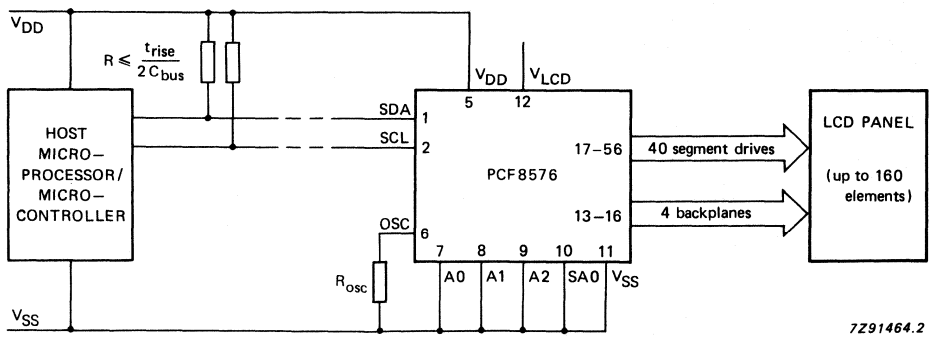


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8576 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\,V_{th}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex). The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\,V_{off(rms)} = 2{,}449\,V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\,V_{off(rms)} = 2{,}309\,V_{off(rms)}$

These compare with $V_{op} = 3\,V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

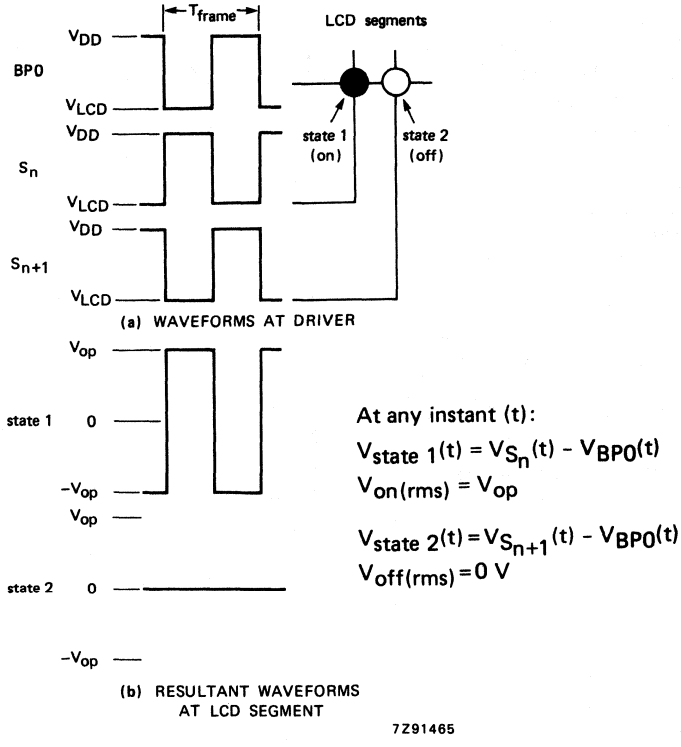


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8576 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

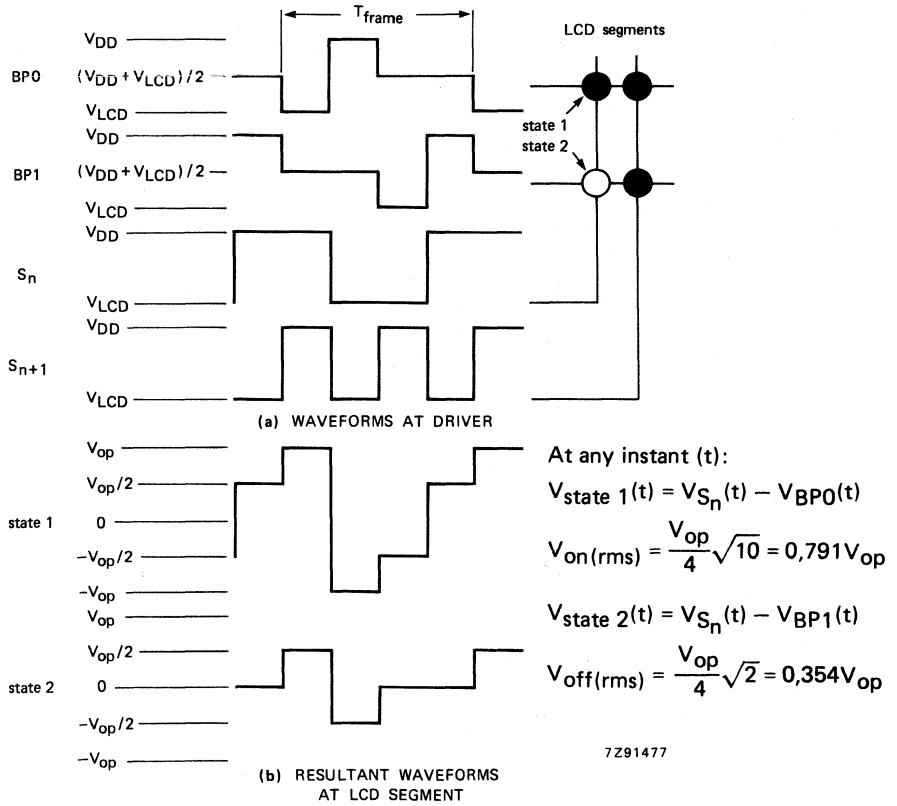


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

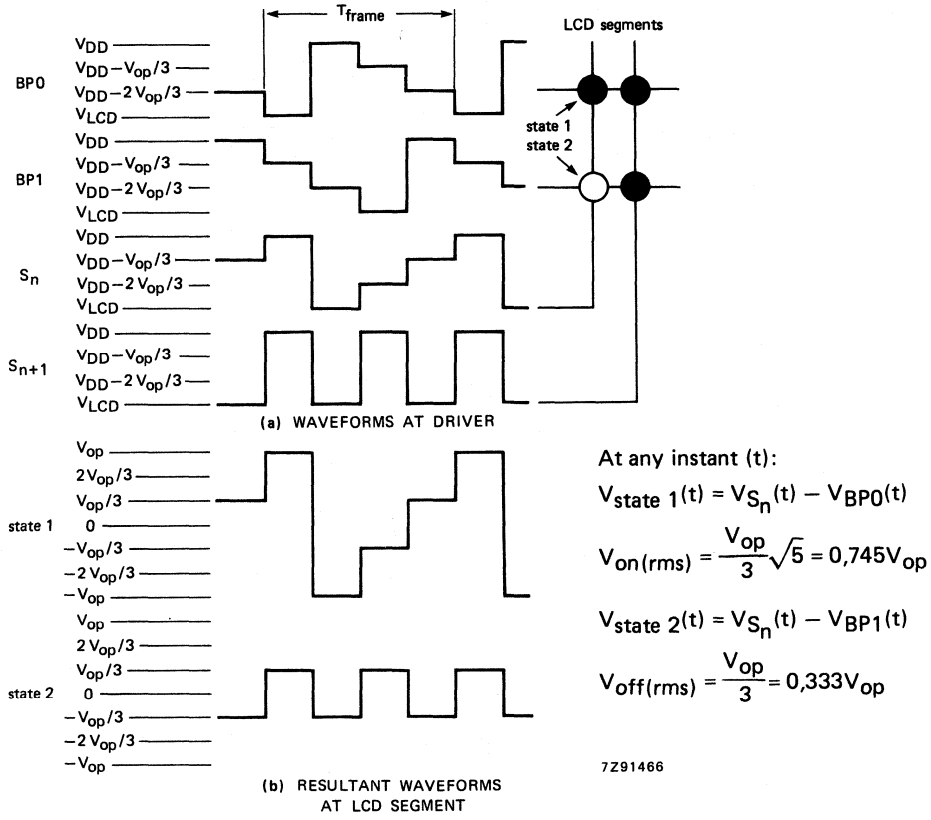


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive waveform for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

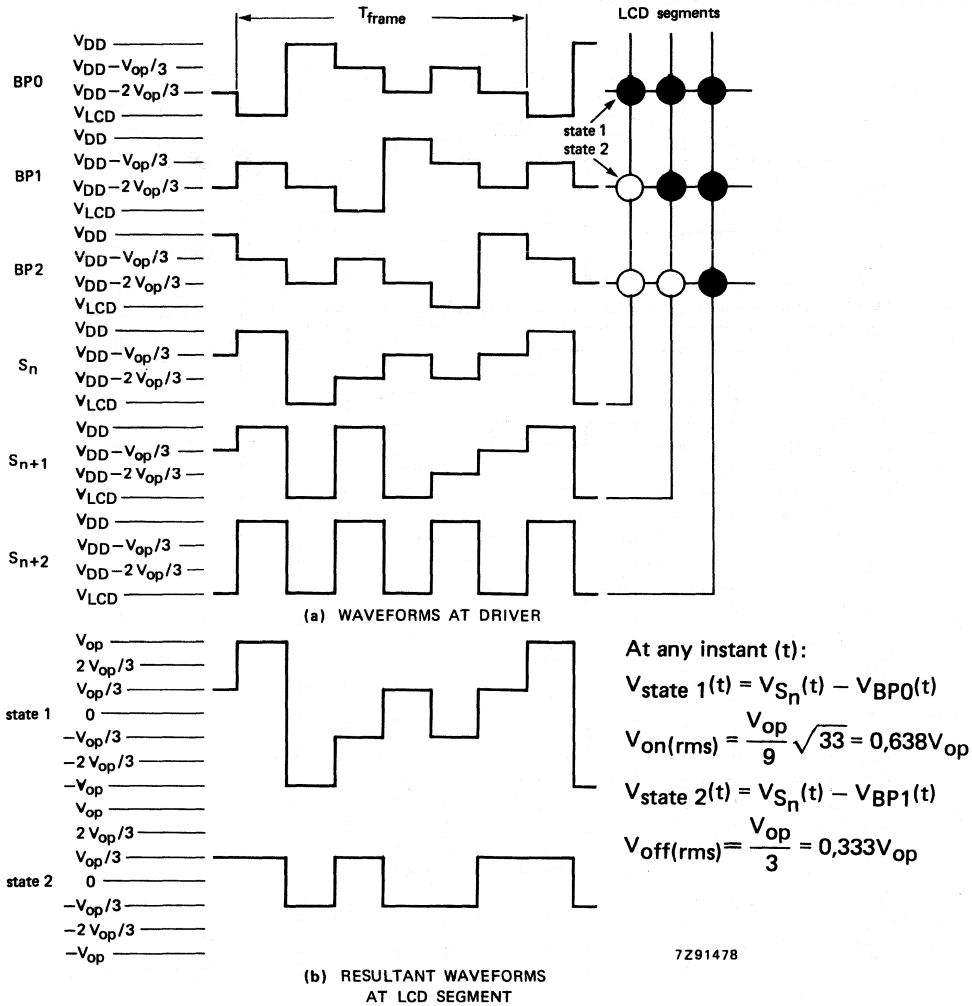


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

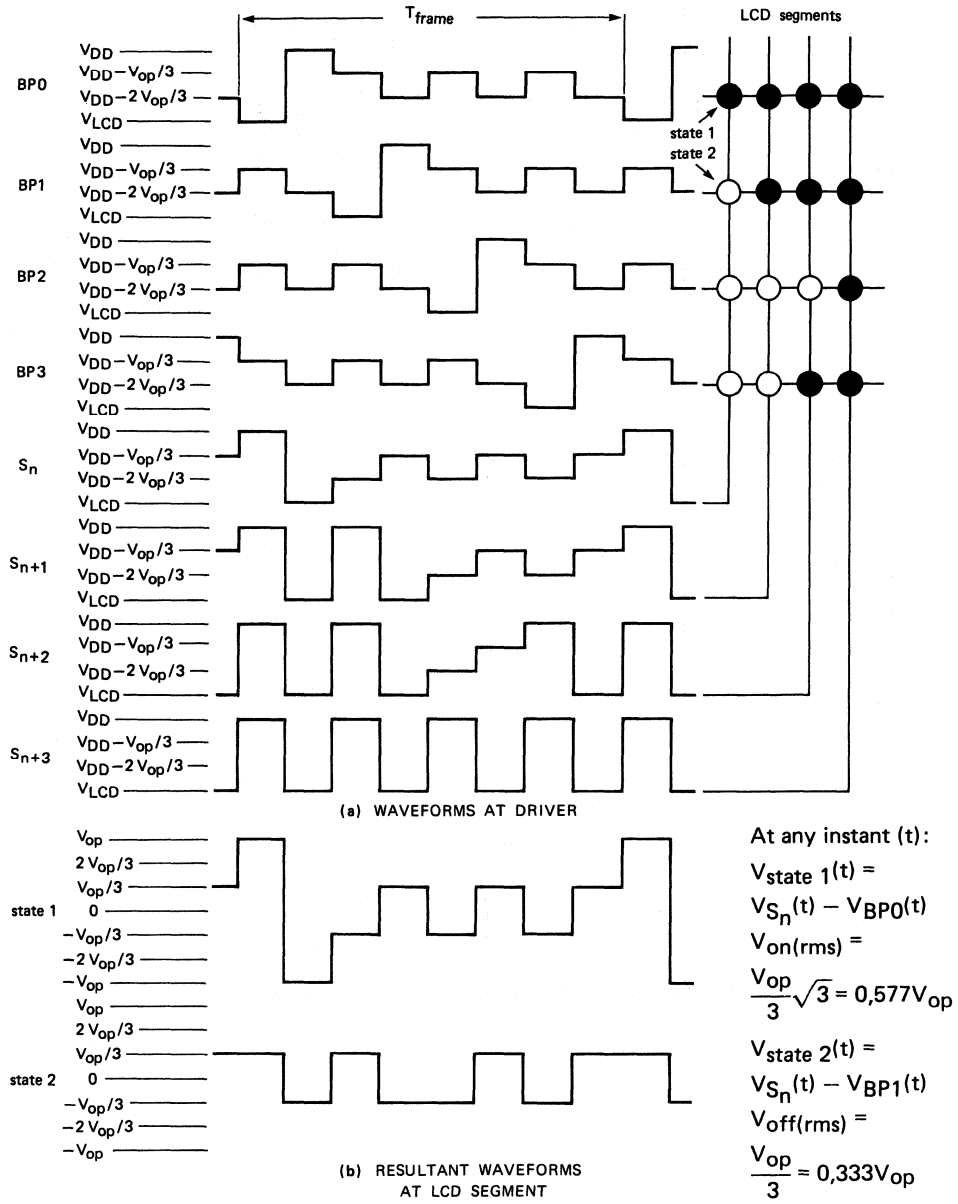


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

Internal clock

The internal logic and the LCD drive signals of the PCF8576 are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, frequency control is performed by a single resistor connected between OSC (pin 6) and V_{SS} (pin 11) as shown in Fig. 9. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8576s in the system.

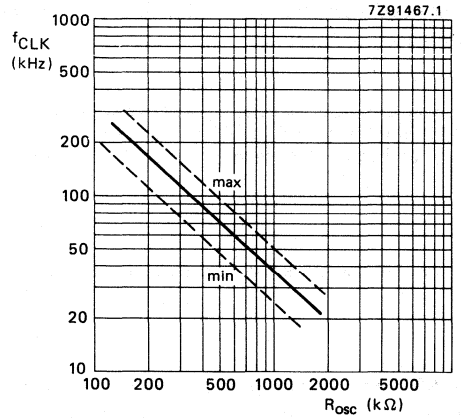


Fig. 9 Oscillator frequency as a function of R_{osc}: $f_{CLK} \approx (3{,}4 \times 10^7 / R_{osc})$ kHz·Ω.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I²C bus. To allow I²C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a d.c. state.

Timing

The timing of the PCF8576 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by the choice of value for R_{osc} when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8576 mode	recommended R_{osc} (kΩ)	f_{frame}	nominal f_{frame} (Hz)
normal mode	180	$f_{CLK}/2880$	64
power-saving mode	1200	$f_{CLK}/480$	64

Timing (continued)

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the normal mode, R_{OSC} = 180 kΩ will result in the nominal frame frequency. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six and for the same frame frequency R_{OSC} will be 1,2 MΩ. The reduced clock frequency and the increased value of R_{OSC} together contribute to a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 (pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 40 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (Fig. 10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

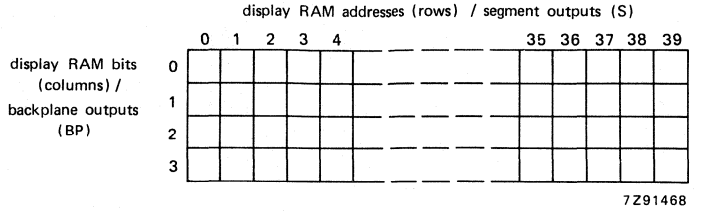


Fig. 10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8576 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 11. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

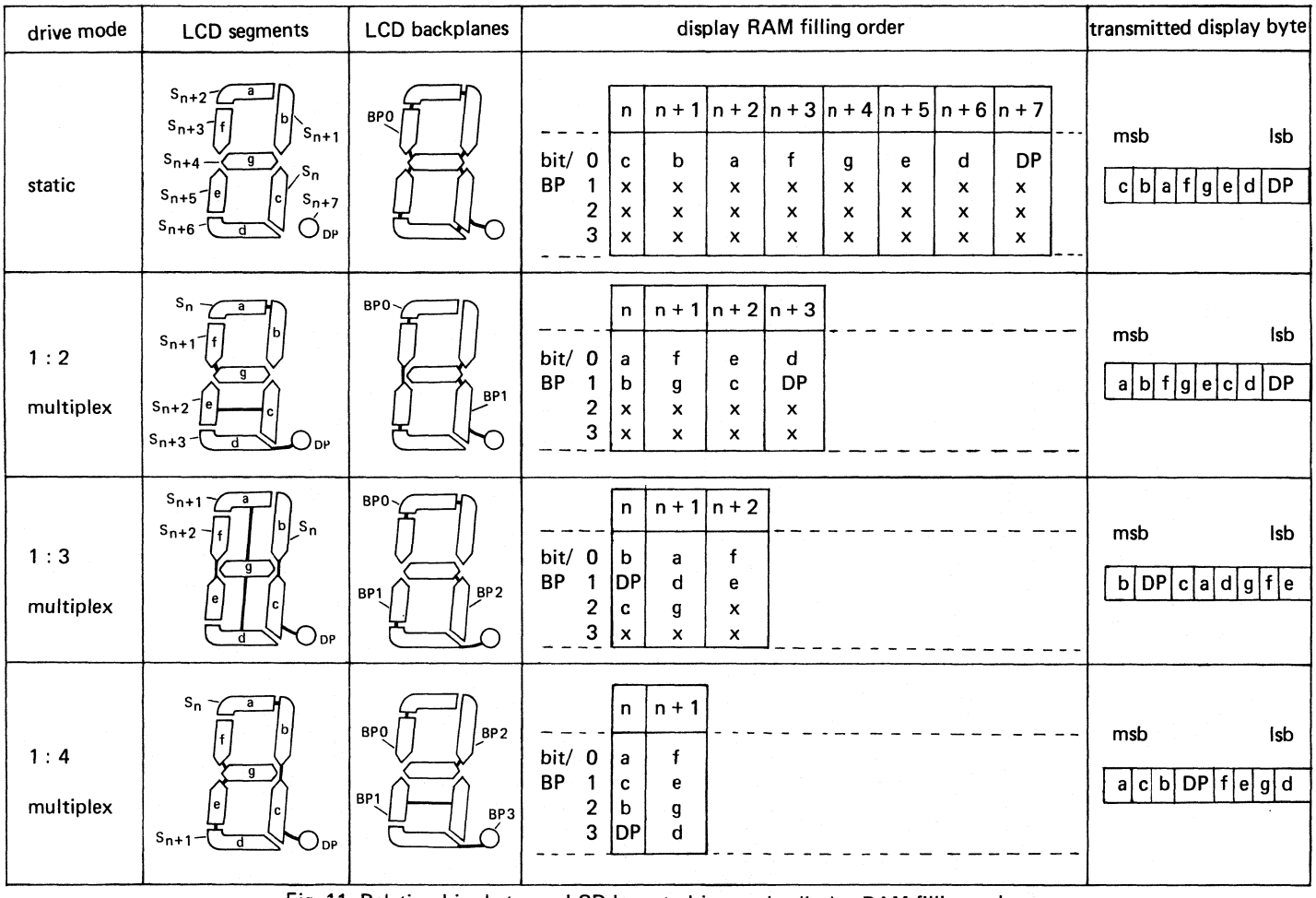


Fig. 11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

7Z91469

Subaddress counter (continued)

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8576 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8576 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Blinker (continued)

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

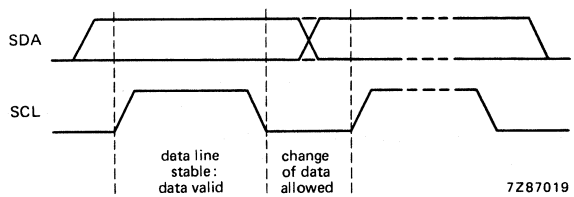


Fig. 12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

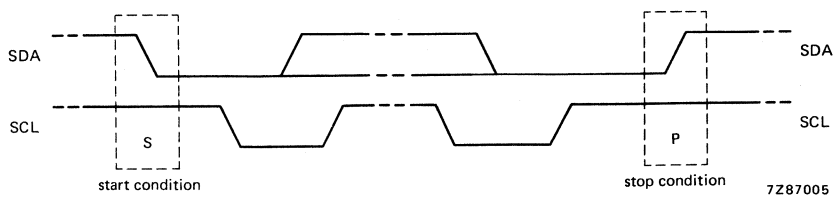


Fig. 13 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

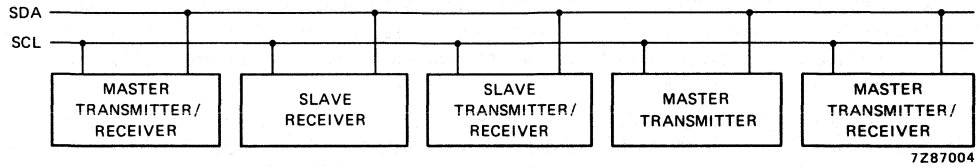


Fig. 14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

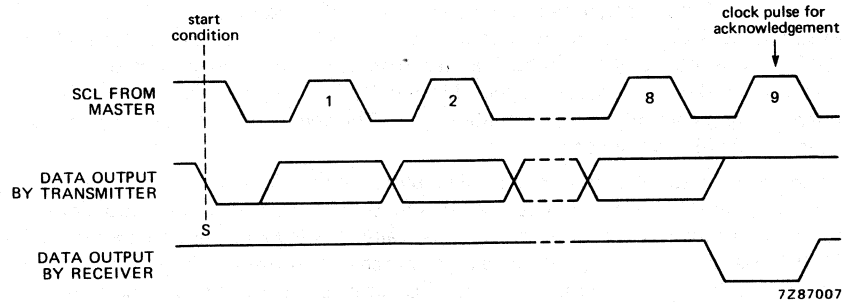


Fig. 15 Acknowledgement on the I^2C bus.

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

PCF8576 I²C bus controller

The PCF8576 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8576 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111000 and 0111001) are reserved for PCF8576. The least-significant bit of the slave address that a PCF8576 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8576 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8576s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 16. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8576 slave addresses available. All PCF8576s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8576s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8576 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8576. After the last display byte, the I²C bus master issues a stop condition (P).

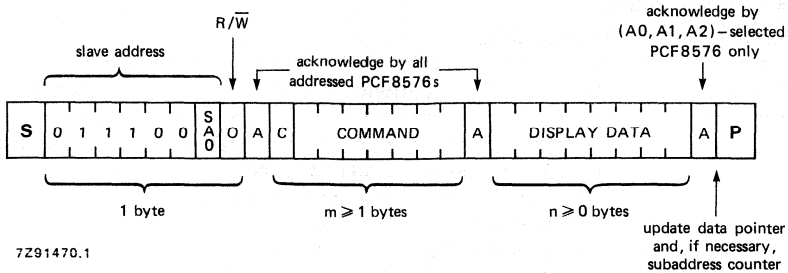


Fig. 16 I²C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I²C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

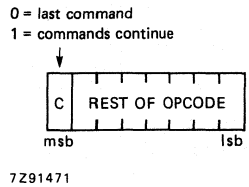


Fig. 17 General format of command byte.

The five commands available to the PCF8576 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8576 commands

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>MODE SET

C | 1 | 0 | LP | E | B | M1 | M0</td><td>
<table>
<tr><td>LCD drive mode</td><td>bits M1 M0</td></tr>
<tr><td>static (1 BP)
1 : 2 MUX (2 BP)
1 : 3 MUX (3 BP)
1 : 4 MUX (4 BP)</td><td>0 1
1 0
1 1
0 0</td></tr>
</table>
<table>
<tr><td>LCD bias</td><td>bit B</td></tr>
<tr><td>1/3 bias
1/2 bias</td><td>0
1</td></tr>
</table>
<table>
<tr><td>display status</td><td>bit E</td></tr>
<tr><td>disabled (blank)
enabled</td><td>0
1</td></tr>
</table>
<table>
<tr><td>mode</td><td>bit LP</td></tr>
<tr><td>normal mode
power-saving mode</td><td>0
1</td></tr>
</table>
</td><td>Defines LCD drive mode

Defines LCD bias configuration

Defines display status
The possibility to disable the display allows implementation of blinking under external control

Defines power dissipation mode</td></tr>
<tr><td>LOAD DATA POINTER

C | 0 | P5 P4 P3 P2 P1 P0</td><td>
<table>
<tr><td>bits P5 P4 P3 P2 P1 P0</td></tr>
<tr><td>6-bit binary value of 0 to 39</td></tr>
</table>
</td><td>Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses</td></tr>
<tr><td>DEVICE SELECT

C | 1 1 0 0 | A2 A1 A0</td><td>
<table>
<tr><td>bits A0 A1 A2</td></tr>
<tr><td>3-bit binary value of 0 to 7</td></tr>
</table>
</td><td>Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses</td></tr>
</table>

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>BANK SELECT
<table><tr><td>C</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>I</td><td>O</td></tr></table></td><td>
<table><tr><th>static</th><th>1 : 2 MUX</th><th>bit I</th></tr><tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr></table>
<table><tr><th>static</th><th>1 : 2 MUX</th><th>bit O</th></tr><tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr></table>
</td><td>Defines input bank selection (storage of arriving display data)

Defines output bank selection (retrieval of LCD display data)

The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td>BLINK
<table><tr><td>C</td><td>1</td><td>1</td><td>1</td><td>0</td><td>A</td><td>BF1</td><td>BF0</td></tr></table></td><td>
<table><tr><th>blink frequency</th><th>bits BF1</th><th>BF0</th></tr><tr><td>off</td><td>0</td><td>0</td></tr><tr><td>2 Hz</td><td>0</td><td>1</td></tr><tr><td>1 Hz</td><td>1</td><td>0</td></tr><tr><td>0,5 Hz</td><td>1</td><td>1</td></tr></table>
<table><tr><th>blink mode</th><th>bit A</th></tr><tr><td>normal blinking
alternation blinking</td><td>0
1</td></tr></table>
</td><td>Defines the blinking frequency

Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
</table>

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8576s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8576s. When cascaded, several PCF8576s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576s of the cascade contribute additional segment outputs but their backplane outputs are left open (Fig. 18).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8576s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576s with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8576 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8576 to assert $\overline{SYNC}$. The timing relationships between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576 are shown in Fig. 19.

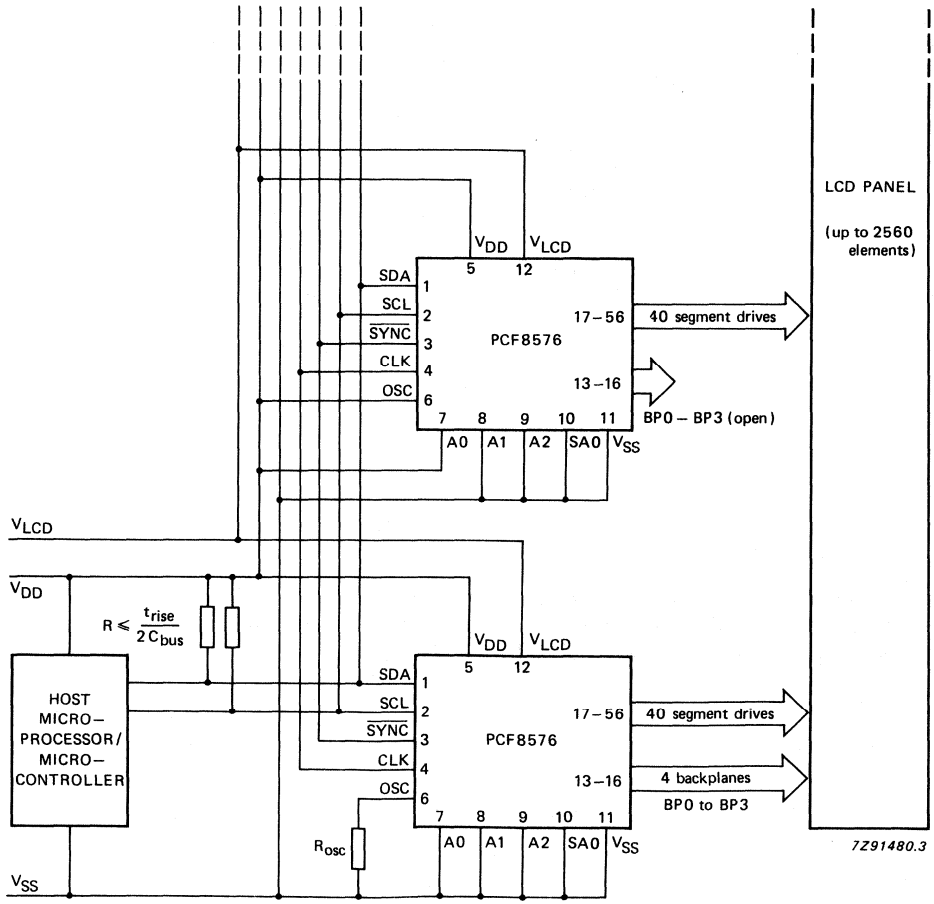
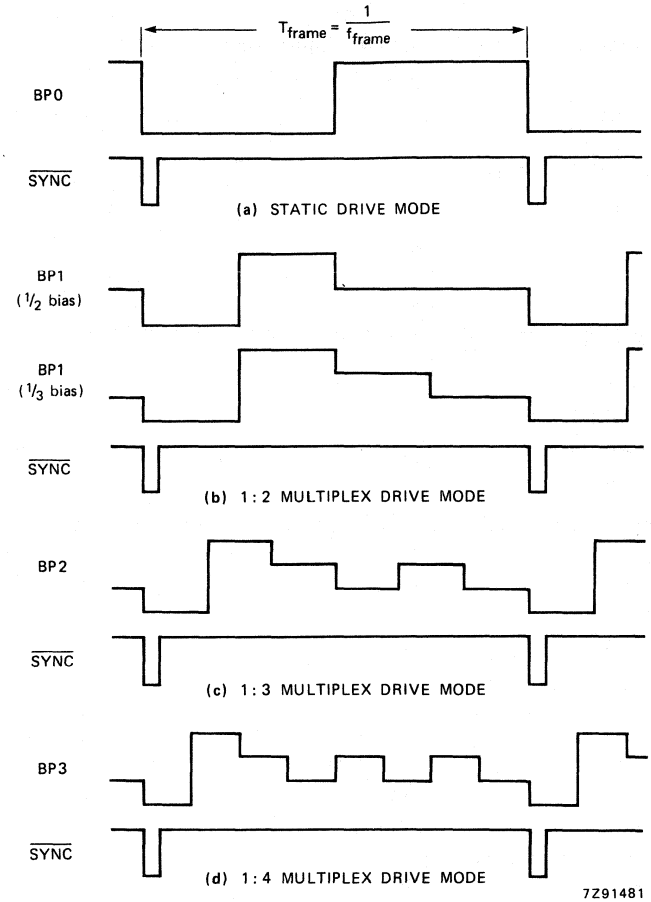


Fig. 18 Cascaded PCF8576 configuration.



Note

Excessive capacitive coupling between SCL or CLK and SYNC may cause erroneous synchronization. If this proves to be a problem, the capacitance of the $\overline{SYNC}$ line should be increased (e.g. by an external capacitor between $\overline{SYNC}$ and V_{DD}). Degradation of the positive edge of the $\overline{SYNC}$ pulse may be countered by an external pull-up resistor.

Fig. 19 Synchronization of the cascade for the various PCF8576 drive modes.

For single plane wiring of packaged PCF8576s and chip-on-glass cascading, see 'APPLICATION INFORMATION'.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to + 11	V
LCD supply voltage range	V_{LCD}		V_{DD}−11 to V_{DD}	V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5	V
Output voltage range (S0 to S39; BP0 to BP3)	V_O		V_{LCD}−0,5 to V_{DD} + 0,5	V
D.C. input current	$\pm I_I$	max.	20	mA
D.C. output current	$\pm I_O$	max.	25	mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50	mA
Power dissipation per package	P_{tot}	max.	400	mW
Power dissipation per output	P_O	max.	100	mW
Storage temperature range	T_{stg}		−65 to + 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2 to 9 V; V_{LCD} = V_{DD}−2 to V_{DD}−9 V;

T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2	–	9	V
LCD supply voltage (note 1)	V_{LCD}	V_{DD}−9	–	V_{DD}−2	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 2)	I_{DD}	–	–	180	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz (note 2)	I_{LP}	–	–	60	μA
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD}−0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	−1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0; A0 to A2; CLK; SCL; SDA) at V_I = V_{SS} or V_{DD}	$\pm I_{L1}$	–	–	1	μA

parameter	symbol	min.	typ.	max.	unit
Leakage current (OSC) at $V_I = V_{DD}$	$\pm I_{L2}$	–	–	1	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	20	50	150	kΩ
Power-on reset level (note 3)	V_{REF}	–	1,0	1,6	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 4)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S39) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_{BP}	–	–	5	kΩ
Output impedance (S0 to S39) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_S	–	–	7,0	kΩ

A.C. CHARACTERISTICS (note 6)

V_{SS} = 0 V; V_{DD} = 2 to 9 V; $V_{LCD} = V_{DD}-2$ to $V_{DD}-9$ V;

$T_{amb} = -40$ to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V; R_{osc} = 180 kΩ (note 7)	f_{CLK}	125	185	288	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V; R_{osc} = 1,2 MΩ	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at $V_{LCD} = V_{DD}-5$ V	t_{PLCD}	–	–	30	μs

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
I²C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_R	–	–	1	μs
Fall time	t_F	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

Notes to characteristics

1. $V_{LCD} \leqslant V_{DD}-3$ V for 1/3 bias.
2. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
3. Resets all logic when $V_{DD} < V_{REF}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.
6. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
7. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

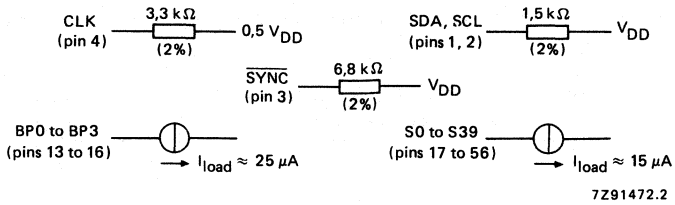


Fig. 20 Test loads.

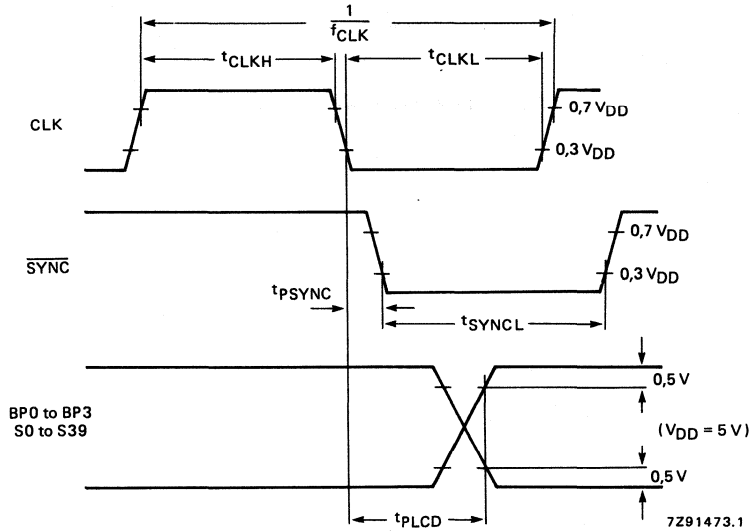


Fig. 21 Driver timing waveforms.

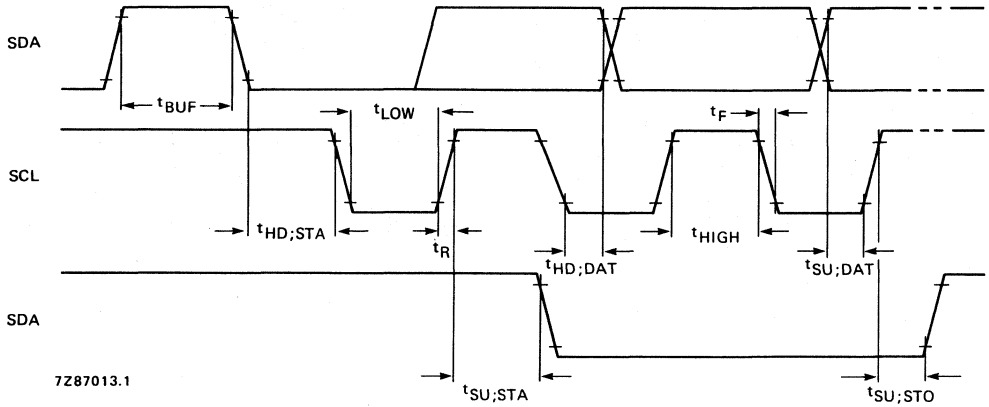
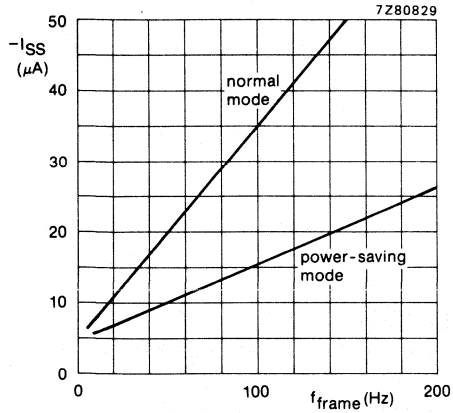
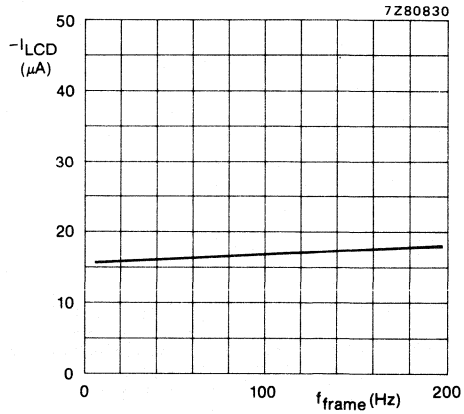


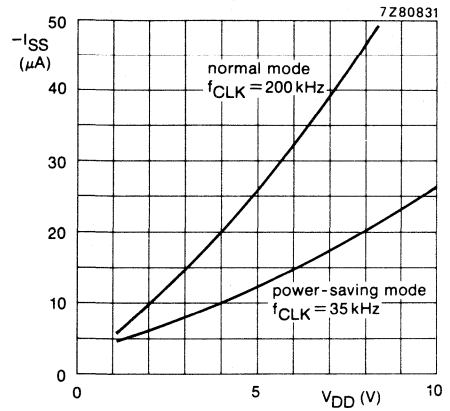
Fig. 22 I²C bus timing waveforms.



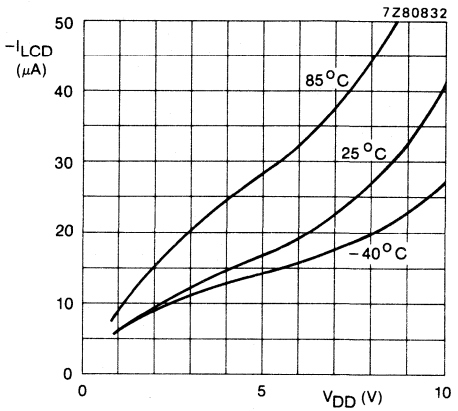
(a) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

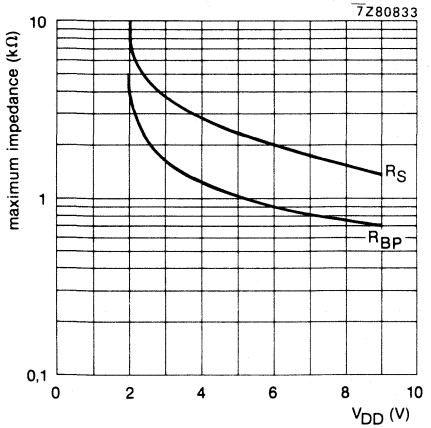


(c) V_{LCD} = 0 V; external clock; T_{amb} = −40 to + 85 °C.

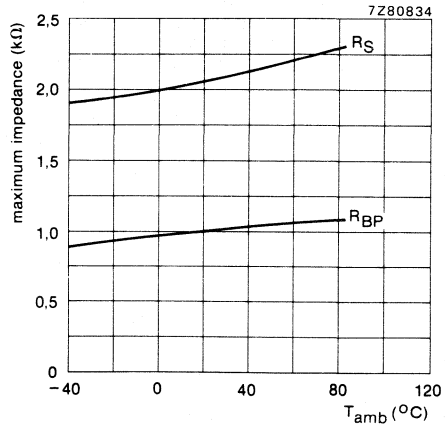


(d) V_{LCD} = 0 V; external clock; f_{CLK} = nominal frequency.

Fig. 23 Typical supply current characteristics.



(a) V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V.

Fig. 24 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

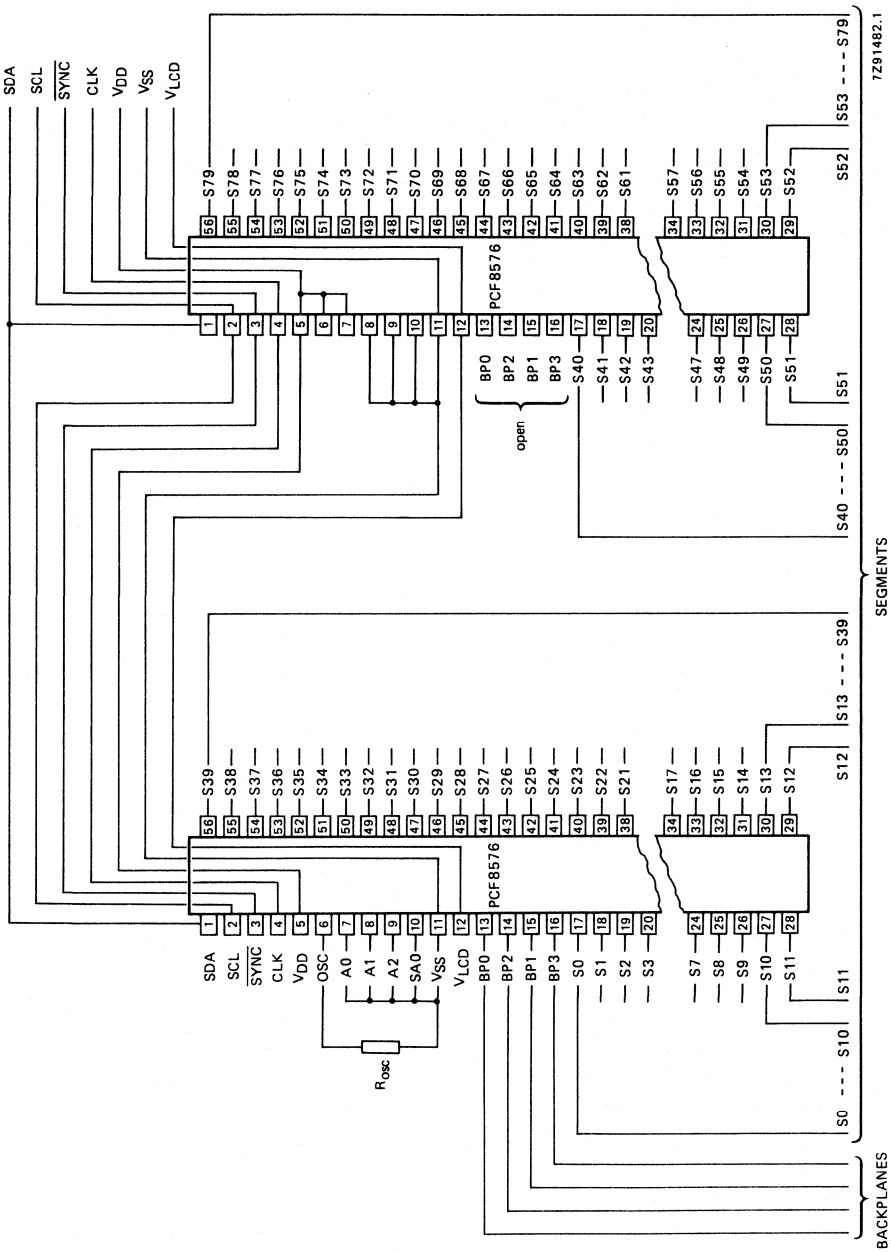


Fig. 25 Single plane wiring of packaged PCF8576s.

Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto the glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576 bonding pad layout (Fig. 26). Pads needing bus interconnection between all PCF8576s of the cascade are V_{DD}, V_{SS}, V_{LCD}, CLK, SCL, SDA and $\overline{SYNC}$. These lines may be led to the corresponding pads of the next PCF8576 through the wide opening between the V_{LCD} pad and the backplane output pads. The only bussed line that does not require a second opening to lead through to the next PCF8576 is V_{LCD}, being the cascade centre. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be tied together.

Fig. 27 shows the connection diagram for a cascaded PCF8576 application with single plane wiring. Note the use of the open space between the V_{LCD} pad and the backplane output pads to route V_{DD}, V_{SS}, CLK, SCL, SDA and $\overline{SYNC}$. The external connections may be made to either end of the cascade, wherever most convenient for the connector.

When an external clocking source is to be used, OSC of all devices should be tied to V_{DD}. The pads OSC, A0, A1, A2 and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress and slave address.

APPLICATION INFORMATION (continued)

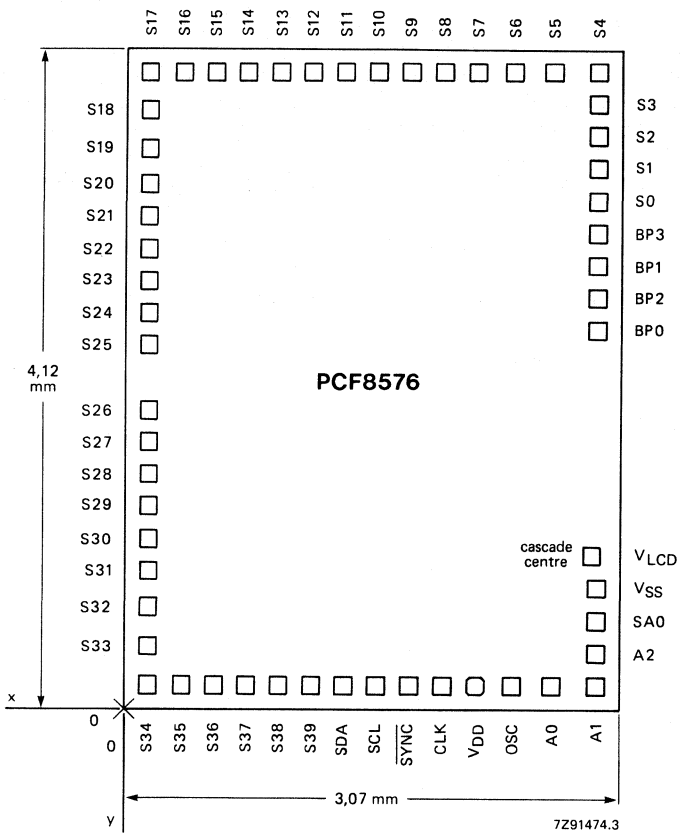


Fig. 26 PCF8576 bonding pad locations.

Bonding pad locations

All x/y coordinates are referenced to left-hand bottom corner (0/0, Fig. 26).

Dimensions in μm

pad	x	y	
S34	160	160	bottom
S35	380		
S36	580		
S37	780		
S38	980		
S39	1180		
SDA	1380		
SCL	1580		
$\overline{\text{SYNC}}$	1780		
CLK	1980		
V_{DD}	2180		
OSC	2400		
A0	2640		
A1	2910	160	bottom
S17	160	3960	top
S16	380		
S15	580		
S14	780		
S13	980		
S12	1180		
S11	1380		
S10	1580		
S9	1780		
S8	1980		
S7	2180		
S6	2400		
S5	2640		
S4	2910	3960	top

pad	x	y	
S33	160	400	left
S32		640	
S31		860	
S30		1060	
S29		1260	
S28		1460	
S27		1660	
S26		1860	
S25		2260	
S24		2460	
S23		2660	
S22		2860	
S21		3060	
S20		3260	
S19		3480	
S18	160	3720	left
A2	2910	360	right
SA0		560	
V_{SS}	2910	760	
V_{LCD}	2880	960	
BP0	2910	2360	
BP2		2560	
BP1		2760	
BP3		2960	
S0		3160	
S1		3360	
S2		3560	
S3	2910	3760	right

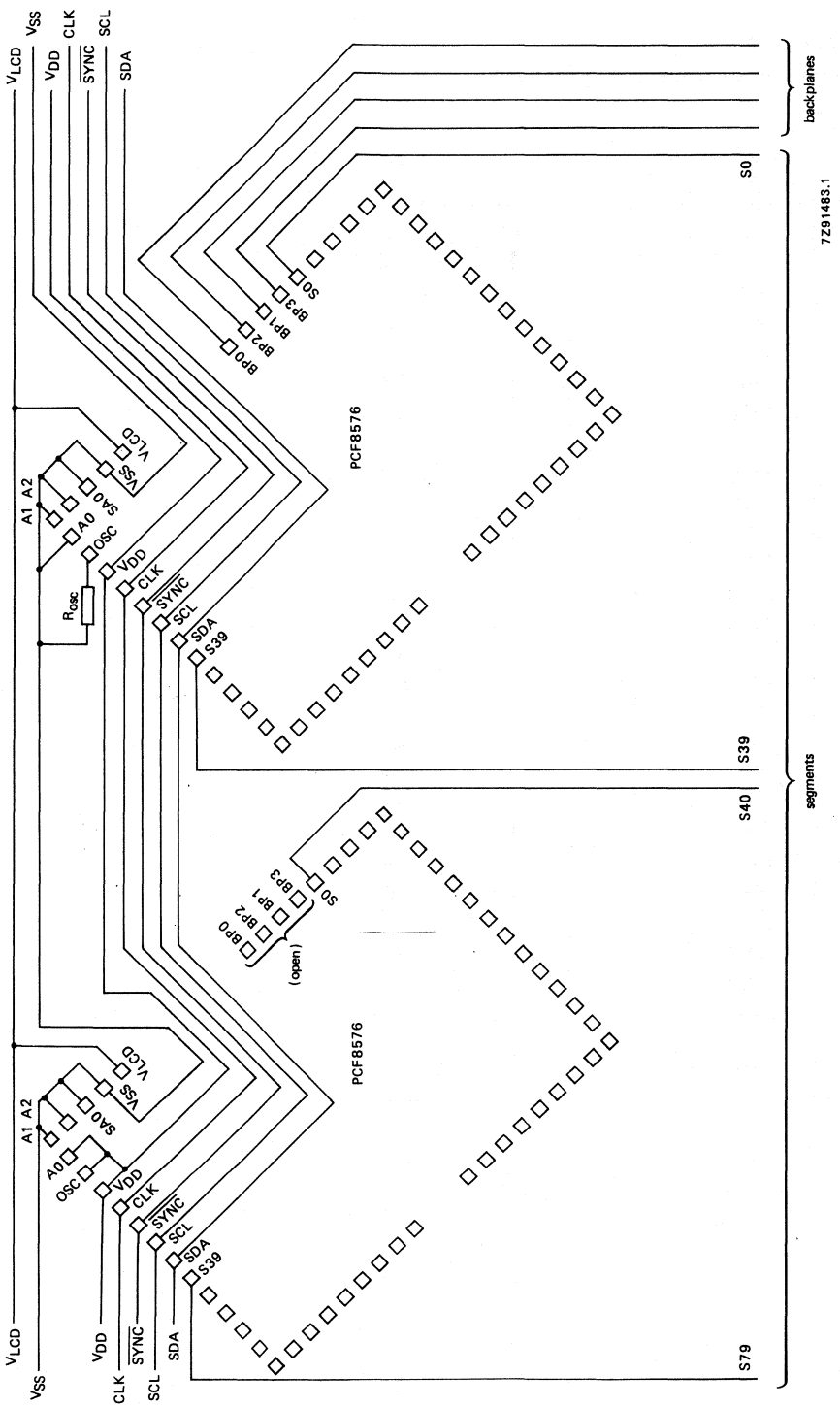


Fig. 27 Chip-on-glass application; cascaded PCF8576s with single-plane wiring (viewed from back of chip).

LCD DIRECT/DUPLEX DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).

The PCF8577 and PCF8577A differ only in their slave addresses.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2.5 to 9 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A)
- Power-on-reset blanks display

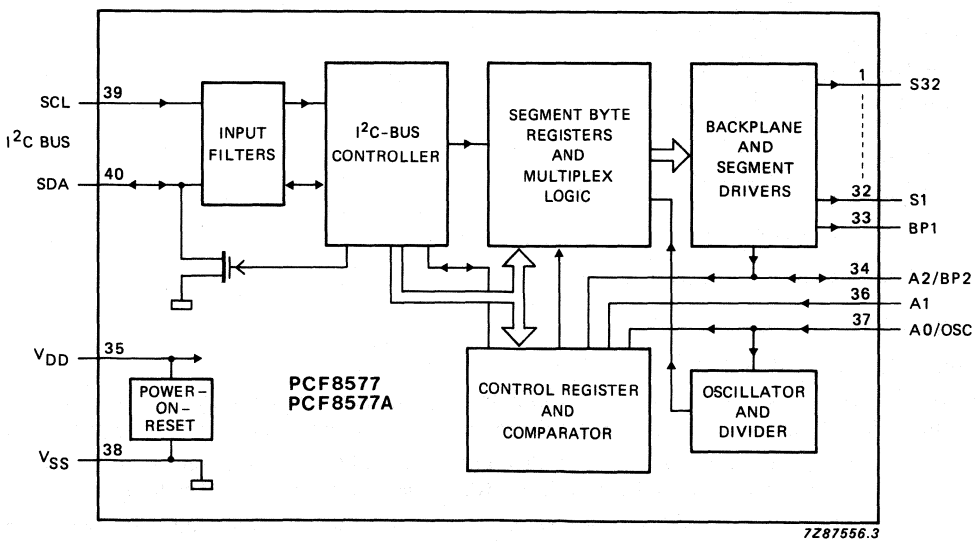


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8577P, PCF8577AP: 40-lead DIL; plastic (SOT129).
PCF8577T, PCF8577AT: 40-lead mini-pack; plastic (VSO40; SOT158A).
PCF8577T, PCF8577AT: in blister tape.
PCF8577U/5, PCF8577AU/5: wafer unsawn.
PCF8577U/10, PCF8577AU/10: chip-on-film frame carrier (FFC).

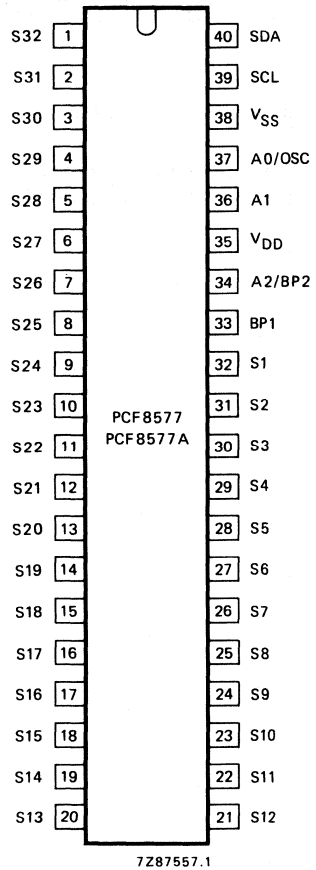


Fig.2 Pinning diagram.

PINNING

Supply

35	V_{DD}	positive supply
38	V_{SS}	negative supply

I^2C-bus

40	SDA	I^2C-bus data line
39	SCL	I^2C-bus clock line

Inputs

36	A1	hardware address line
37	A0/OSC	hardware address line/oscillator pin

Outputs

1 – 32	S32 – S1	segment outputs

Input – Output

34	A2/BP2	harware address line/cascade sync input/backplane output
33	BP1	cascade sync input/backplane output

FUNCTIONAL DESCRIPTION

Hardware subaddress A0, A1, A2

The hardware subaddress lines A0, A1, A2 are used to program the device subaddress for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

A0/OSC Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.

A1 Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.

A2/BP2 In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.

In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

Oscillator A0/OSC

The PCF8577 has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator. In an expanded system containing more than one PCF8577 the backplane signals are usually common to all devices and only one oscillator is needed. The devices which are not used for the oscillator are put into the cascade mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the cascade mode each PCF8577 is synchronized from the backplane signal(s).

User-accessible registers

There are nine user-accesible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even numbered segment byte registers is called BANK A. Odd numbered segment byte registers are called BANK B.

There are two slave addresses, one for PCF8577, and one for PCF8577A (see Fig.6). All addressed devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register at all times (see I²C-bus protocol Fig.7), i.e. all addressed devices respond to control commands sent on the bus.

The control register is shown in more detail in Fig.3. The least-significant bits select which device and which segment byte register is loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware subaddress input signals A2, A1 and A0. If they are the same then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

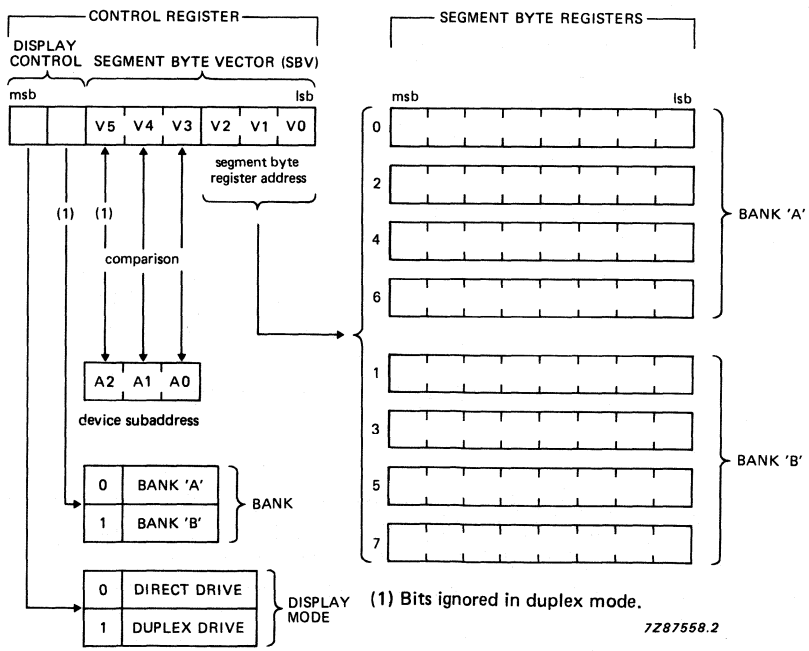


Fig.3 PCF8577 register organization.

FUNCTIONAL DESCRIPTION (continued)

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

Auto-incremented loading

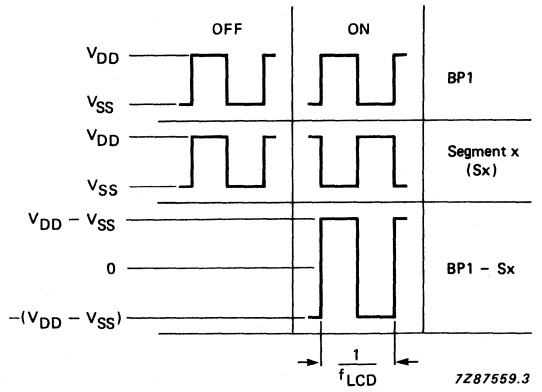
After each segment byte is loaded the SBV is incremented automatically. Thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers in all addressed chips, auto-incremented loading may proceed across device boundaries provided that the hardware subaddresses are arranged contiguously.

Direct drive mode

The PCF8577 is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode only four bytes are needed to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A); setting the BANK bit to logic 1 selects odd bytes (BANK B).

In the direct drive mode the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in Fig.4.



$V_{on(rms)} = V_{DD} - V_{SS}$
$V_{off(rms)} = 0$

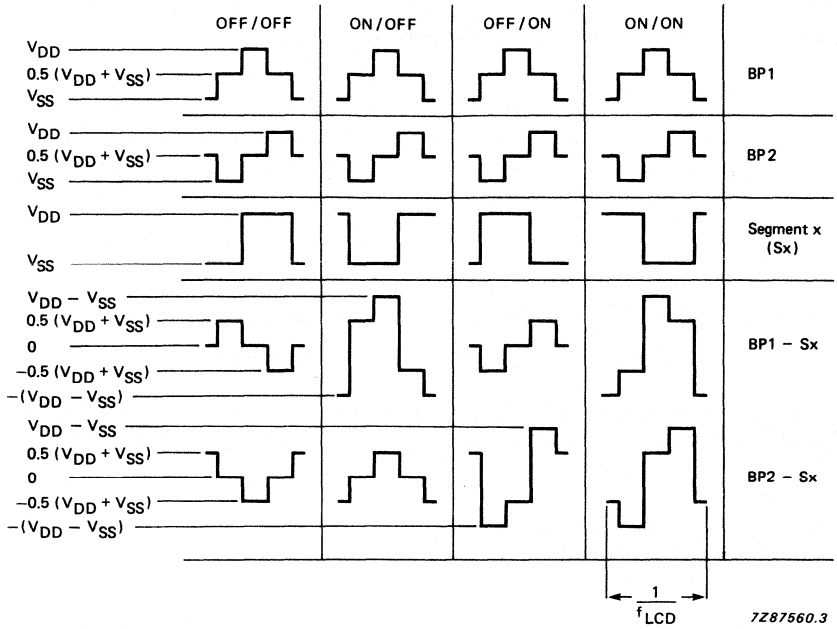
Fig.4 Direct drive mode display output waveforms.

Duplex mode

The PCF8577 is set to the duplex mode by loading the MODE bit with logic 1. In this mode a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are needed to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in Fig.5.



$$V_{on(rms)} = 0.791\,(V_{DD} - V_{SS})$$
$$V_{off(rms)} = 0.354\,(V_{DD} - V_{SS})$$
$$\frac{V_{on(rms)}}{V_{off(rms)}} = 2.236$$

Fig.5 Duplex mode display output waveforms.

Power-on reset

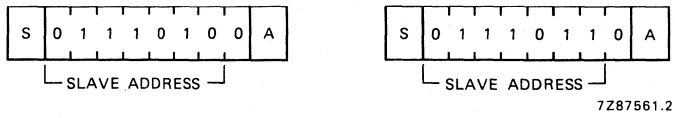
At power-on reset the PCF8577 resets to a defined starting condition as follows:

1. Both backplane outputs are set to V_{SS} in master mode; to 3-state in cascade mode.
2. All segment outputs are set to V_{SS}.
3. The segment byte registers and control register are cleared.
4. The I²C-bus interface is initialized.

DEVELOPMENT DATA

Slave address

The slave address for PCF8577 and PCF8577A are shown in Fig.6.



(a) PCF8577 (b) PCF8577A

Fig.6 PCF8577 and PCF8577A slave addresses.

Before any data is transmitted on the I^2C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

I^2C-bus protocol

The PCF8577 I^2C-bus protocol is shown in Fig.7.

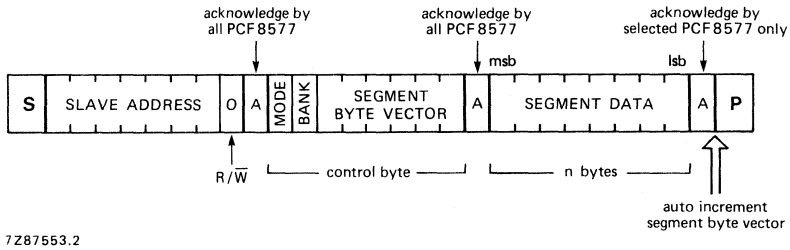


Fig.7 I^2C-bus protocol.

The PCF8577 is a slave receiver and has a fixed slave address (Fig.6). All PCF8577s with the same slave address acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577 on the bus. All addressed devices acknowledge the control byte. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge the segment data remains unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data only the selected PCF8577 gives an acknowledge. Loading is terminated by generating a stop (P) condition.

Display memory mapping

The mapping between the eight segment registers and the segment outputs S1 to S32 is shown in Tables 1 and 2.

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0 even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode.

Table 1 Segment byte-segment driver mapping in the direct drive mode

MODE	BANK	V2	V1	V0	segment register / bit	MSB 7	6	5	4	3	2	1	LSB 0	backplane
0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP1

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

In duplex mode even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 2 Segment byte; segment driver mapping in the duplex mode

MODE	BANK	V2	V1	V0	segment register / bit	MSB 7	6	5	4	3	2	1	LSB 0	backplane
1	x	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
1	x	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP2
1	x	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
1	x	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP2
1	x	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
1	x	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP2
1	x	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
1	x	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP2

X = don't care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

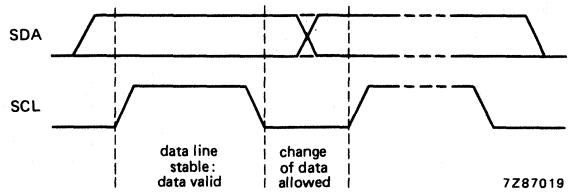


Fig.8 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

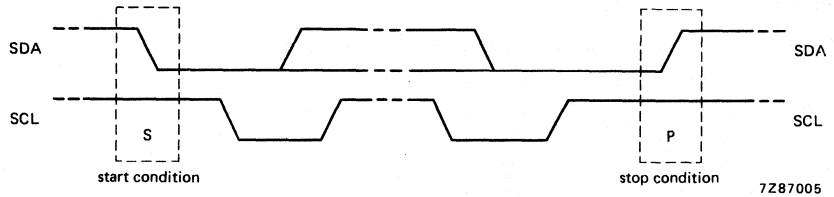


Fig.9 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

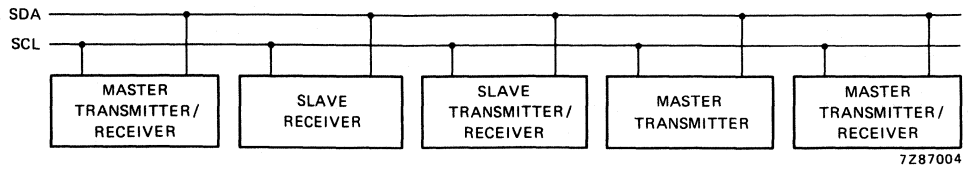


Fig.10 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

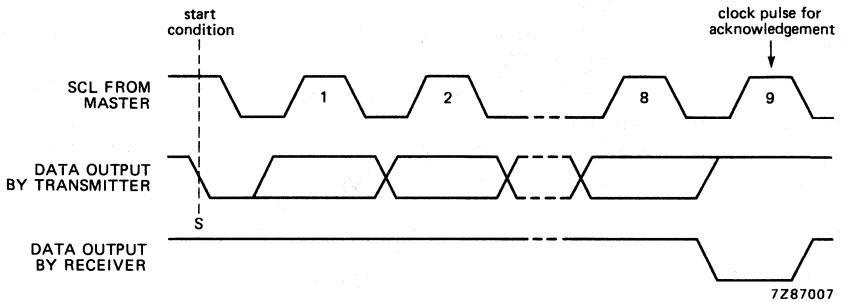


Fig.11 Acknowledgement on the I²C-bus.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+11.0	V
Voltage on pin	V_I	−0.5	V_{DD} + 0.5	V
V_{DD} or V_{SS} current	I_{DD}; I_{SS}	−50	+ 50	mA
DC input current	I_I	−20	+ 20	mA
DC output current	I_O	−25	+ 25	mA
Power dissipation per package	P_{tot}	−	500*	mW
Power dissipation per output	P_o	−	100	mW
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* Derate 7.7 mW/K when $T_{amb} > 60$ °C.

DC CHARACTERISTICS

V_{DD} = 2.5 to 9.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.*	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	9.0	V
Supply current	non specified inputs at V_{DD} or V_{SS}					
at f_{SCL} = 100 kHz	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF	I_{DD1}	–	80	250	μA
at f_{SCL} = 0	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF	I_{DD2}	–	25	150	μA
at f_{SCL} = 0	no load; R_{OSC} = 1 MΩ; C_{OSC} = 680 pF; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD3}	–	25	40	μA
at f_{SCL} = 0	no load; A0/OSC = V_{DD} or V_{SS}	I_{DD4}	–	10	20	μA
Power-on reset level	note 1	V_{POR}	–	1.1	2.0	V
Input A0						
Input voltage LOW		V_{IL1}	0	–	0.05	V
Input voltage HIGH		V_{IH1}	V_{DD}−0.05	–	V_{DD}	V
Input A1						
Input voltage LOW		V_{IL2}	0	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH2}	0.7 V_{DD}	–	V_{DD}	V
Input A2						
Input voltage LOW		V_{IL3}	0	–	0.10	V
Input voltage HIGH		V_{IH3}	V_{DD}−0.10	–	V_{DD}	V
Inputs SCL; SDA						
Input voltage LOW		V_{IL4}	0	–	0.08	V
Input voltage HIGH		V_{IH4}	2.0	–	9.0	V
Input capacitance	note 2	C_I	–	–	7	pF
Output SDA						
Output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL}	3.0	–	–	mA
A1; SCL; SDA						
Leakage current	V_I = V_{DD} or V_{SS}	$+I_{L1}$	–	–	1	μA
A2; BP2						
Leakage current	V_I = V_{SS}	I_{L2}	–	–	1	μA
Pull-down current	V_I = V_{DD}	$-I_{L2}$	–	1.5	5	μA

* Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

parameter	conditions	symbol	min.	typ.*	max.	unit
A0/OSC						
Leakage current	$V_I = V_{DD}$	$-I_{L3}$	–	–	1	μA
Oscillator						
Start-up current	$V_I = V_{SS}$	I_{OSC}	–	1.2	5	μA
LCD outputs						
DC component of LCD driver		$\pm V_{BP}$	–	20	–	mV
Segment output current	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL}	0.3	–	–	mA
	$V_{OH} = V_{DD}$ –0.4 V; V_{DD} = 5 V	$-I_{OH}$	0.3	–	–	mA
Backplane output resistance (BP1; BP2)	$V_O = V_{SS}$, V_{DD}, $(V_{SS}+V_{DD})/2$; note 3	R_{BP}	–	0.4	5	kΩ

AC CHARACTERISTICS (note 2)

V_{DD} = 2.5 to 9.0 V; V_{SS} = 0 V; T_{amb} = –40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.*	max.	unit
Display frequency	C_{OSC} = 680 pF; R_{OSC} = 1 MΩ	f_{LCD}	65	90	120	Hz
Driver delays with test loads	V_{DD} = 5 V	t_{BS}	–	20	100	μs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	μs
Start condition set-up time		$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time		t_{LOW}	4.7	–	–	μs
SCL HIGH time		t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time		t_r	–	–	1.0	μs
SCL and SDA fall time		t_f	–	–	1.3	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU;STO}$	4.7	–	–	μs

DEVELOPMENT DATA

* Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

Notes to the characteristics

1. Resets all logic when $V_{DD} < V_{POR}$.
2. Periodically sampled, not 100% tested.
3. Outputs measured one at a time; V_{DD} = 5 V; I_{load} = 100 μA.
4. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

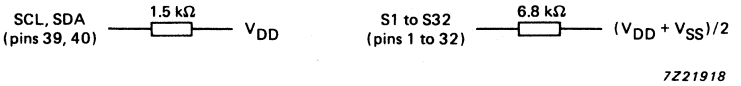


Fig.12 Test loads.

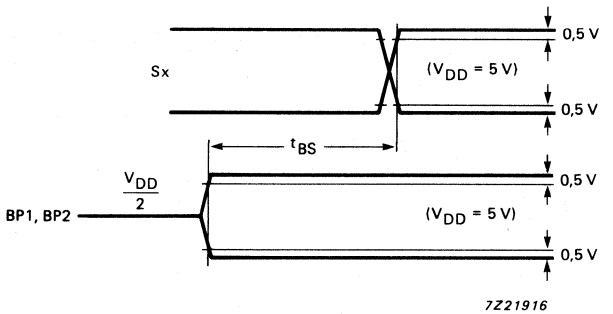


Fig.13 Driver timing waveforms.

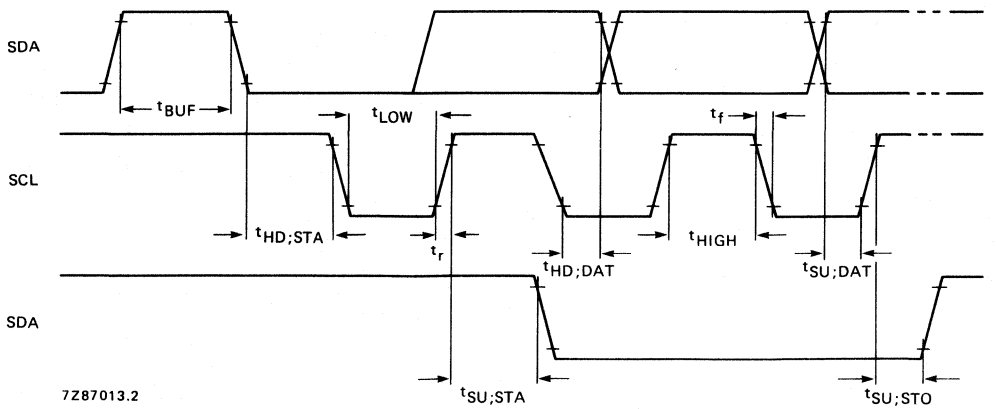


Fig.14 I^2C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

APPLICATION INFORMATION

DEVELOPMENT DATA

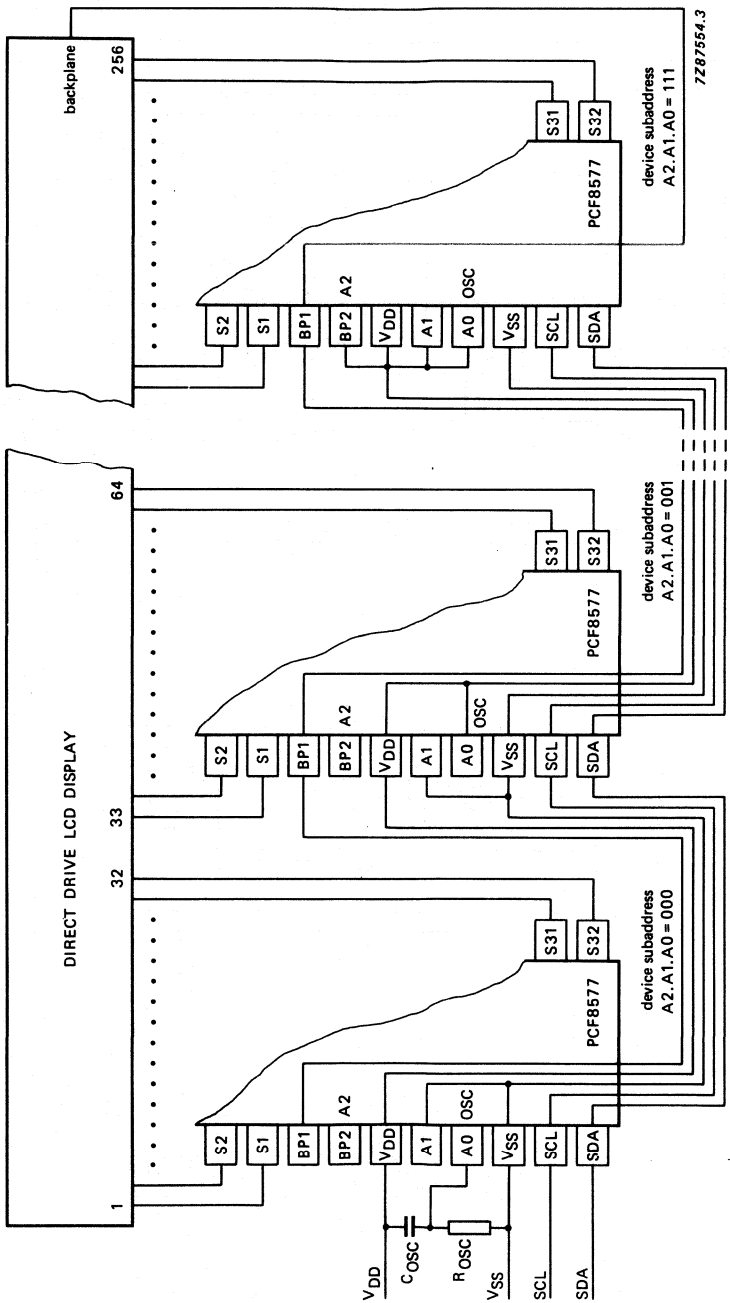


Fig.15 Direct drive display; expansion to 256 segments using eight PCF8577.

APPLICATION INFORMATION (continued)

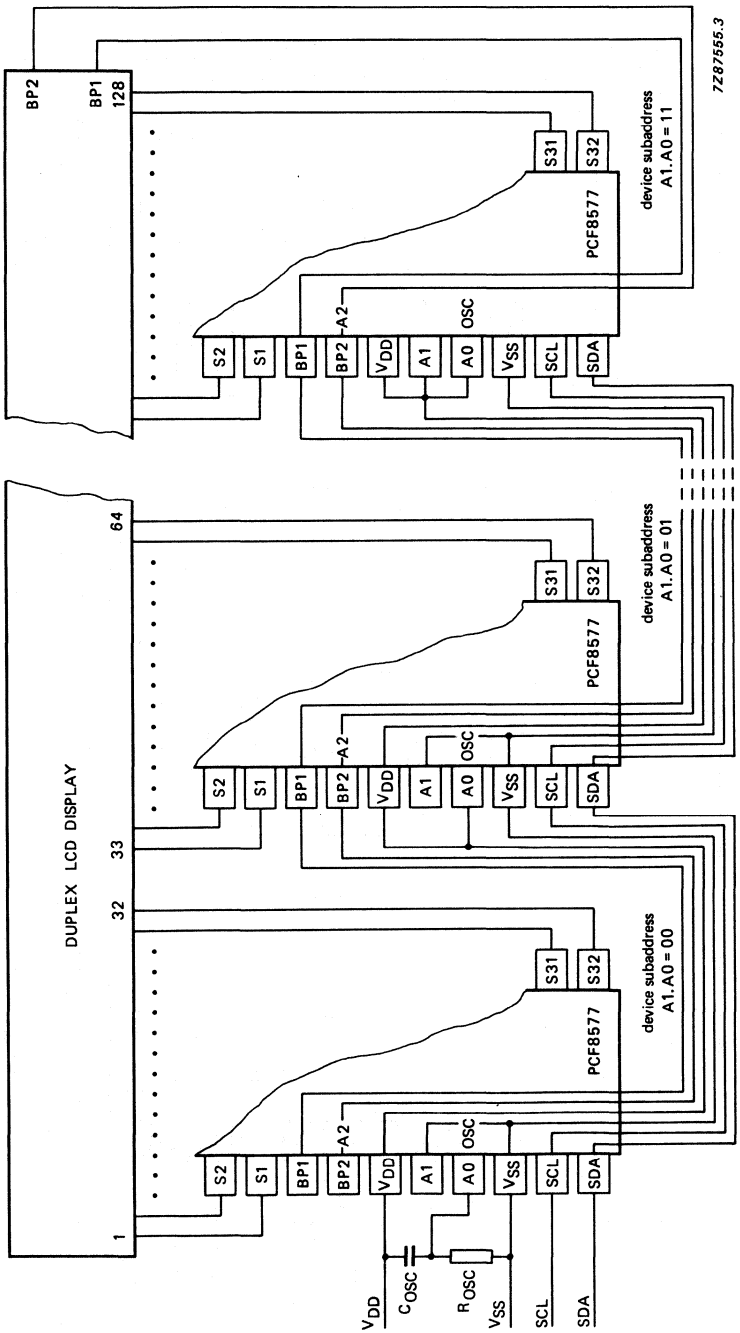
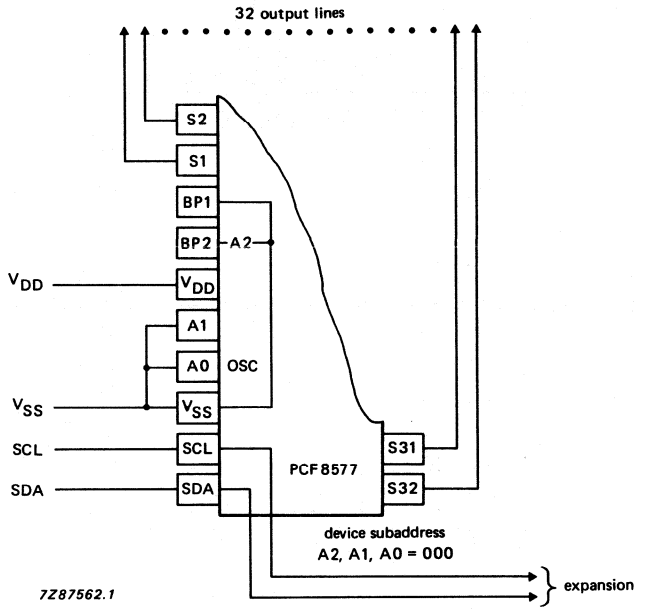


Fig.16 Duplex display; expansion to 2 x 128 segments using four PCF8577.

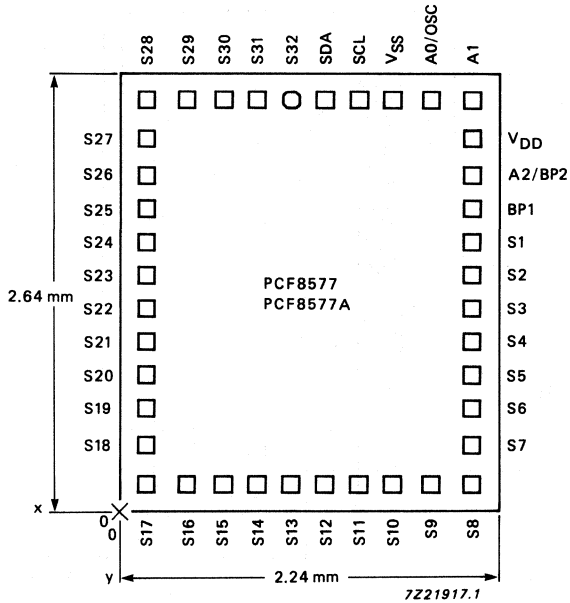


Notes

1. MODE bit must always be set to logic 0 (direct drive).
2. BANK switching is permitted.
3. BP1 must always be connected to V_{SS} and A0/OSC must be connected to either V_{DD} or V_{SS} (no LCD modulation).

Fig.17 Use of PCF8577 as 32-bit output expander in I²C-bus application.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 5.91 mm^2

Bonding pad dimensions: 120 μm x 120 μm

Fig.18 Bonding pad locations.

Table 3 Bonding pad locations (dimensions in μm)

All x/y coordinates are referenced to bottom corner, see Fig.18.

pad	X	Y	pad	X	Y
S32	1020	2480	S12	1220	160
S31	820	2480	S11	1420	160
S30	620	2480	S10	1620	160
S29	400	2480	S9	1840	160
S28	160	2480	S8	2080	160
S27	160	2240	S7	2080	400
S26	160	2020	S6	2080	620
S25	160	1820	S5	2080	820
S24	160	1620	S4	2080	1020
S23	160	1420	S3	2080	1220
S22	160	1220	S2	2080	1420
S21	160	1020	S1	2080	1620
S20	160	820	BP1	2080	1820
S19	160	620	A2/BP2	2080	2020
S18	160	400	V_{DD}	2080	2240
S17	160	160	A1	2080	2480
S16	400	160	A0/OSC	1840	2480
S15	620	160	V_{SS}	1620	2480
S14	820	160	SCL	1420	2480
S13	1020	160	SDA	1220	2480

LCD ROW/COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs, of which 24 are programmable, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40,960 dots possible)
- 40 driver outputs, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8578T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8578V: 64-lead tape-automated-bonding module (SO121).
PCF8578U: chip with bumps on-tape.

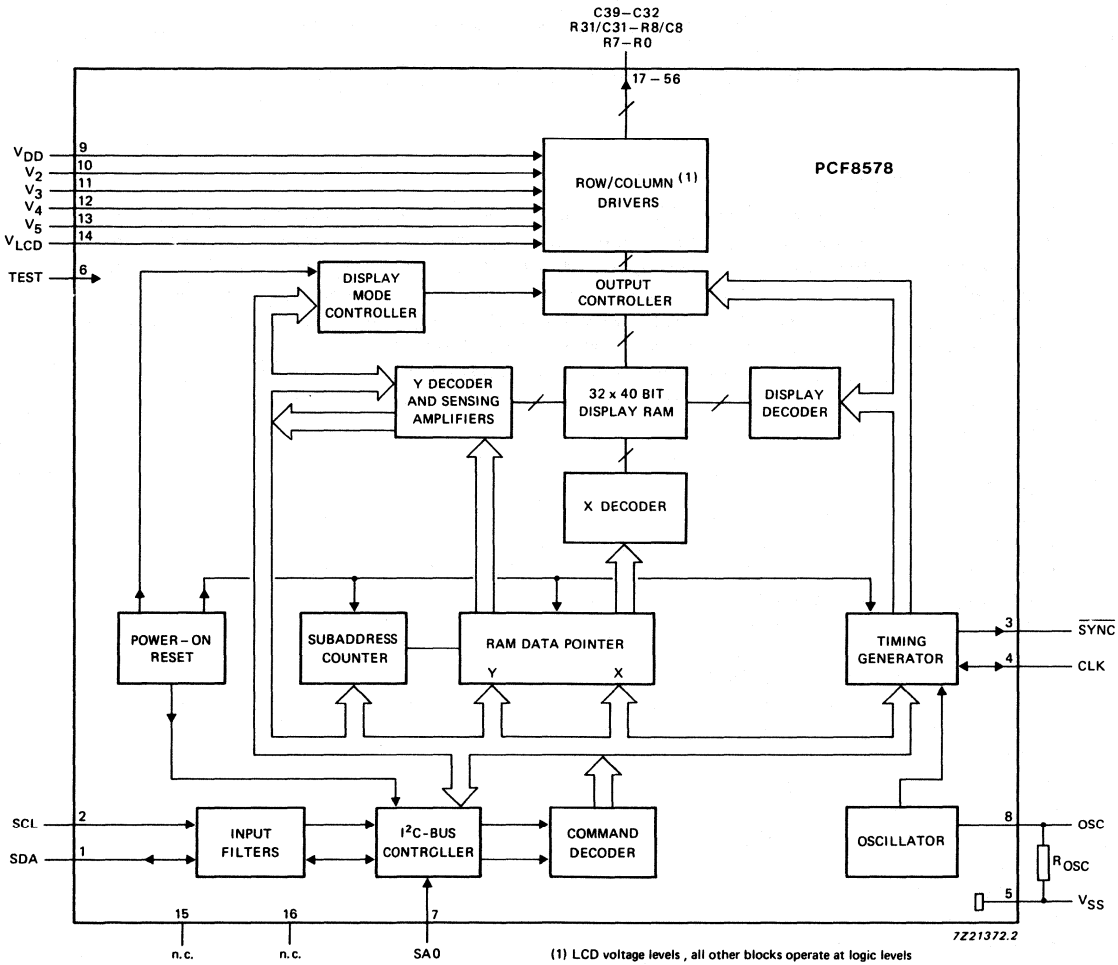


Fig.1 Block diagram.

DEVELOPMENT DATA

PINNING

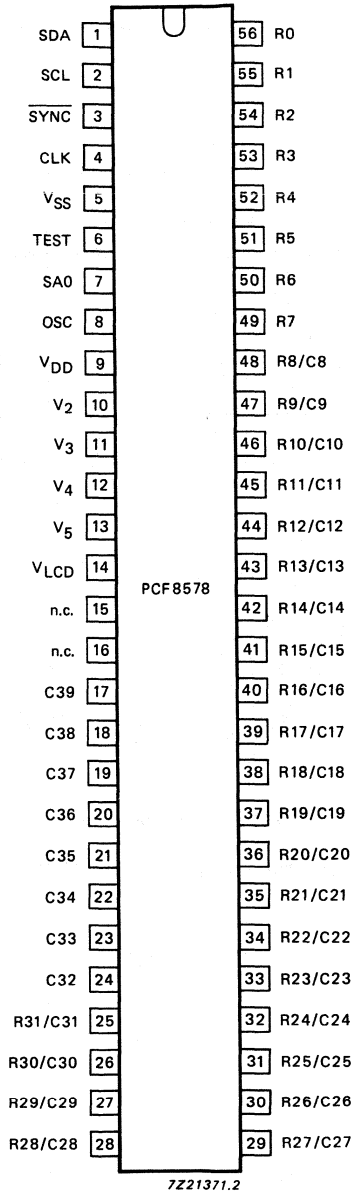
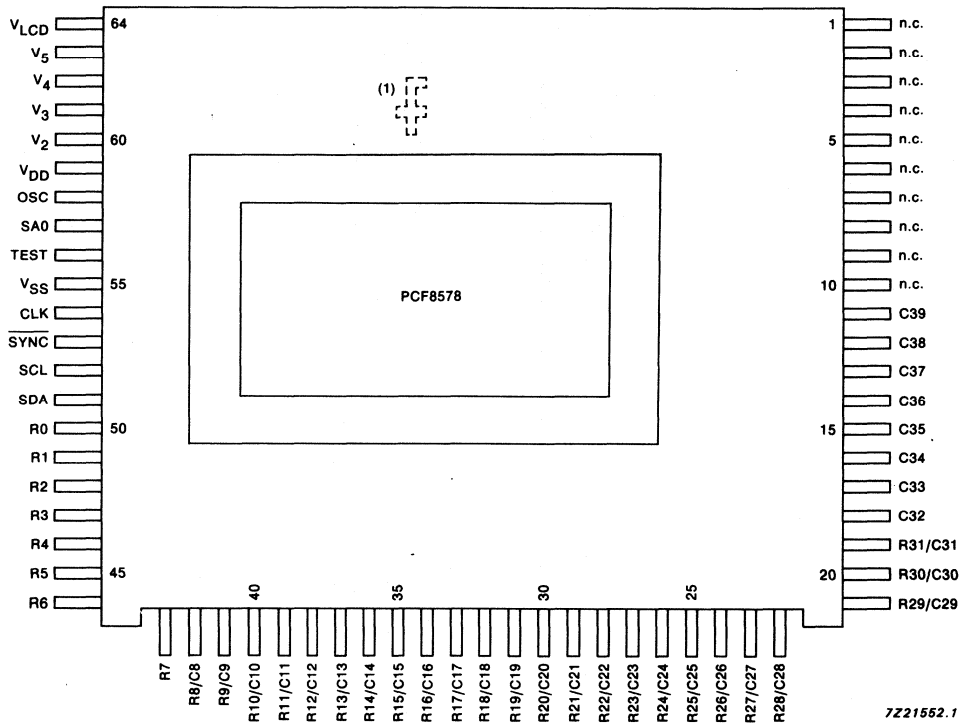


Fig.2 (a) Pinning diagram: VSO56; SOT190.

PINNING (continued)



(1) Orientation mark.

Fig.2 (b) Pinning diagram; SO121.

mnemonic	pin no.		description
	SOT190	SO121	
SDA	1	51	I^2C-bus serial data line
SCL	2	52	I^2C-bus serial clock line
$\overline{SYNC}$	3	53	cascade synchronization output
CLK	4	54	external clock input/output
V_{SS}	5	55	ground (logic)
TEST	6	56	test pin (connect to V_{SS})
SA0	7	57	I^2C-bus slave address input (bit 0)
OSC	8	58	oscillator input
V_{DD}	9	59	positive supply voltage
V_2 to V_5	10 - 13	60 - 63	LCD bias voltage inputs
V_{LCD}	14	64	LCD supply voltage
n.c.	15 - 16	1 - 10	not connected
C39 to C32	17 - 24	11 - 18	LCD column driver outputs
R31/C31 to R8/C8	25 - 48	19 - 42	LCD row/column driver outputs
R7 to R0	49 - 56	43 - 50	LCD row driver outputs

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The PCF8578 row/column driver is designed for use in one of three ways:

- Stand-alone row/column driver for small displays (mixed mode)
- Row/column driver with cascaded PCF8579s (mixed mode)
- Row driver with cascaded PCF8579s (row mode)

Mixed mode

In mixed mode, the device functions as both a row and column driver. It can be used in small stand-alone applications, or for larger displays with up to 15 PCF8579s (31 PCF8579s when two slave addresses are used). See table 1 for common display configurations.

Row mode

In row mode, the device functions as a row driver with up to 32 row outputs and provides the clock and synchronization signals for the PCF8579. Up to 16 PCF8579s can normally be cascaded (32 when two slave addresses are used).

Table 1 Possible display configurations

application	multiplex rate	mixed mode		row mode		typical applications
		rows	columns	rows	columns	
stand-alone	1:8	8	32	–	–	small digital or alphanumeric displays
	1:16	16	24	–	–	
	1:24	24	16	–	–	
	1:32	32	8	–	–	
with PCF8579	1:8	8	632	8 x 4	640	alphanumeric displays and dot matrix graphic displays
	1:16	16	624	16 x 2	640	
	1:24	24	616	24	640	
	1:32	32	608	32	640	
		using 15 PCF8579s		using 16 PCF8579s		

Timing signals are derived from the on-chip oscillator, whose frequency is determined by the value of the resistor connected between OSC and V_{SS}.

Commands sent on the I^2C-bus from the host microprocessor set the mode (row or mixed), configuration (multiplex rate and number of rows and columns) and control the operation of the device. The device may have one of two slave addresses. The only difference between these slave addresses is the least significant bit, which is set by the logic level applied to SA0. The PCF8578 and PCF8579 also have subaddresses. The subaddress of the PCF8578 is only defined in mixed mode and is fixed at 0. The RAM may only be accessed in mixed mode and data is loaded as described for the PCF8579.

Bias levels may be generated by an external potential divider with appropriate decoupling capacitors. For large displays, bias sources with high drive capability should be used. A typical mixed mode system operating with up to 15 PCF8579s is shown in Fig.3 (a stand-alone system would be identical but without the PCF8579s).

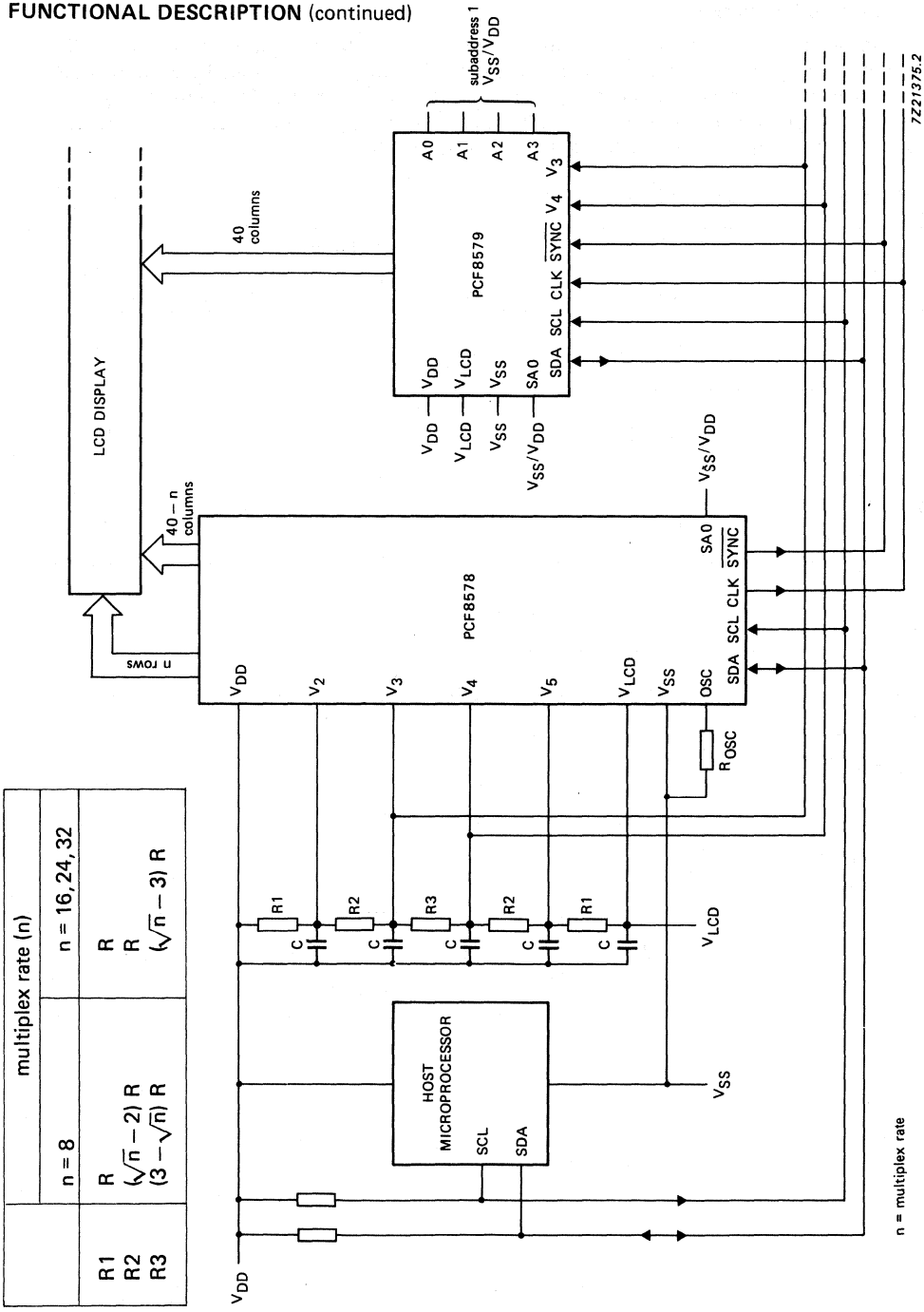
Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast. Table 2 shows the optimum voltage bias levels for the PCF8578 as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}.

Table 2 Optimum LCD bias voltages

parameter	multiplex rate			
	1:8	1:16	1:24	1:32
$\frac{V_2}{V_{op}}$	0.739	0.800	0.830	0.850
$\frac{V_3}{V_{op}}$	0.522	0.600	0.661	0.700
$\frac{V_4}{V_{op}}$	0.478	0.400	0.339	0.300
$\frac{V_5}{V_{op}}$	0.261	0.200	0.170	0.150
$\frac{V_{off(rms)}}{V_{op}}$	0.297	0.245	0.214	0.193
$\frac{V_{on(rms)}}{V_{op}}$	0.430	0.316	0.263	0.230
$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	1.447	1.291	1.230	1.196
$\frac{V_{op}}{V_{th}}$	3.37	4.08	4.68	5.19

FUNCTIONAL DESCRIPTION (continued)



	multiplex rate (n)	
	n = 8	n = 16, 24, 32
R1	R	R
R2	$(\sqrt{n} - 2)$ R	R
R3	$(3 - \sqrt{n})$ R	$(\sqrt{n} - 3)$ R

Fig.3 Typical mixed mode configuration.

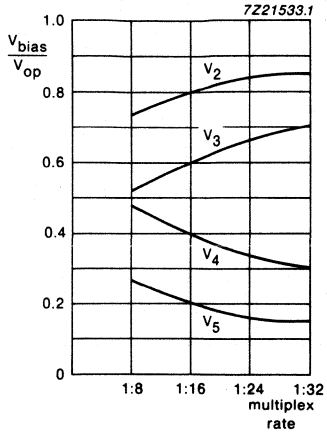


Fig.4 LCD bias voltages as a function of the multiplex rate.

DEVELOPMENT DATA

Power-on reset

At power-on the PCF8578 resets to a defined starting condition as follows:

1. Display blank
2. 1:32 multiplex rate, row mode
3. Start bank 0 selected
4. Data pointer is set to X, Y address 0, 0
5. Character mode
6. Subaddress counter is set to 0
7. I^2C-bus interface is initialized.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on, to allow completion of the reset action.

FUNCTIONAL DESCRIPTION (continued)

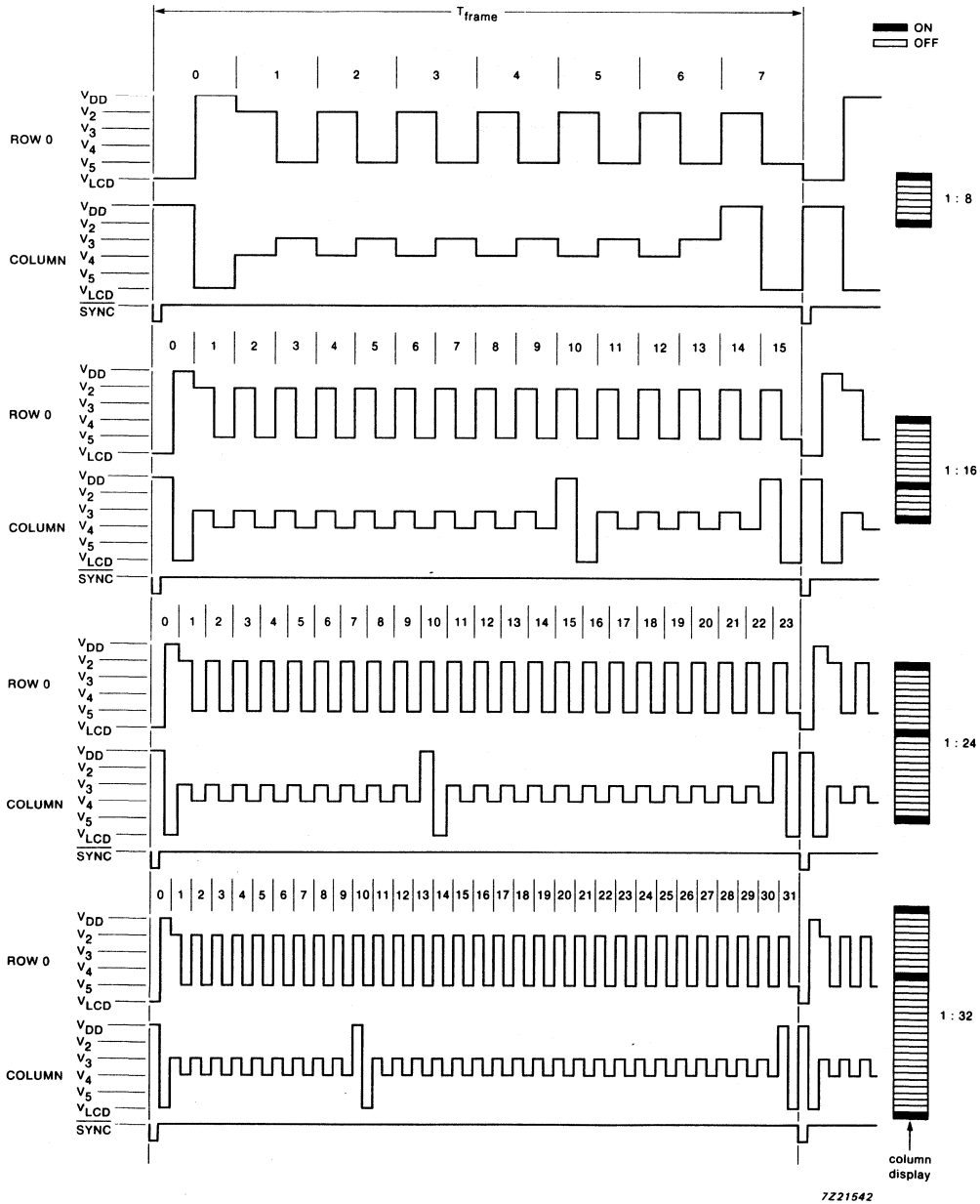
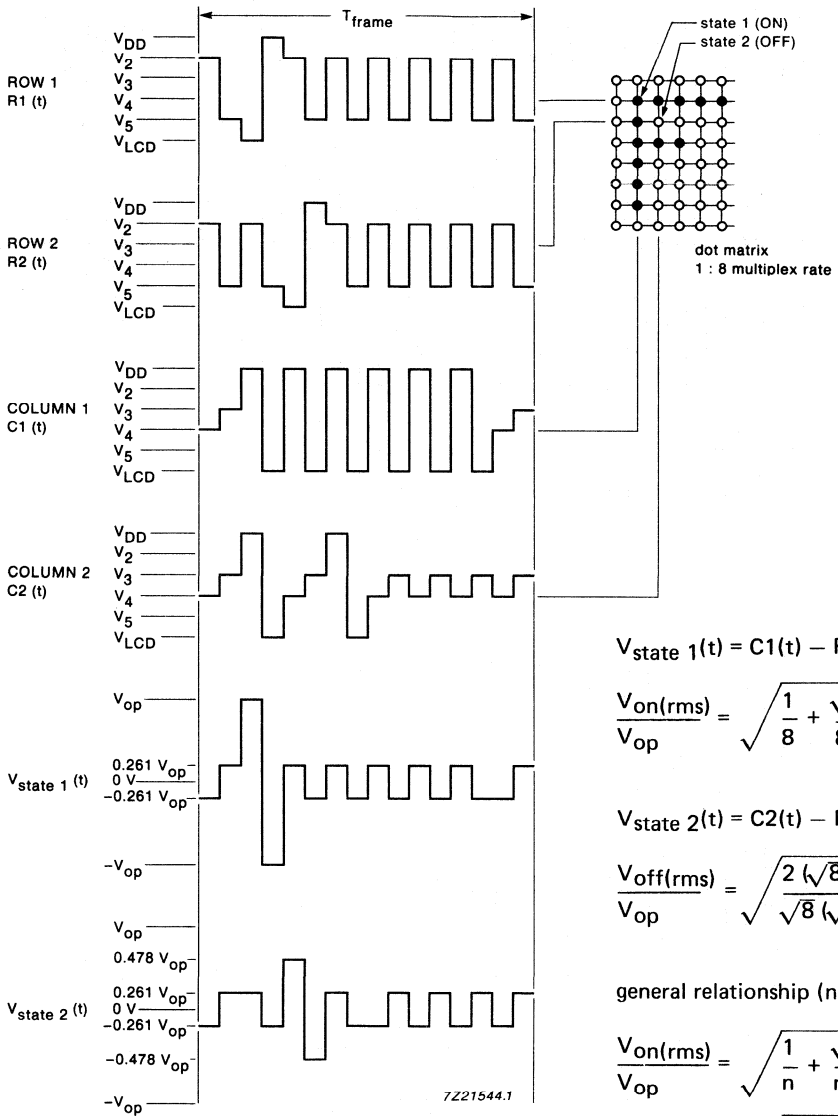


Fig.5 LCD row/column waveforms.

DEVELOPMENT DATA



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8}-1}{8(\sqrt{8}+1)}} = 0.430$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{8}-1)}{\sqrt{8}(\sqrt{8}+1)^2}} = 0.297$$

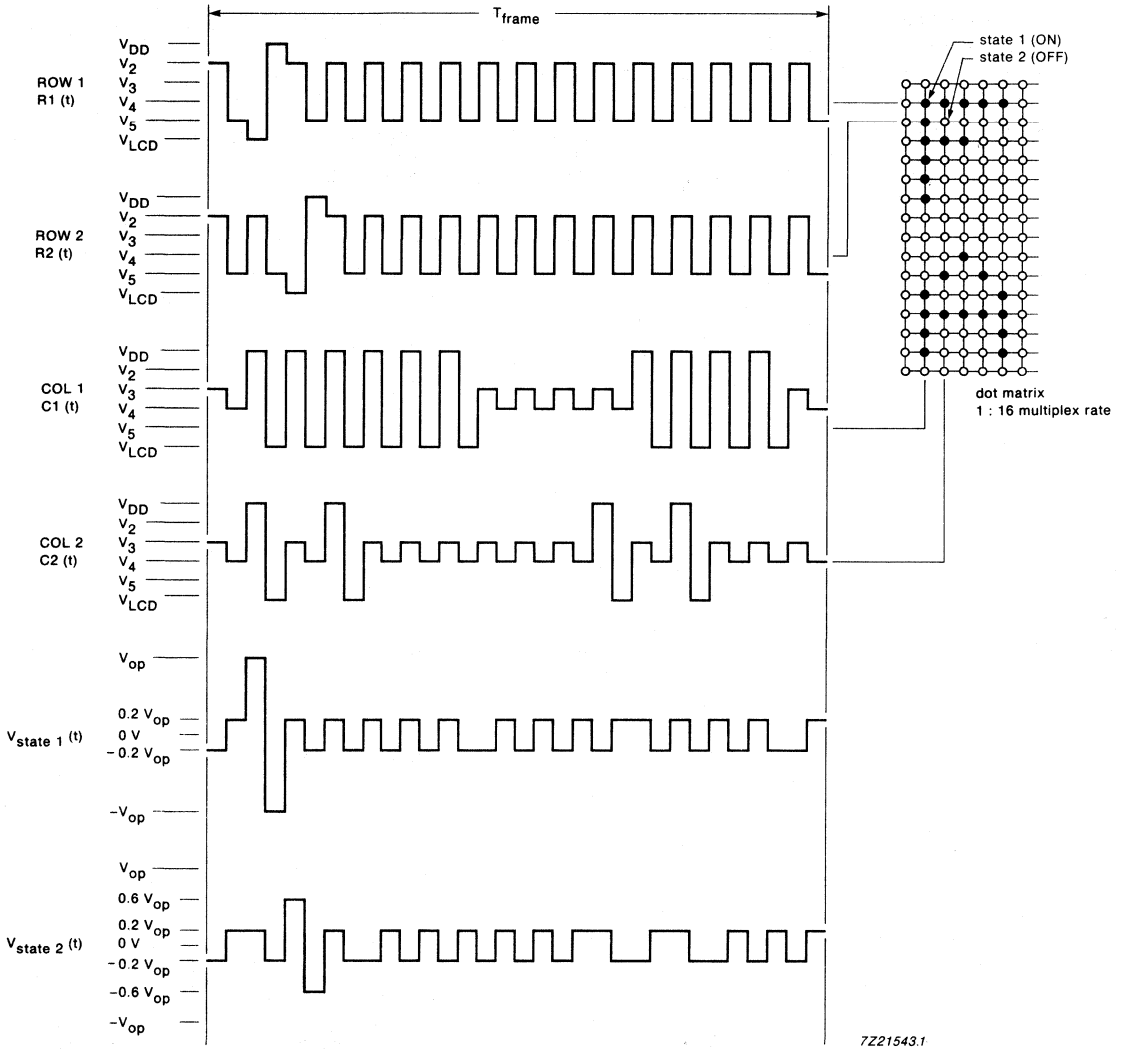
general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$$

Fig.6 LCD drive mode waveforms for 1:8 multiplex rate.

FUNCTIONAL DESCRIPTION (continued)



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16} - 1}{16\,(\sqrt{16} + 1)}} = 0.316$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{16} - 1)}{\sqrt{16}\,(\sqrt{16} + 1)^2}} = 0.245$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n} - 1}{n\,(\sqrt{n} + 1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{n} - 1)}{\sqrt{n}\,(\sqrt{n} + 1)^2}}$$

Fig.7 LCD drive mode waveforms for 1:16 multiplex rate.

DEVELOPMENT DATA

Internal clock

The clock signal for the system may be generated by the internal oscillator and prescaler. The frequency is determined by the value of the resistor R_{OSC}, see Fig.8. For normal use a value of 330 kΩ is recommended. The clock signal, for cascaded PCF8579s, is output at CLK and has a frequency one-sixth (multiplex rate 1:8, 1:16 and 1:32) or one-eighth (multiplex rate 1:24) of the oscillator frequency.

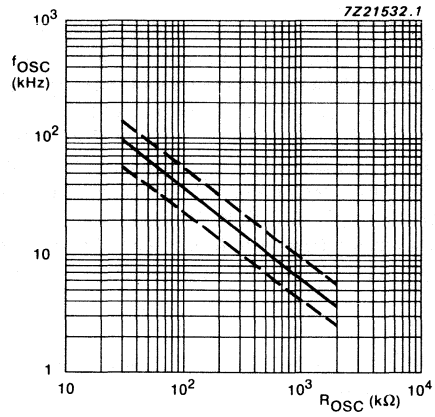


Fig.8 Oscillator frequency as a function of R_{OSC}.

Note

To avoid capacitive coupling, which could adversely affect oscillator stability, R_{OSC} should be placed as closely as possible to the OSC pin. If this proves to be a problem, a filtering capacitor may be connected in parallel to R_{OSC}.

External clock

If an external clock is used, OSC must be connected to V_{DD} and the external clock signal to CLK. Table 3 summarizes the nominal CLK and $\overline{SYNC}$ frequencies.

Table 3 Signal frequencies required for nominal 64 Hz frame frequency

oscillator frequency (R_{OSC} = 330 kΩ) f_{OSC} (Hz)	frame frequency $f_{\overline{SYNC}}$ (Hz)	multiplex rate n	division ratio	clock frequency f_{CLK} (Hz)
12288	64	1:8; 1:16; 1:32	6	2048
12288	64	1:24	8	1536

A clock signal must always be present, otherwise the LCD may be frozen in a DC state.

FUNCTIONAL DESCRIPTION (continued)

Timing generator

The timing generator of the PCF8578 organizes the internal data flow of the device and generates the LCD frame synchronization pulse $\overline{SYNC}$, whose period is an integer multiple of the clock period. In cascaded applications, this signal maintains the correct timing relationship between the PCF8578 and PCF8579s in the system.

Row/column drivers

Outputs R0 to R7 and C32 to C39 are fixed as row and column drivers respectively. The remaining 24 outputs R8/C8 to R31/C31 are programmable and may be configured (in blocks of 8) to be either row or column drivers. The row select signal is produced sequentially at each output from R0 up to the number defined by the multiplex rate (see Table 1). In mixed mode the remaining outputs are configured as columns. In row mode all programmable outputs (R8/C8 to R31/C31) are defined as row drivers and the outputs C32 to C39 should be left open-circuit. Using a 1:16 multiplex rate, two sets of row outputs are driven, thus facilitating split-screen configurations; i.e. a row select pulse appears simultaneously at R0 and R16/C16, R1 and R17/C17 etc. Similarly, using a multiplex rate of 1:8, four sets of row outputs are driven simultaneously. Driver outputs must be connected directly to the LCD. Unused outputs should be left open-circuit.

Display mode controller

The configuration of the outputs (row or column) and the selection of the appropriate driver waveforms are controlled by the display mode controller.

Display RAM

The PCF8578 contains a 32 x 40 bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes (4 x 8 x 40 bits). During RAM access, data is transferred to/from the RAM via the I^2C-bus. The first eight columns of data (0 to 7) cannot be displayed but are available for general data storage and provide compatibility with the PCF8579.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into, or read from, the display RAM, controlled by commands sent on the I^2C-bus.

Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage takes place only when the contents of the subaddress counter agree with the hardware subaddress. The hardware subaddress of the PCF8578, valid in mixed mode only, is fixed at 0000.

I^2C-bus controller

The I^2C-bus controller detects the I^2C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8578 acts as an I^2C-bus slave transmitter/receiver in mixed mode, and as a slave receiver in row mode. A slave device cannot control bus communication.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

RAM access

RAM operations are only possible when the PCF8578 is in mixed mode. In this event its hardware subaddress is internally fixed at 0000 and the hardware subaddresses of any PCF8579 used in conjunction with the PCF8578 must start at 0001.

There are three RAM ACCESS modes:

- Character
- Half-graphic
- Full-graphic

These modes are specified by bits G1 and G0 of the RAM ACCESS command. The RAM ACCESS command controls the order in which data is written to or read from the RAM (see Fig.9).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Fig.10):

- Device subaddress (specified by the DEVICE SELECT command)
- RAM X-address (specified by the LOAD X-ADDRESS command)
- RAM bank (specified by bits Y1 and Y0 of the RAM ACCESS command)

Subsequent data bytes will be written or read according to the chosen RAM access mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.

Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M1 and M0 of the SET MODE command.

The display status (all dots on/off and normal/inverse video) is set by bits E1 and E0 of the SET MODE command. For bank switching, the RAM bank corresponding to the top of the display is set by bits B1 and B0 of the SET START BANK command. This is shown in Fig.11. This feature is useful when scrolling in alphanumeric applications.

FUNCTIONAL DESCRIPTION (continued)

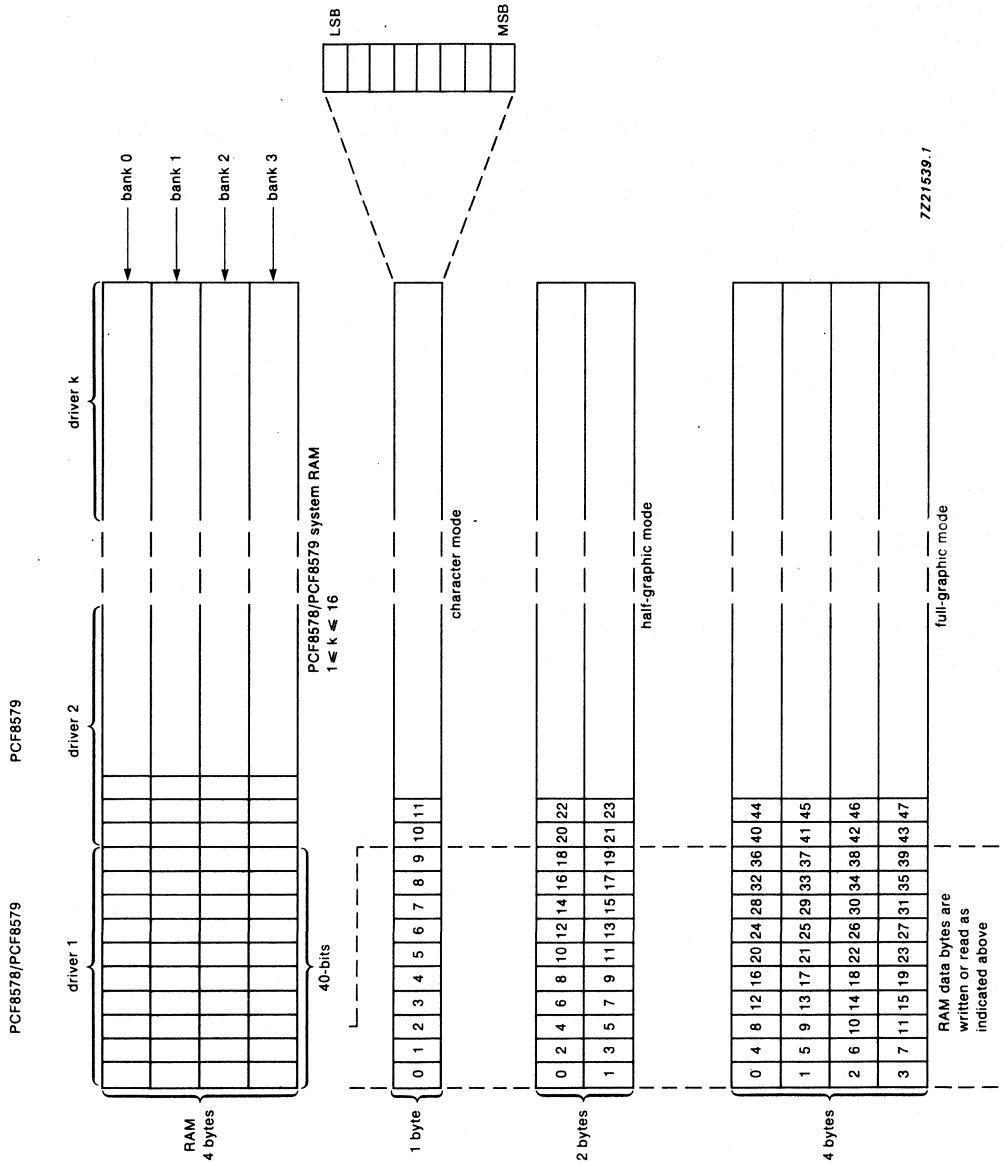


Fig.9 RAM access mode.

DEVELOPMENT DATA

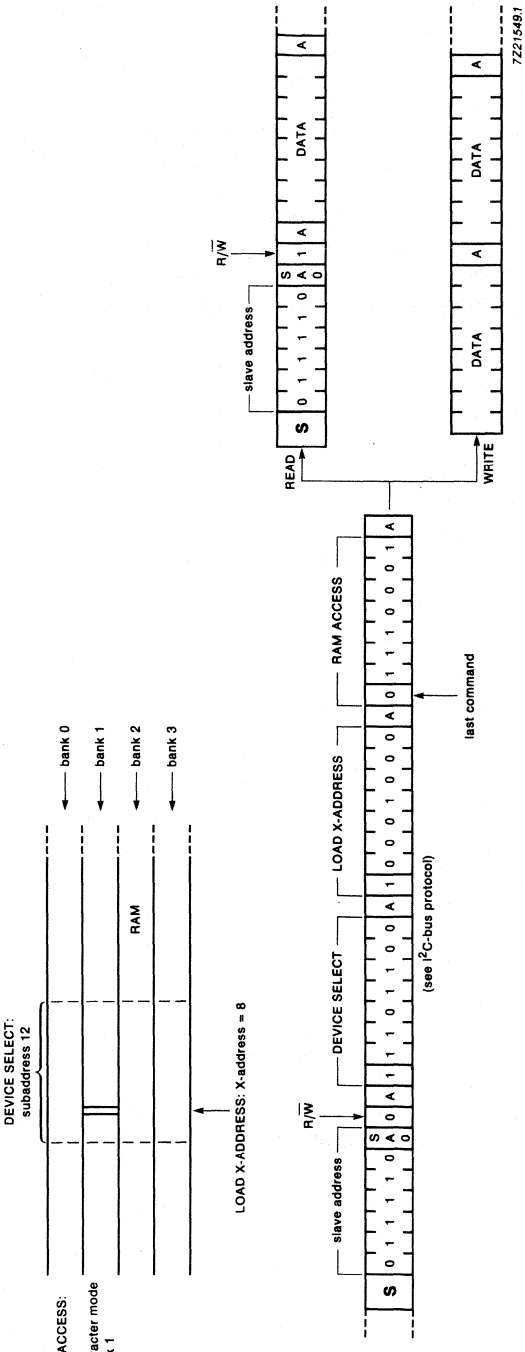


Fig.10 Example of commands specifying initial data byte RAM locations.

FUNCTIONAL DESCRIPTION (continued)

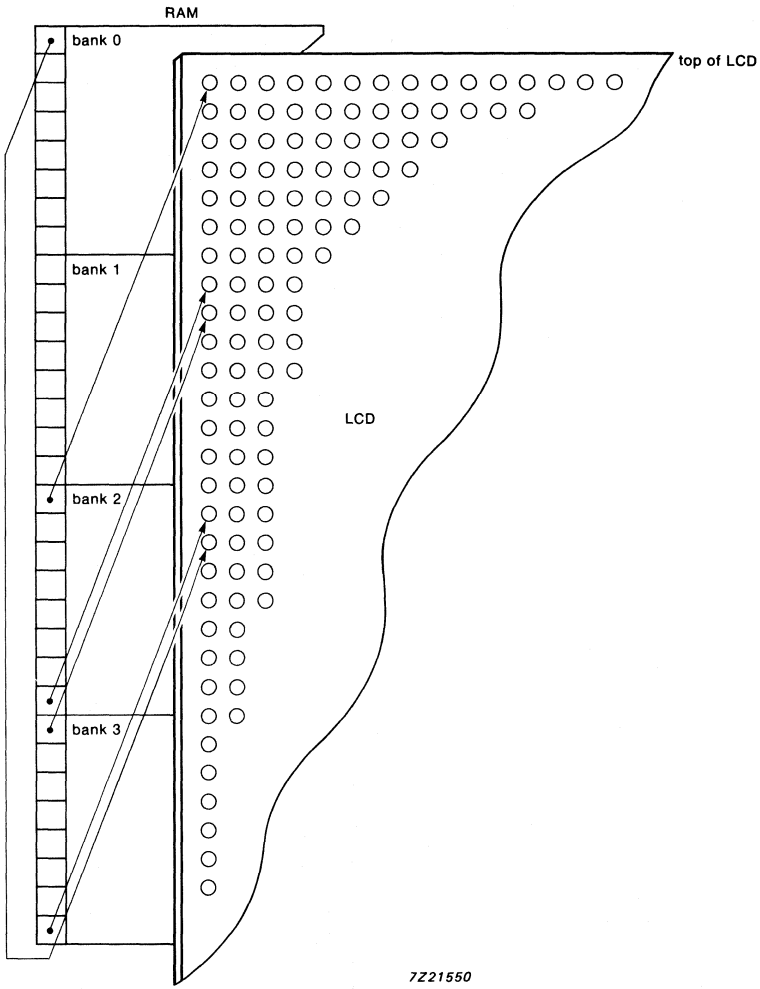


Fig.11 Relationship between display and SET START BANK; 1:32 multiplex rate and start bank = 2.

I²C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8578 and PCF8579. The least-significant bit of the slave address is set by connecting input SA0 to either 0 (V_{SS}) or 1 (V_{DD}). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I²C-bus which allows:

(a) one PCF8578 to operate with up to 32 PCF8579s on the same I²C-bus for very large applications
(b) the use of two types of LCD multiplex schemes on the same I²C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

The I²C-bus protocol is shown in Fig. 12. All communications are initiated with a start condition (S) from the I²C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I²C-bus master issues a stop condition (P).

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8578 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by **not** generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a stop condition (P).

Display bytes are written into, or read from, the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from, the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8579s (A_0 to A_3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated a unique hardware subaddress.

I²C-BUS PROTOCOL (continued)

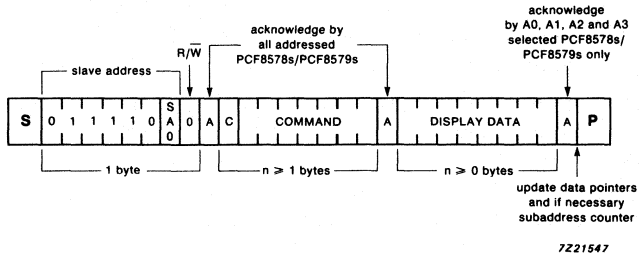


Fig.12(a) Master transmits to slave receiver (WRITE mode).

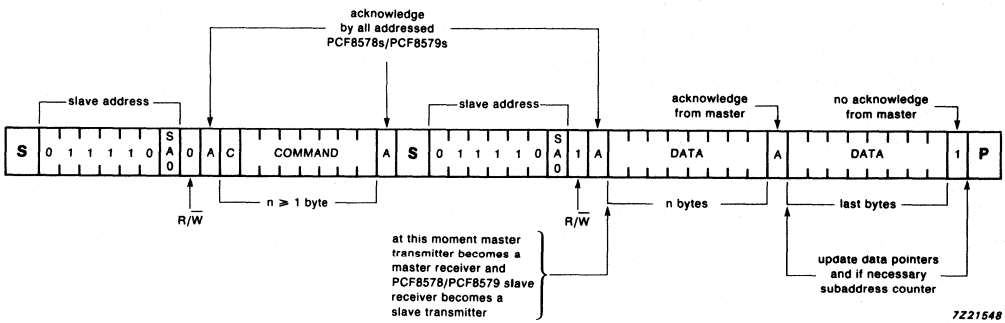


Fig.12(b) Master reads after sending command string (WRITE commands; READ data).

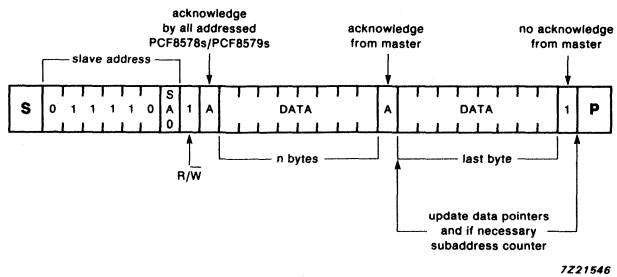
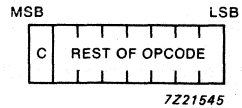


Fig.12(c) Master reads slave immediately after sending slave address (READ mode).

Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. The most-significant bit of a command is the continuation bit C (see Fig.13). When this bit is set, it indicates that the next byte to be transferred will also be a command. If the bit is reset, it indicates the conclusion of the command transfer. Further bytes will be regarded as display data. Commands are transferred in WRITE mode only.



C = 0; last command
C = 1; commands continue

Fig.13 General format of command byte.

The five commands available to the PCF8578 are defined in Tables 4 and 5.

Table 4 Summary of commands

code	command	description
C 0 D D D D D D	LOAD X-ADDRESS	0 to 39
C 1 0 D D D D D	SET MODE	multiplex rate, display status, system type
C 1 1 0 D D D D	DEVICE SELECT	defines device subaddress
C 1 1 1 D D D D	RAM ACCESS	graphic mode, bank select (D D D D ⩾ 12 is not allowed; see SET START BANK opcode)
C 1 1 1 1 1 D D	SET START BANK	defines bank at top of LCD

Where:

C = command continuation bit
D = may be a logic 1 or 0.

I²C-BUS PROTOCOL (continued)

Table 5 Definition of PCF8578/PCF8579 commands

command / opcode	options	description
SET MODE C 1 0 T E1 E0 M1 M0	LCD drive mode bits M1 M0 1:8 MUX (8 rows) 0 1 1:16 MUX (16 rows) 1 0 1:24 MUX (24 rows) 1 1 1:32 MUX (32 rows) 0 0	defines LCD drive mode
	display status bits E1 E0 blank 0 0 normal 0 1 all segments on 1 0 inverse video 1 1	defines display status
	system type bit T PCF8578 row only 0 PCF8578 mixed mode 1	defines system type
SET START BANK C 1 1 1 1 1 B1 B0	start bank pointer bits B1 B0 bank 0 0 0 bank 1 0 1 bank 2 1 0 bank 3 1 1	defines pointer to RAM bank corresponding to the top of the LCD. Useful for scrolling, pseudo-motion and background preparation of new display
DEVICE SELECT C 1 1 0 A3 A2 A1 A0	bits A3 A2 A1 A0 4-bit binary value of 0 to 15	four bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of sixteen hardware subaddresses

command / opcode	options	description
RAM ACCESS C | 1 1 1 | G1 G0 | Y1 Y0	RAM access mode bits G1 G0 character 0 0 half graphic 0 1 full graphic 1 0 not allowed * 1 1	defines the auto-increment behaviour of the address for RAM access
	bits Y1 Y0 2-bit binary value of 0 to 3	two bits of immediate data, bits Y0 to Y1, are transferred to the Y-address pointer to define one of four banks for RAM access
LOAD X-ADDRESS C | 0 | X5 X4 X3 X2 X1 X0	bits X5 X4 X3 X2 X1 X0 6-bit binary value of 0 to 39	six bits of immediate data, bits X0 to X5, are transferred to the X-address pointer to define one of forty display RAM columns

DEVELOPMENT DATA

* See opcode for SET START BANK.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL) which must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this moment will be interpreted as control signals.

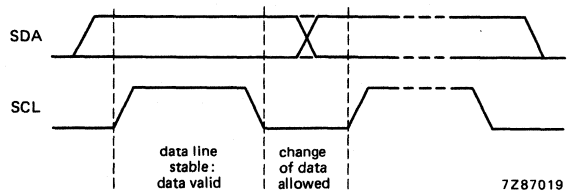


Fig.14 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

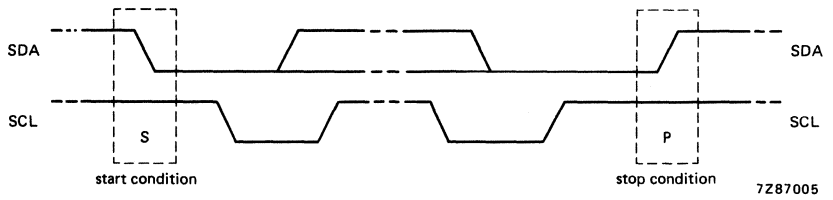


Fig.15 Definition of start and stop condition.

System configuration

A device transmitting a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message flow is the "master" and the devices which are controlled by the master are the "slaves".

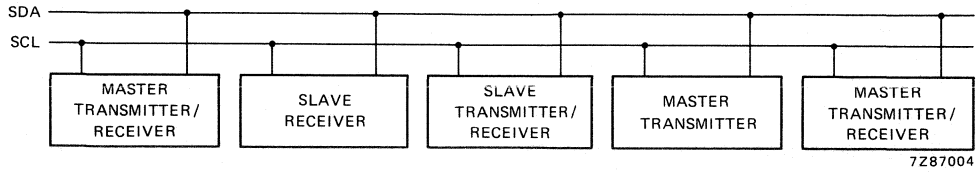


Fig.16 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

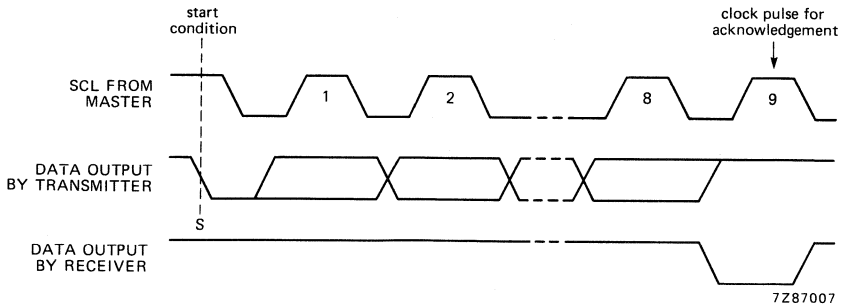


Fig.17 Acknowledgement on the I^2C-bus.

Note

The general characteristics and detailed specification of the I^2C-bus are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+8.0	V
LCD supply voltage range	V_{LCD}	V_{DD} −11	V_{DD}	V
Input voltage range at SDA, SCL, CLK, TEST, SA0 and OSC	V_{I1}	V_{SS} −0.5	V_{DD} +0.5	V
V_2 to V_5	V_{I2}	V_{LCD} −0.5	V_{DD} +0.5	V
Output voltage range at $\overline{SYNC}$ and CLK	V_{O1}	V_{SS} −0.5	V_{DD} +0.5	V
R0 to R7, R8/C8 to R31/C31, and C32 to C39	V_{O2}	V_{LCD} −0.5	V_{DD} +0.5	V
DC input current	I_I	−10	10	mA
DC output current	I_O	−10	10	mA
V_{DD}, V_{SS} or V_{LCD} current	I_{DD}, I_{SS}, I_{LCD}	−50	50	mA
Power dissipation per package	P_{tot}	−	400	mW
Power dissipation per output	P_o	−	100	mW
Storage temperature range	T_{stg}	−65	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 2.5 V to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
LCD supply voltage		V_{LCD}	V_{DD} −9	–	V_{DD} −3.5	V
Supply current	note 1;					
external clock	f_{CLK} = 2 kHz	I_{DD1}	–	6	15	μA
internal clock	R_{OSC} = 330 kΩ	I_{DD2}	–	20	50	μA
Power-on reset level	note 2	V_{POR}	0.8	1.3	1.8	V
Logic						
Input voltage LOW		V_{IL}	V_{SS}	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Output current LOW at $\overline{SYNC}$ and CLK	V_{OL} = 1.0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH at $\overline{SYNC}$ and CLK	V_{OH} = 4.0 V; V_{DD} = 5 V	I_{OH1}	–	–	−1	mA
SDA output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL2}	3.0	–	–	mA
Leakage current at SDA, SCL, $\overline{SYNC}$, CLK, TEST and SA0	V_I = V_{DD} or V_{SS}	I_{L1}	−1	–	1	μA
Leakage current at OSC	V_I = V_{DD}	I_{L2}	−1	–	1	μA
Input capacitance at SCL and SDA	note 3	C_I	–	–	5	pF
LCD outputs						
Leakage current at V_2 to V_5	V_I = V_{DD} or V_{LCD}	I_{L3}	−2	–	2	μA
DC component of LCD drivers R0 to R7, R8/C8 to R31/C31, and C32 to C39		± V_{DC}	–	20	–	mV
Output resistance at R0 to R7 and R8/C8 to R31/C31	note 4; row mode	R_{ROW}	–	1.5	3.0	kΩ
R8/C8 to R31/C31 and C32 to C39	column mode	R_{COL}	–	3	6	kΩ

AC CHARACTERISTICS (note 5)

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = - 40 to + 85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Clock frequency at multiplex rates of	R_{OSC} = 330 kΩ; V_{DD} = 6 V					
1:8, 1:16 and 1:32		f_{CLK1}	1.2	2.1	3.3	kHz
1:24		f_{CLK2}	0.9	1.6	2.5	kHz
$\overline{SYNC}$ propagation delay		t_{PSYNC}	–	–	500	ns
Driver delays	V_{DD} − V_{LCD} = 9 V; with test loads	t_{PLCD}	–	–	100	μs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	μs
Start condition set-up time	repeated start codes only	$t_{SU;STA}$	4.7	–	-	μs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time		t_{LOW}	4.7	–	–	μs
SCL HIGH time		t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time		t_r	–	–	1.0	μs
SCL and SDA fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU;STO}$	4.0	–	–	μs

Notes to the characteristics

1. Outputs are open; inputs at V_{DD} or V_{SS}; I^2C-bus inactive; external clock with 50% duty factor, (I_{DD1} only).
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (R0 to R7, R8/C8 to R31/C31 and C32 to C39) and bias input (V_2 to V_5, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 2):

   $V_{OP} = V_{DD} - V_{LCD} = 9$ V;

   row mode, R0 to R7 and R8/C8 to R31/C31 (row mode):
   $V_2 - V_{LCD} \geqslant 6.65$ V; $V_5 - V_{LCD} \leqslant 2.35$ V; $I_{LOAD} = 150\ \mu$A

   column mode, R8/C8 to R31/C31 (column mode) and C32 to C39:
   $V_3 - V_{LCD} \geqslant 4.70$ V; $V_4 - V_{LCD} \leqslant 4.30$ V; $I_{LOAD} = 100\ \mu$A.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

DEVELOPMENT DATA

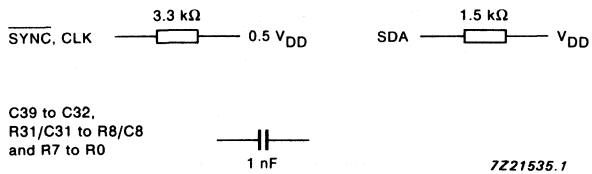


Fig.18 Test loads.

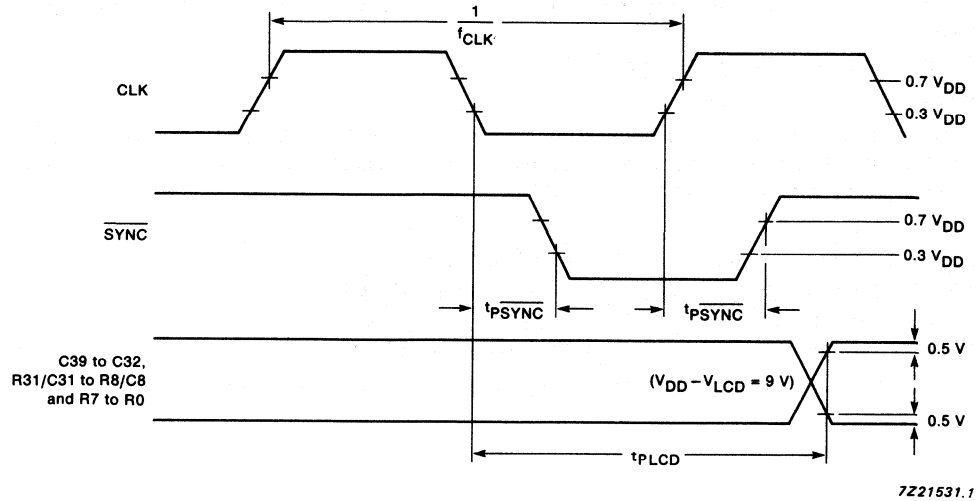


Fig.19 Driver timing waveforms.

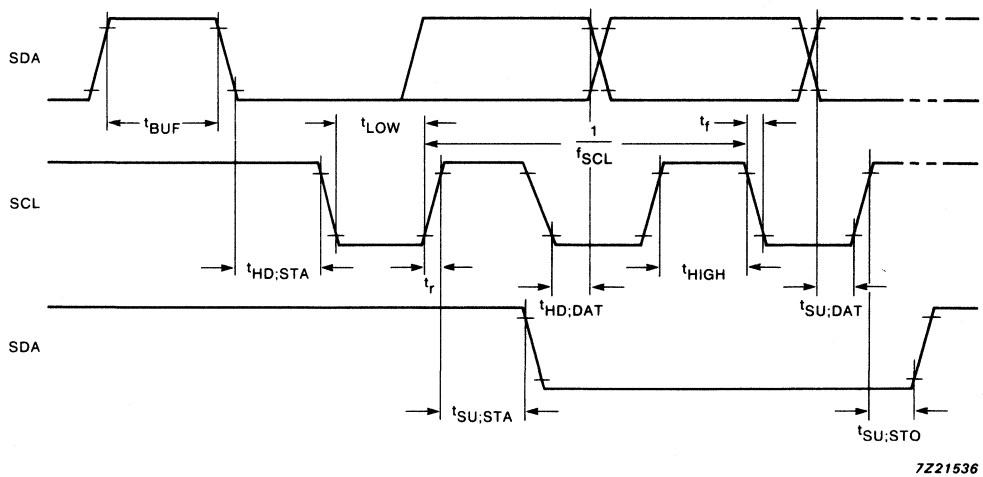


Fig.20 I^2C-bus timing waveforms.

APPLICATION INFORMATION

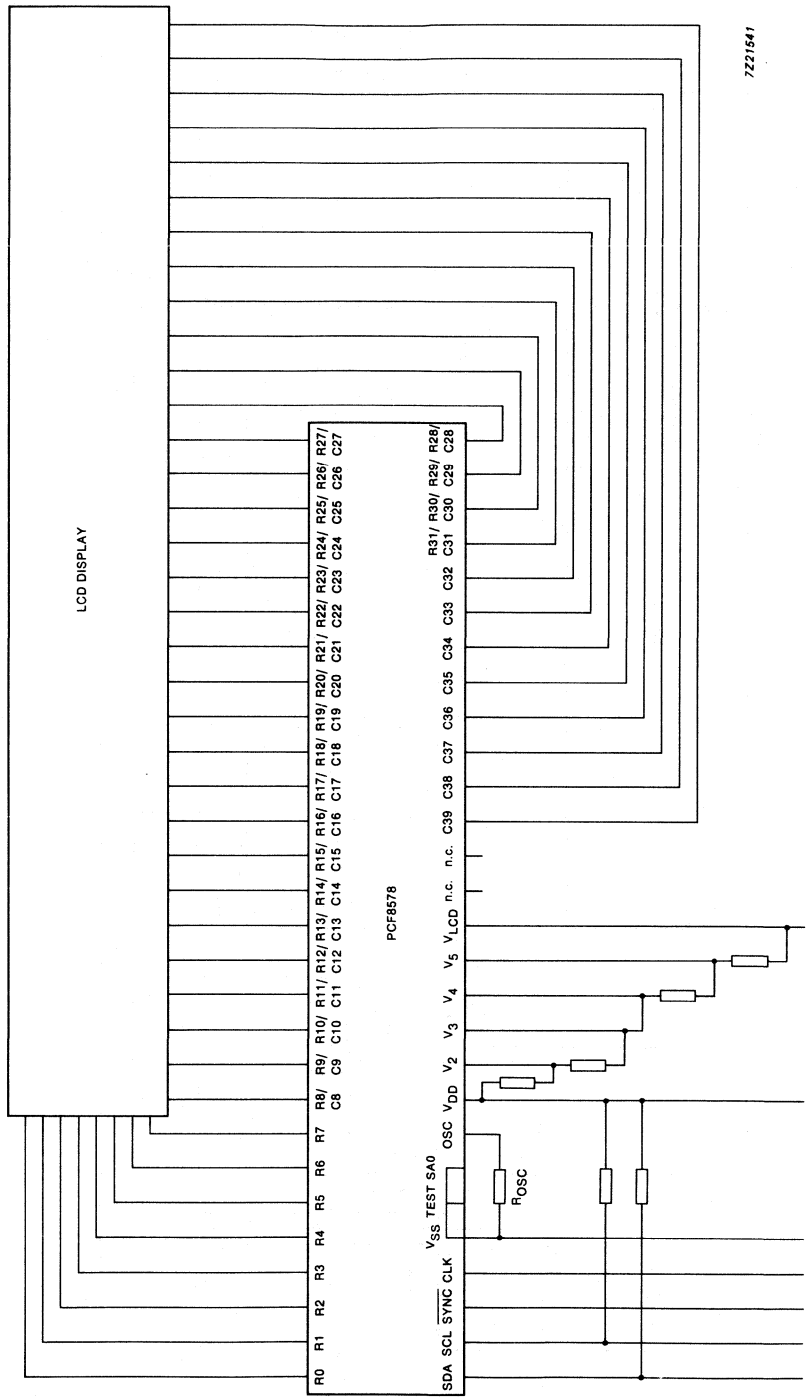


Fig.21 Stand-alone application using 8 rows and 32 columns.

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

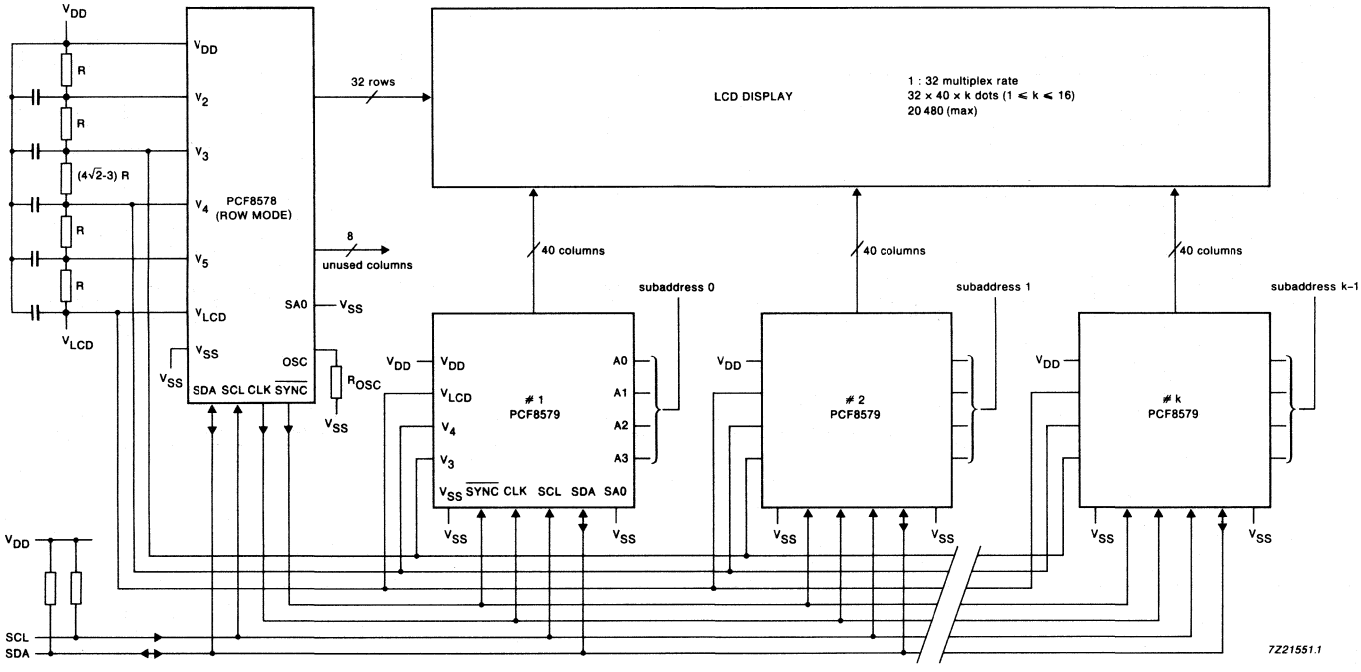


Fig.22 Typical LCD driver system with 1:32 multiplex rate.

DEVELOPMENT DATA

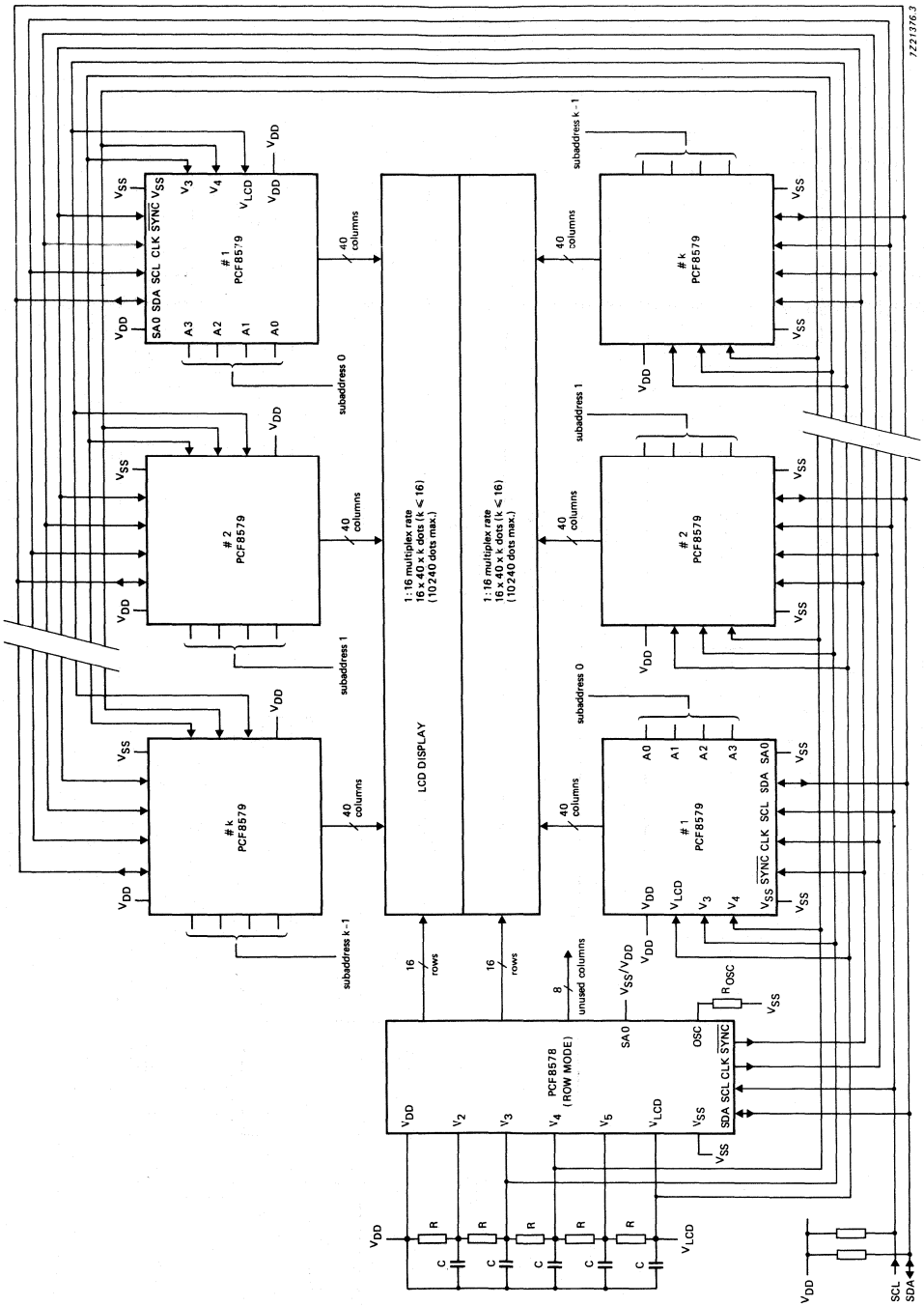


Fig.23 Split screen application with 1:16 multiplex rate for improved contrast.

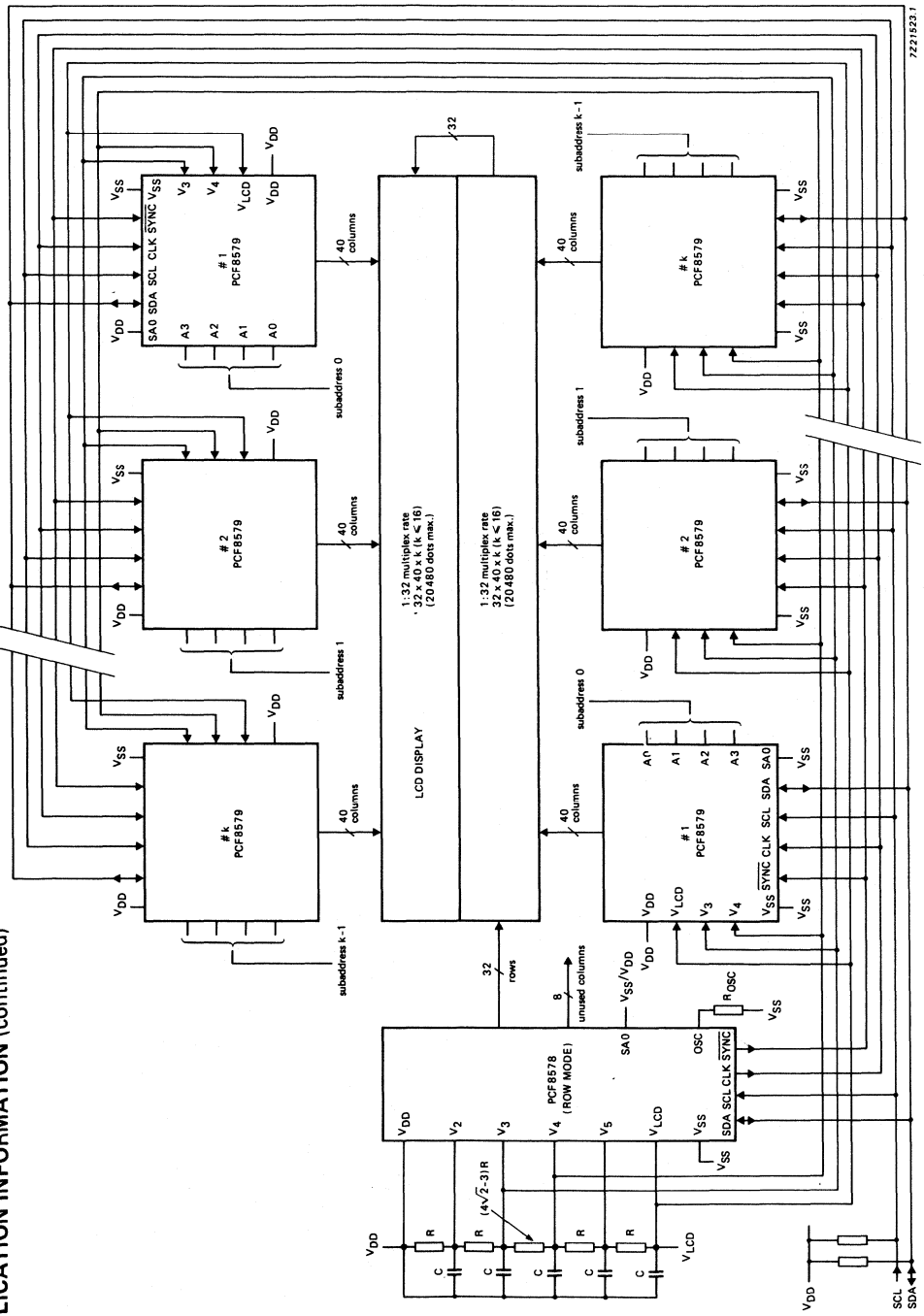


Fig.24 Split screen application with 1:32 multiplex rate.

DEVELOPMENT DATA

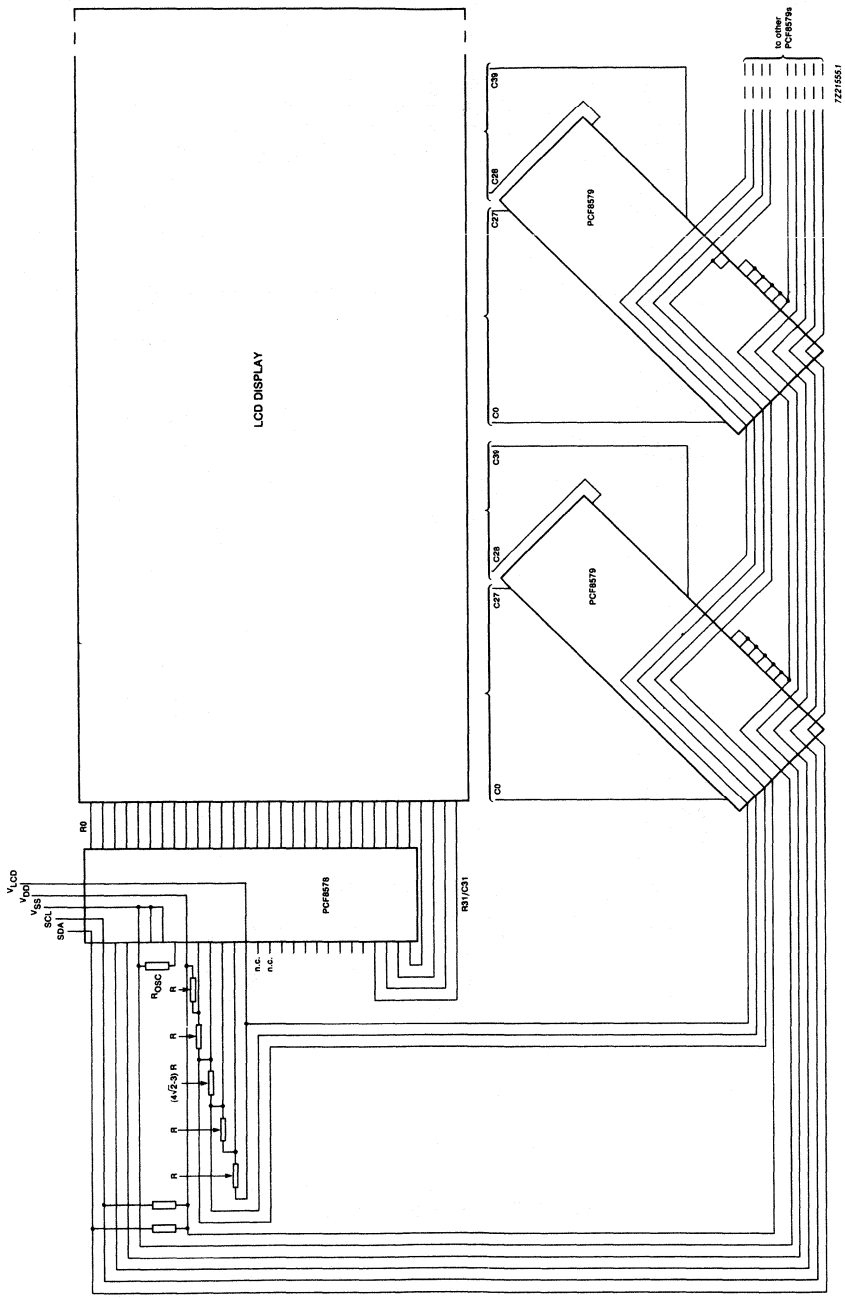
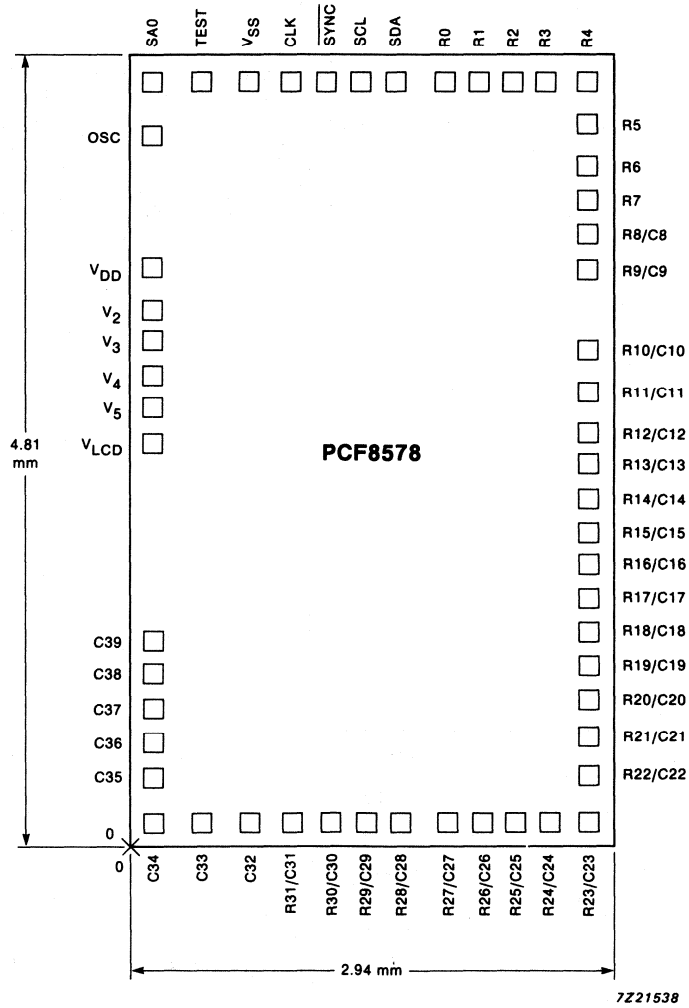


Fig.25 Example of single plane wiring, single screen with 1:32 multiplex rate (PCF8578 in row driver mode).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 14.14 mm^2
Bonding pad dimensions: 120 μm x 120 μm.

Fig.26 Bonding pad locations.

Table 6 Bonding pad locations (dimensions in μm)

All x/y co-ordinates are referenced to the bottom left corner, see Fig.26.

pad	X	Y	pad	X	Y
SDA	1642	4642	R27/C27	1936	160
SCL	1438	4642	R26/C26	2140	160
$\overline{SYNC}$	1234	4642	R25/C25	2344	160
CLK	1000	4642	R24/C24	2548	160
V_{SS}	742	4642	R23/C23	2776	160
TEST	454	4642	R22/C22	2776	424
SA0	160	4642	R21/C21	2776	670
OSC	160	4318	R20/C20	2776	886
V_{DD}	160	3514	R19/C19	2776	1096
V_2	160	3274	R18/C18	2776	1300
V_3	160	3064	R17/C17	2776	1504
V_4	160	2860	R16/C16	2776	1708
V_5	160	2656	R15/C15	2776	1912
V_{LCD}	160	2452	R14/C14	2776	2116
n.c.	—	—	R13/C13	2776	2320
n.c.	—	—	R12/C12	2776	2524
C39	160	1252	R11/C11	2776	2752
C38	160	1048	R10/C10	2776	3004
C37	160	844	R9/C9	2776	3502
C36	160	628	R8/C8	2776	3706
C35	160	406	R7	2776	3916
C34	160	160	R6	2776	4132
C33	454	160	R5	2776	4378
C32	742	160	R4	2776	4642
R31/C31	1000	160	R3	2548	4642
R30/C30	1234	160	R2	2344	4642
R29/C29	1438	160	R1	2140	4642
R28/C28	1642	160	R0	1936	4642

DEVELOPMENT DATA

CHIP-ON GLASS INFORMATION

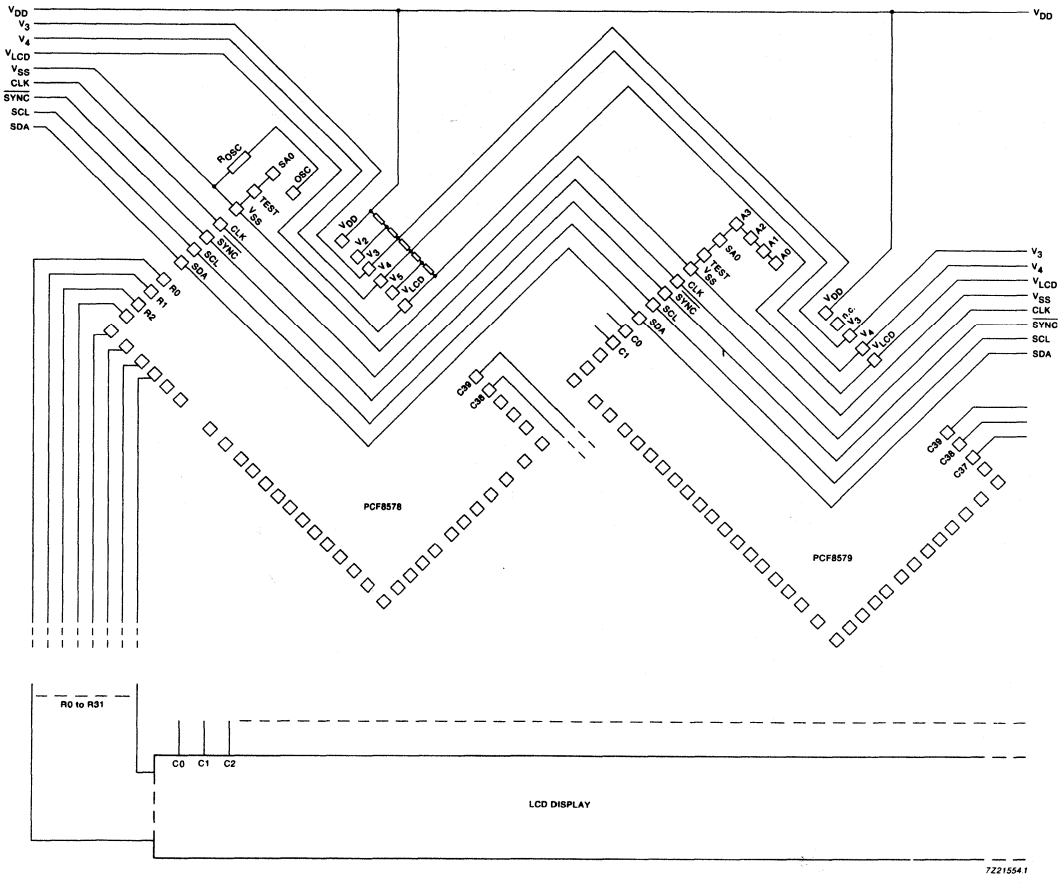


Fig.27 Typical chip-on glass application (viewed from underside of chip).

Note to Fig.27

If inputs SA0 and A0 to A3 are left unconnected they are internally pulled-up to V_{DD}.

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs and can drive 32 x 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40,960 dots
- 40 column outputs
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8579T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8579V: 64-lead tape-automated-bonding module (SO122).
PCF8579U: chip with bumps on-tape.

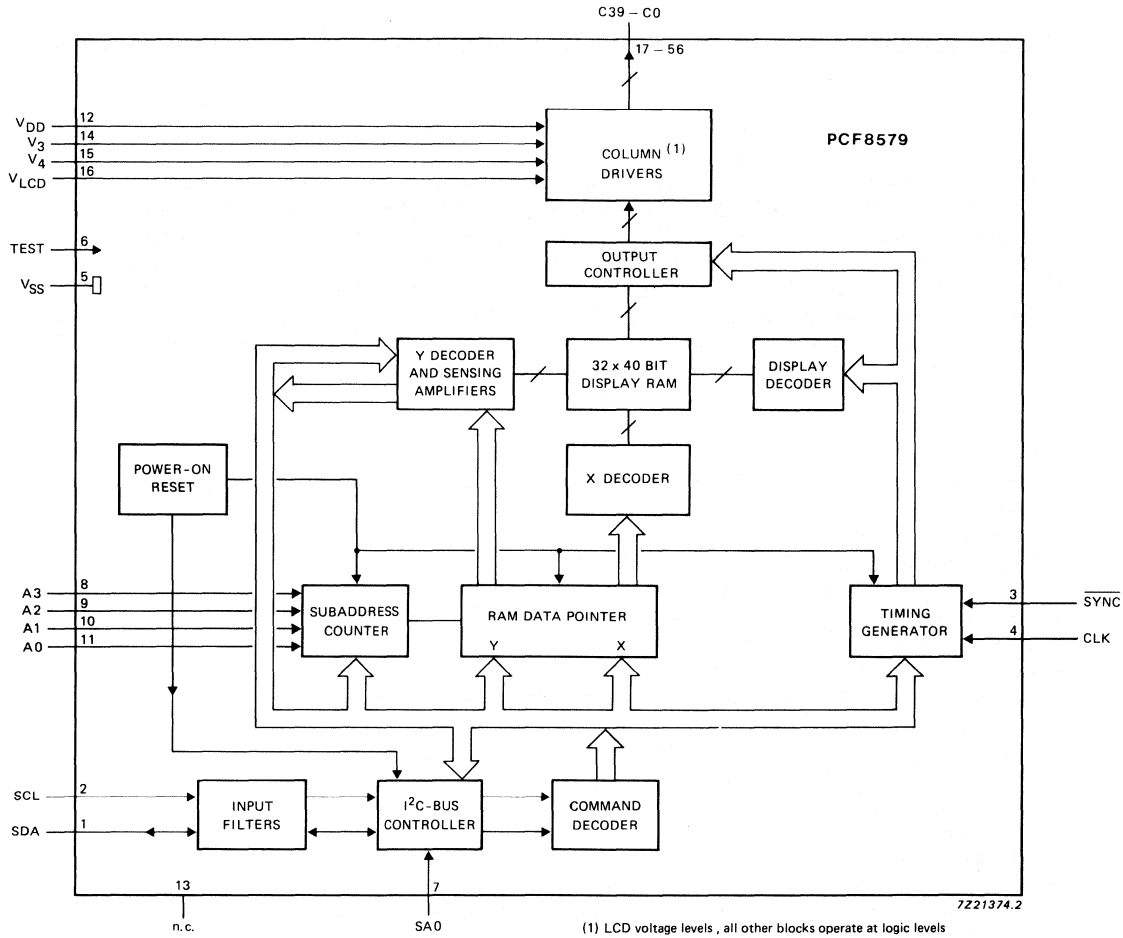


Fig.1 Block diagram.

DEVELOPMENT DATA

PINNING

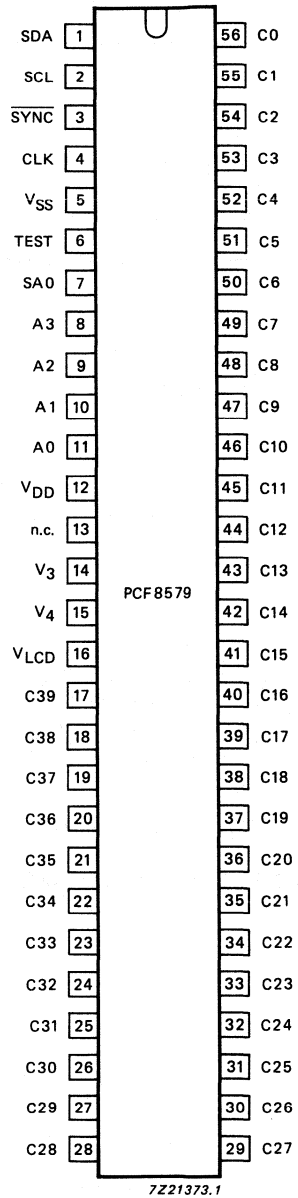
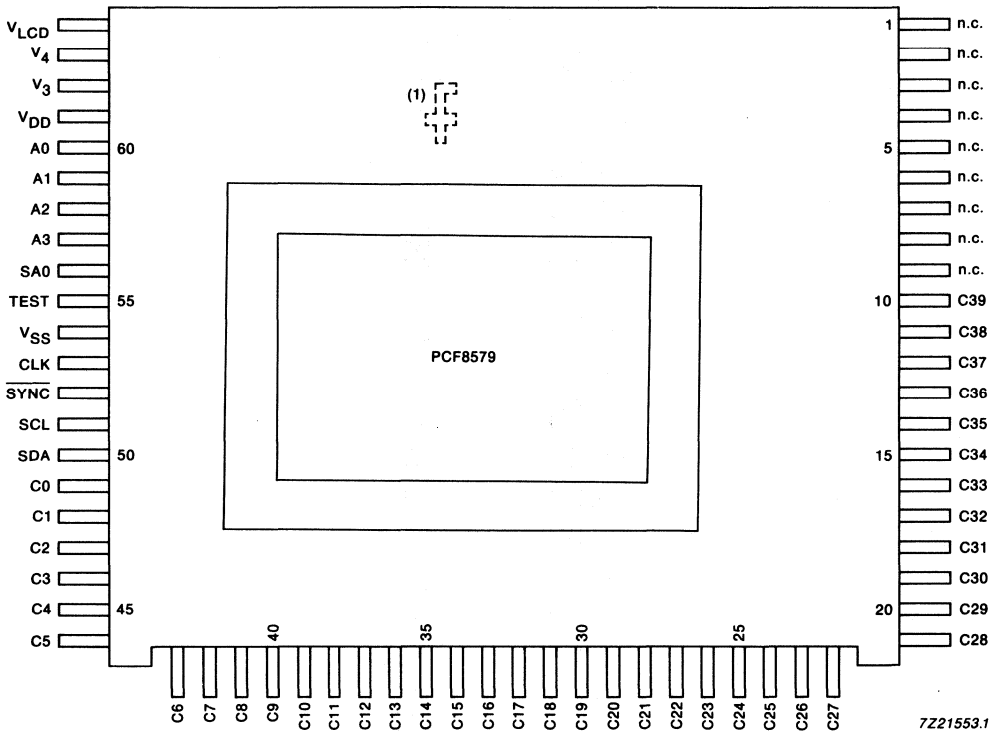


Fig.2 (a) Pinning diagram: VSO56; SOT190.

PINNING (continued)



(1) Orientation mark.

Fig.2 (b) Pinning diagram: SO122.

mnemonic	pin no.		description
	SOT190	SO122	
SDA	1	50	I^2C-bus serial data line
SCL	2	51	I^2C-bus serial clock line
$\overline{SYNC}$	3	52	cascade synchronization input
CLK	4	53	external clock input
V_{SS}	5	54	ground (logic)
TEST	6	55	test pin (connect to V_{SS})
SA0	7	56	I^2C-bus slave address input (bit 0)
A3 to A0	8 - 11	57 - 60	I^2C-bus subaddress inputs
V_{DD}	12	61	positive supply voltage
n.c.	13 *	1 - 9	not connected
V_3 to V_4	14 - 15	62 - 63	LCD bias voltage inputs
V_{LCD}	16	64	LCD supply voltage
C39 to C0	17 - 56	10 - 49	LCD column driver outputs

DEVELOPMENT DATA

* Do not connect, this pin is reserved.

FUNCTIONAL DESCRIPTION

The PCF8579 column driver is designed for use with the PCF8578. Together they form a general purpose LCD dot matrix chip set.

Typically up to 16 PCF8579s may be used with one PCF8578. Each of the PCF8579s is identified by a unique 4-bit hardware subaddress, set by pins A0 to A3. The PCF8578 can operate with up to 32 PCF8579s when using two I^2C-bus slave addresses. The two slave addresses are set by the logic level on input SA0.

Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast. Table 1 shows the optimum voltage bias levels for the PCF8578/PCF8579 chip set as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}.

Table 1 Optimum LCD bias voltages

parameter	multiplex rate			
	1:8	1:16	1:24	1:32
$\frac{V_2}{V_{op}}$	0.739	0.800	0.830	0.850
$\frac{V_3}{V_{op}}$	0.522	0.600	0.661	0.700
$\frac{V_4}{V_{op}}$	0.478	0.400	0.339	0.300
$\frac{V_5}{V_{op}}$	0.261	0.200	0.170	0.150
$\frac{V_{off(rms)}}{V_{op}}$	0.297	0.245	0.214	0.193
$\frac{V_{on(rms)}}{V_{op}}$	0.430	0.316	0.263	0.230
$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	1.447	1.291	1.230	1.196
$\frac{V_{op}}{V_{th}}$	3.37	4.08	4.68	5.19

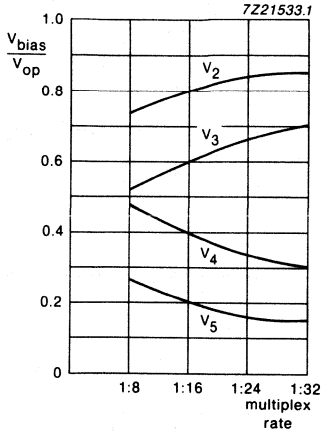


Fig.3 LCD bias voltage as a function of the multiplex rate.

DEVELOPMENT DATA

Power-on reset

At power-on the PCF8579 resets to a defined starting condition as follows.

1. Display blank (in conjunction with PCF8578)
2. 1:32 multiplex rate
3. start bank 0 selected
4. Data pointer is set to X, Y address 0, 0
5. Character mode
6. Subaddress counter is set to 0
7. I^2C-bus is initialized.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on, to allow completion of the reset action.

FUNCTIONAL DESCRIPTION (continued)

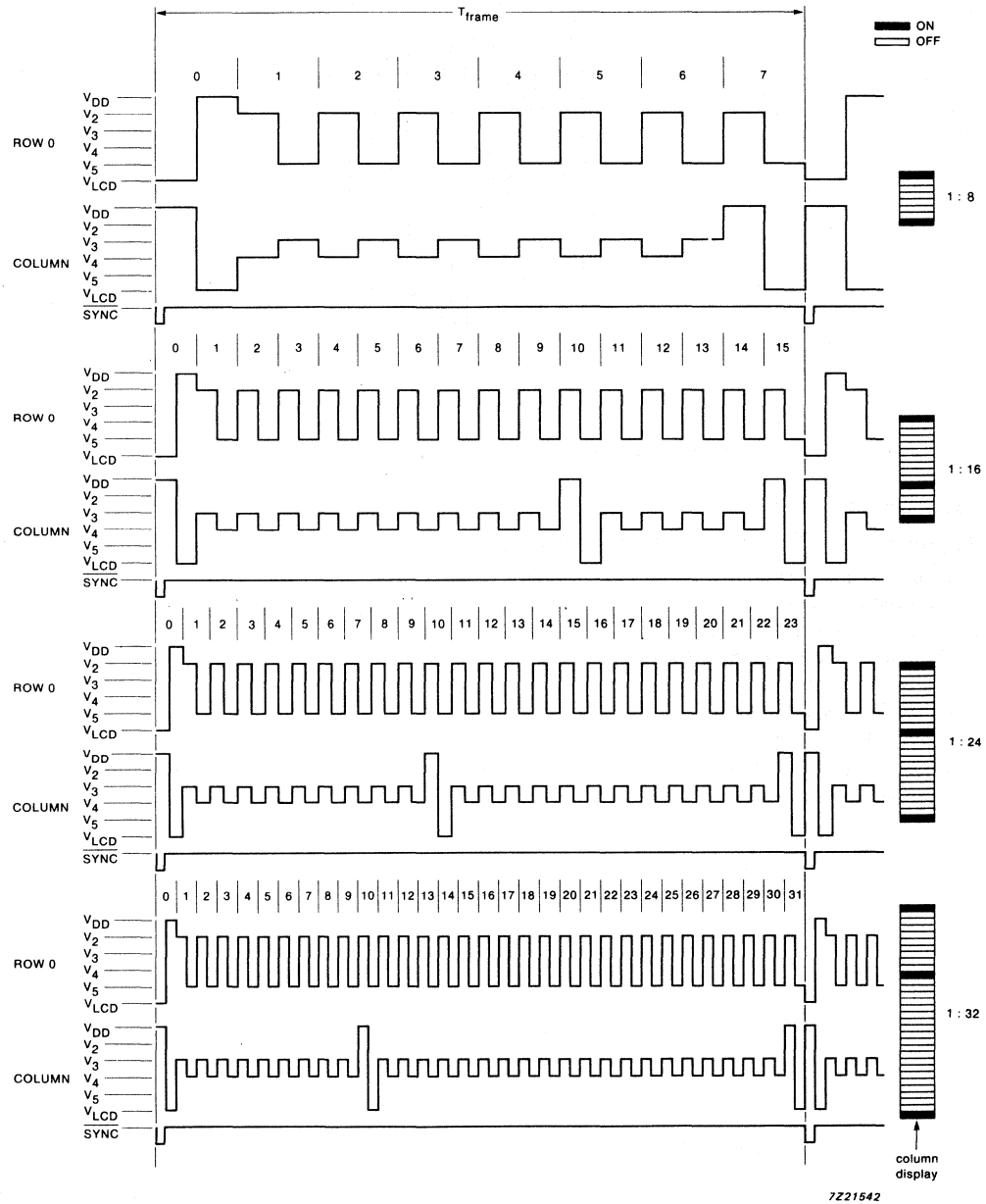
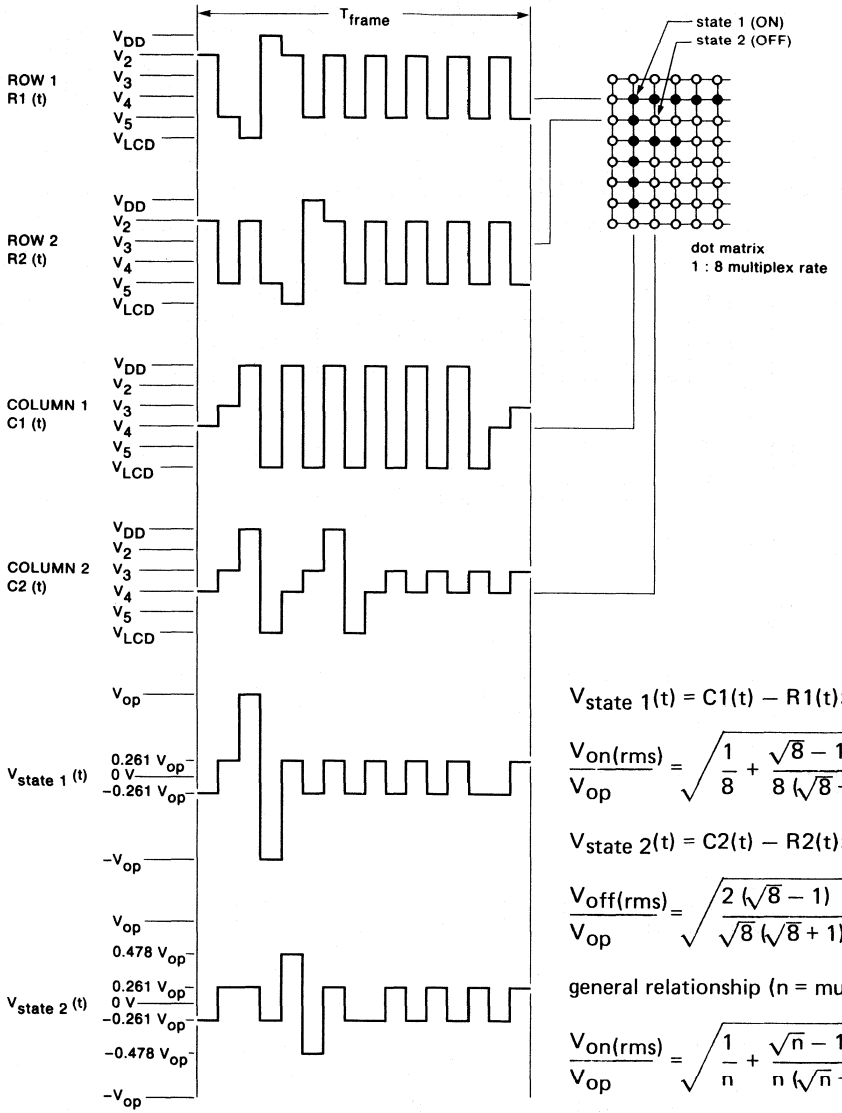


Fig.4 LCD row/column waveforms.

DEVELOPMENT DATA



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8}-1}{8(\sqrt{8}+1)}} = 0.430$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{8}-1)}{\sqrt{8}(\sqrt{8}+1)^2}} = 0.297$$

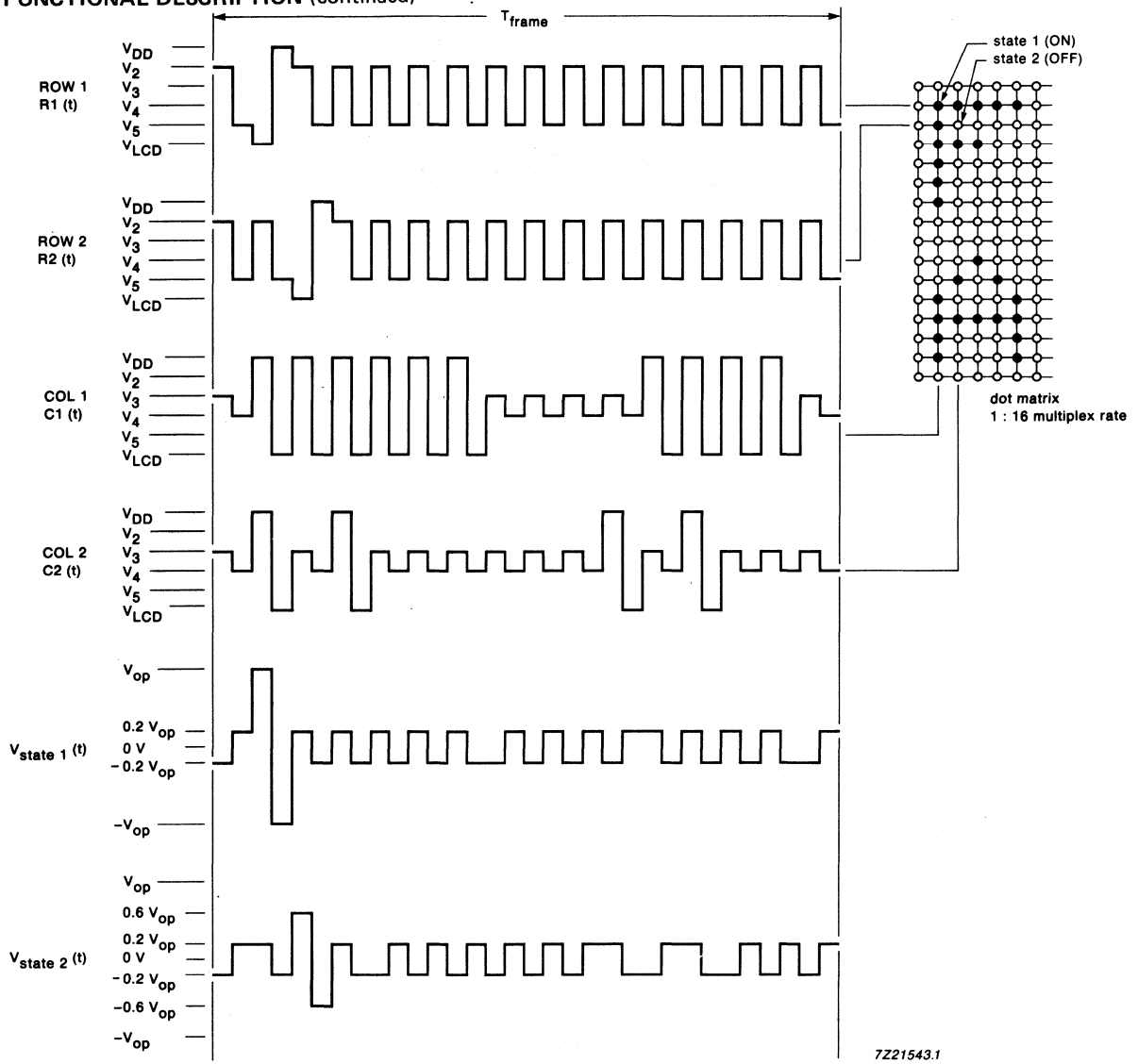
general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$$

Fig.5 LCD drive mode waveforms for 1:8 multiplex rate.

FUNCTIONAL DESCRIPTION (continued)



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16} - 1}{16\,(\sqrt{16} + 1)}} = 0.316$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{16} - 1)}{\sqrt{16}\,(\sqrt{16} + 1)^2}} = 0.245$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n} - 1}{n\,(\sqrt{n} + 1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2\,(\sqrt{n} - 1)}{\sqrt{n}\,(\sqrt{n} + 1)^2}}$$

Fig.6 LCD drive mode waveforms for 1:16 multiplex rate.

Timing generator

The timing generator of the PCF8579 organizes the internal data flow from the RAM to the display drivers. An external synchronization pulse $\overline{SYNC}$ is received from the PCF8578. This signal maintains the correct timing relationship between cascaded devices.

Column drivers

Outputs C0 to C39 are column drivers which must be connected to the LCD. Unused outputs should be left open-circuit.

Display RAM

The PCF8579 contains a 32 x 40 bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes (4 x 8 x 40 bits). During RAM access, data is transferred to/from the RAM via the I^2C-bus.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into or read from the display RAM, as specified by commands sent on the I^2C-bus.

Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage and retrival take place, only when the contents of the subaddress counter agree with the hardware subaddress at pins A0, A1, A2 and A3.

I^2C-bus controller

The I^2C-bus controller detects the I^2C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8579 acts as an I^2C-bus slave transmitter/receiver. Device selection depends on the I^2C-bus slave address, the hardware subaddress and the commands transmitted.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

FUNCTIONAL DESCRIPTION (continued)

RAM access

There are three RAM ACCESS modes:

- Character
- Half-graphic
- Full-graphic

These modes are specified by bits G1 and G0 of the RAM ACCESS command. The RAM ACCESS command controls the order in which data is written to or read from the RAM (see Fig.7).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Fig.8):

- Device subaddress (specified by the DEVICE SELECT command)
- RAM X-address (specified by the LOAD X-ADDRESS command)
- RAM bank (specified by bits Y1 and Y0 of the RAM ACCESS command)

Subsequent data bytes will be written or read according to the chosen RAM access mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.

Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD, via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M1 and M0 of the SET MODE command.

The display status (all dots on/off and normal/inverse video) is set by bits E1 and E0 of the SET MODE command. For bank switching, the RAM bank corresponding to the top of the display is set by bits B1 and B0 of the SET START BANK command. This is shown in Fig.9. This feature is useful when scrolling in alphanumeric applications.

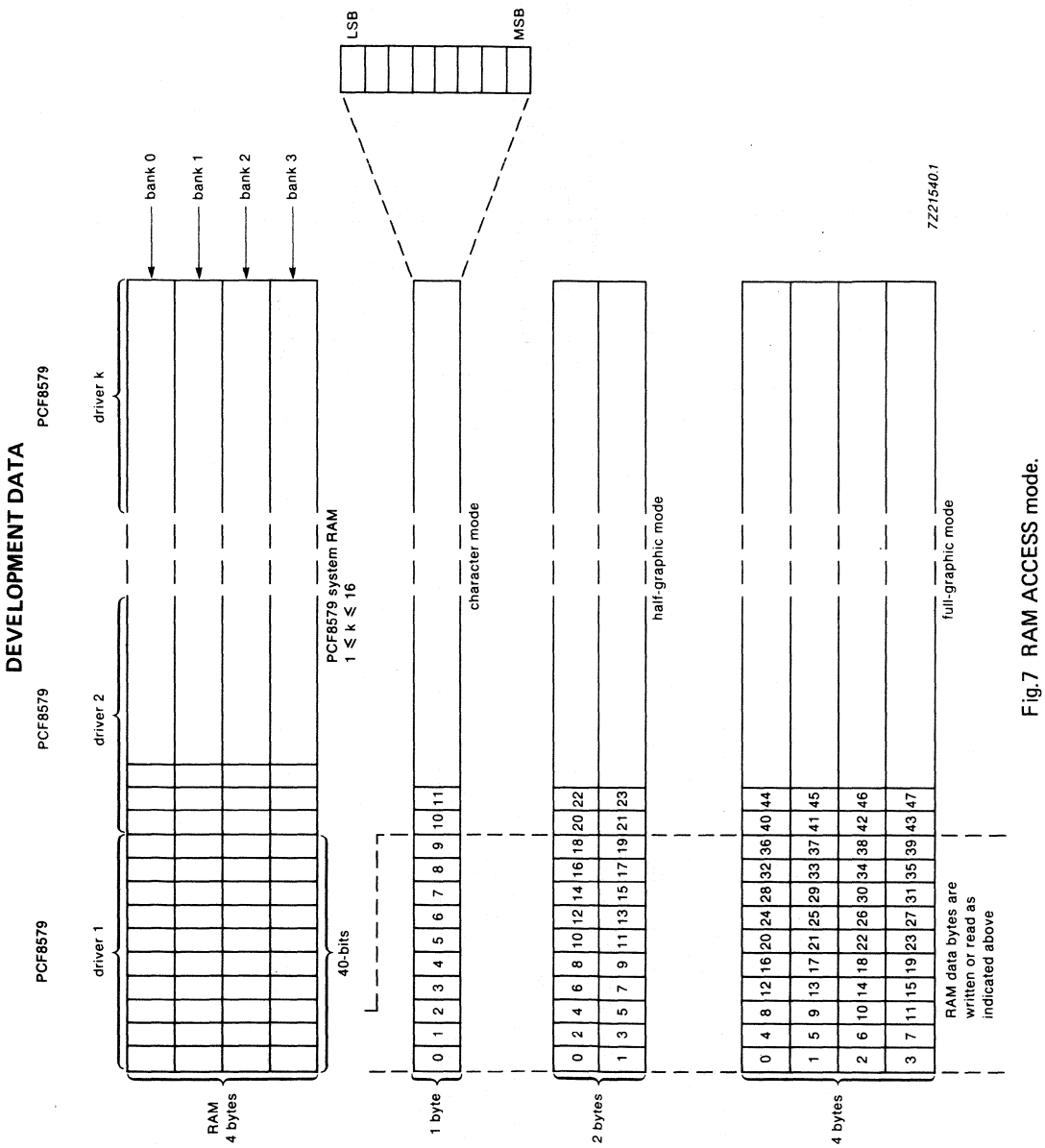


Fig.7 RAM ACCESS mode.

FUNCTIONAL DESCRIPTION (continued)

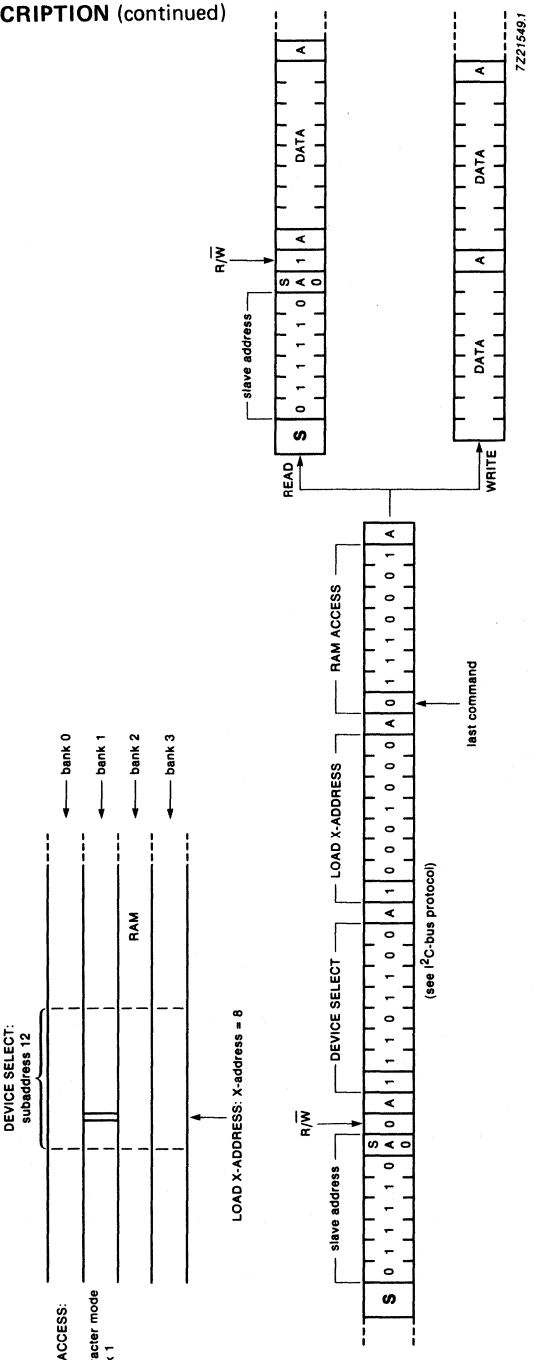


Fig.8 Example of commands specifying initial data byte RAM locations.

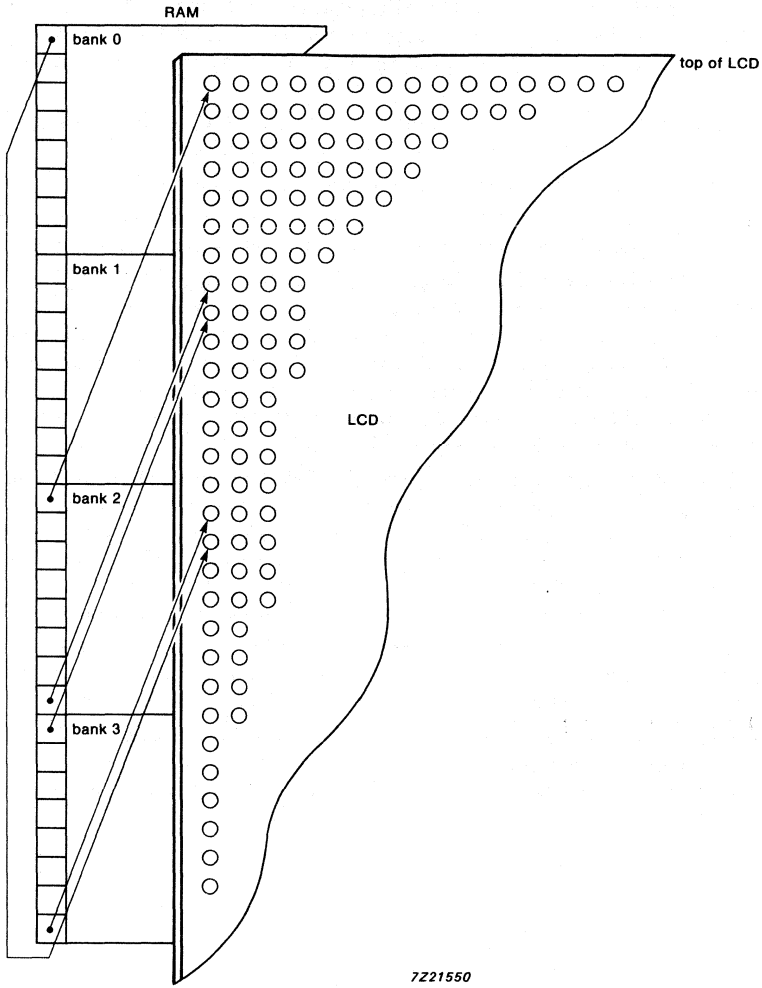


Fig.9 Relationship between display and SET START BANK; 1:32 multiplex rate and start bank = 2.

I²C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8578 and PCF8579. The least-significant bit of the slave address is set by connecting input SA0 to either 0 (V_{SS}) or 1 (V_{DD}). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I²C-bus which allows:

(a) one PCF8578 to operate with up to 32 PCF8579s on the same I²C-bus for very large applications.
(b) the use of two types of LCD multiplex schemes on the same I²C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

The I²C-bus protocol is shown in Fig. 10. All communications are initiated with a start condition (S) from the I²C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I²C-bus master issues a stop condition (P).

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8579 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by **not** generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a stop condition (P).

Display bytes are written into, or read from, the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from, the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8579s (A0, A1, A2 and A3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated with an unique hardware subaddress.

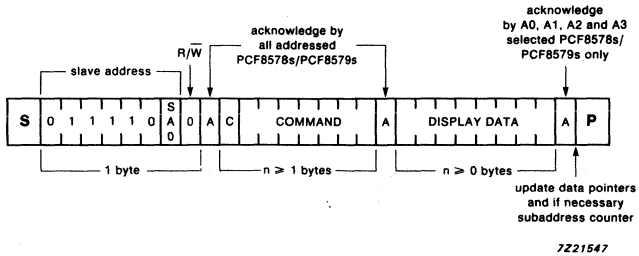


Fig.10(a) Master transmits to slave receiver (WRITE mode).

DEVELOPMENT DATA

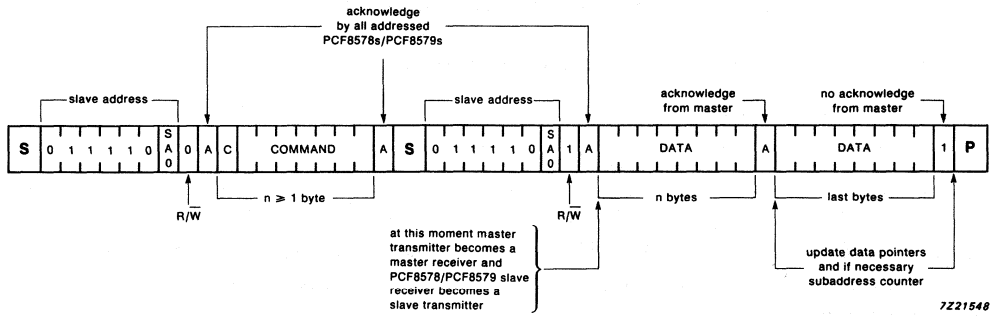


Fig.10(b) Master reads after sending command string (WRITE commands; READ data).

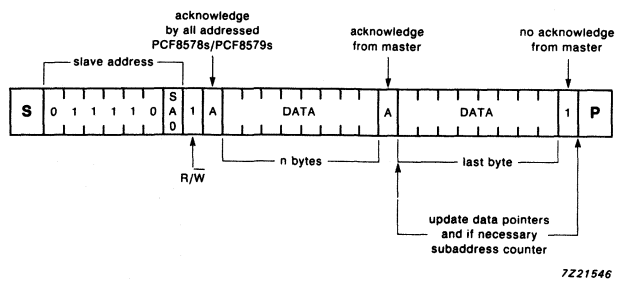
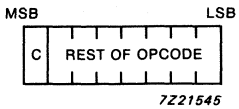


Fig.10(c) Master reads-slave immediately after sending slave address (READ mode).

I²C-BUS PROTOCOL (continued)

Command decoder

The command decoder indentifies command bytes that arrive on the I²C-bus. The most-significant bit of a command is the continuation bit C (see Fig.11). When this bit is set, it indicates that the next byte to be transferred will be a command. If the bit is reset, it indicates the conclusion of the command transfer. Further bytes will be regarded as display data. Commands are transferred in WRITE mode only.



C = 0; last command
C = 1; commands continue

Fig.11 General format of command byte.

The five commands available to the PCF8579 are defined in Table 2.

Table 2 Summary of commands

code	command	description
C 0 D D D D D D	LOAD X-ADDRESS	0 to 39
C 1 0 D D D D D	SET MODE	multiplex rate, display status, system type
C 1 1 0 D D D D	DEVICE SELECT	defines device subaddress
C 1 1 1 D D D D	RAM ACCESS	graphic modes, bank select (D D D D ⩾ 12 is not allowed; see SET START BANK opcode)
C 1 1 1 1 1 D D	SET START BANK	defines bank at top of LCD

Where:

C = command continuation bit
D = may be a logic 1 or 0.

DEVELOPMENT DATA

Table 3 Definition of PCF8578/PCF8579 commands

command / opcode	options	description
SET MODE C 1 0 T E1 E0 M1 M0	LCD drive mode bits M1 M0 1:8 MUX (8 rows) 0 1 1:16 MUX (16 rows) 1 0 1:24 MUX (24 rows) 1 1 1:32 MUX (32 rows) 0 0	defines LCD drive mode
	display status bits E1 E0 blank 0 0 normal 0 1 all segments on 1 0 inverse video 1 1	defines display status
	system type bit T PCF8578 row only 0 PCF8578 mixed mode 1	defines system type
SET START BANK C 1 1 1 1 1 B1 B0	start bank pointer bits B1 B0 bank 0 0 0 bank 1 0 1 bank 2 1 0 bank 3 1 1	defines pointer to RAM bank corresponding to the top of the LCD. Useful for scrolling, pseudo-motion and background preparation of new display
DEVICE SELECT C 1 1 0 A3 A2 A1 A0	bits A3 A2 A1 A0 4-bit binary value of 0 to 15	four bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of sixteen hardware subaddresses

I²C BUS PROTOCOL (continued)

Table 3 (continued)

command / opcode	options	description
RAM ACCESS C 1 1 1 G1 G0 Y1 Y0	RAM access mode bits G1 G0 character 0 0 half graphic 0 1 full graphic 1 0 not allowed* 1 1	defines the auto-increment behaviour of the address for RAM access
	bits Y1 Y0 2-bit binary value of 0 to 3	two bits of immediate data, bits Y0 to Y1, are transferred to the Y-address pointer to define one of four banks for RAM access
LOAD X-ADDRESS C 0 X5 X4 X3 X2 X1 X0	bits X5 X4 X3 X2 X1 X0 6-bit binary value of 0 to 39	six bits of immediate data, bits X0 to X5, are transferred to the X-address pointer to define one of forty display RAM columns

* See opcode for SET START BANK.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

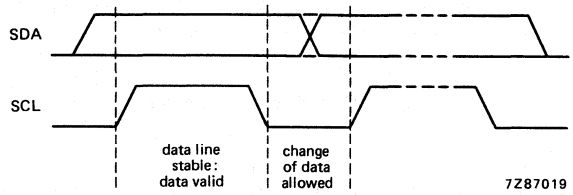


Fig.12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

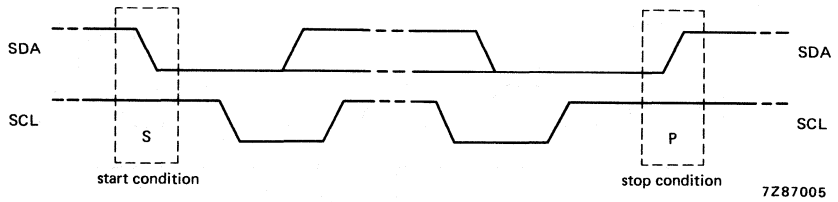


Fig.13 Definition of start and stop condition.

CHARACTERISTICS OF THE I²C-BUS (continued)

System configuration

A device transmitting a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message flow is the "master" and the devices which are controlled by the master are the "slaves".

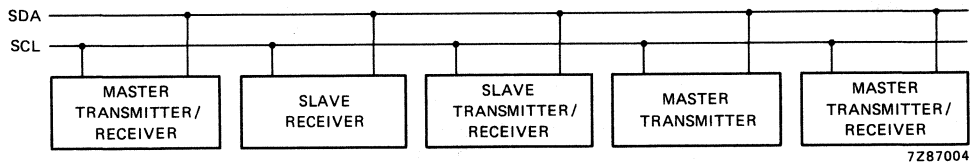


Fig.14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

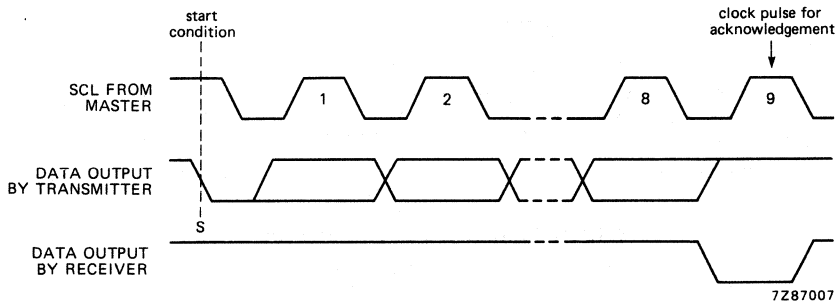


Fig.15 Acknowledgement on the I²C-bus.

Note

The general characteristics and detailed specification of the I²C-bus is available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	+8.0	V
LCD supply voltage range	V_{LCD}	V_{DD} −11	V_{DD}	V
Input voltage range at				
SDA, SCL, $\overline{SYNC}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_{I1}	V_{SS} −0.5	V_{DD} + 0.5	V
V_3 to V_4	V_{I2}	V_{LCD} −0.5	V_{DD} + 0.5	V
Output voltage range at				
SDA	V_{O1}	V_{SS} −0.5	V_{DD} + 0.5	V
C0 to C39	V_{O2}	V_{LCD} −0.5	V_{DD} + 0.5	V
DC input current	I_I	−10	10	mA
DC output current	I_O	−10	10	mA
V_{DD}, V_{SS} or V_{LCD} current	I_{DD}, I_{SS}, I_{LCD}	−50	50	mA
Power dissipation per package	P_{tot}	−	400	mW
Power dissipation per output	P_o	−	100	mW
Storage temperature range	T_{stg}	−65	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{DD} = 2.5 V to 6.0 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage		V_{DD}	2.5	–	6.0	V
LCD supply voltage		V_{LCD}	V_{DD} −9	–	V_{DD} −3.5	V
Supply current	note 1; f_{CLK} = 2 kHz	I_{DD1}	–	9	20	μA
Power-on reset level	note 2	V_{POR}	–	1.3	1.8	V
Logic						
Input voltage LOW		V_{IL}	V_{SS}	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Leakage current at SDA, SCL, $\overline{SYNC}$, CLK, TEST, SA0, A0, A1, A2 and A3	V_I = V_{DD} or V_{SS}	I_{L1}	−1	–	1	μA
SDA output current LOW	V_{OL} = 0.4 V; V_{DD} = 5 V	I_{OL}	3	–	–	mA
Input capacitance	note 3	C_I	–	–	5	pF
LCD outputs						
Leakage current at V_3 to V_4	V_I = V_{DD} or V_{LCD}	I_{L2}	−2	–	2	μA
DC component of LCD drivers C0 to C39		± V_{DC}	–	20	–	mV
Output resistance at C0 to C39	note 4	R_{COL}	–	3	6	kΩ

DEVELOPMENT DATA

AC CHARACTERISTICS (note 5)

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} −3.5 V to V_{DD} −9 V; T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Clock frequency	50% duty factor	f_{CLK}	–	*	10	kHz
Driver delays	$V_{DD} - V_{LCD}$ = 9 V; with test loads	t_{PLCD}	–	–	100	μs
I²C-bus						
SCL clock frequency		f_{SCL}	–	–	100	kHz
Tolerable spike width on bus		t_{SW}	–	–	100	ns
Bus free time		t_{BUF}	4.7	–	–	μs
Start condition set-up time	repeated start codes only	$t_{SU;STA}$	4.7	–	–	μs
Start condition hold time		$t_{HD;STA}$	4.0	–	–	μs
SCL LOW time		t_{LOW}	4.7	–	–	μs
SCL HIGH time		t_{HIGH}	4.0	–	–	μs
SCL and SDA rise time		t_r	–	–	1.0	μs
SCL and SDA fall time		t_f	–	–	0.3	μs
Data set-up time		$t_{SU;DAT}$	250	–	–	ns
Data hold time		$t_{HD;DAT}$	0	–	–	ns
Stop condition set-up time		$t_{SU;STO}$	4.0	–	–	μs

* Typically 0.9 to 3.3 kHz.

Notes to the characteristics

1. Outputs are open; inputs at V_{DD} or V_{SS}; I^2C-bus inactive; clock with 50% duty cycle.
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (C0 to C39) and bias input (V_3 to V_4, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 1):

   $V_{OP} = V_{DD} - V_{LCD} = 9$ V;

   $V_3 - V_{LCD} \geqslant 4.70$ V; $V_4 - V_{LCD} \leqslant 4.30$ V; $I_{LOAD} = 100\ \mu$A.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

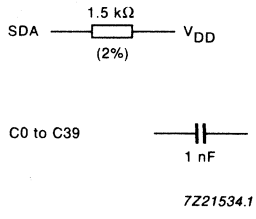


Fig.16 Test loads.

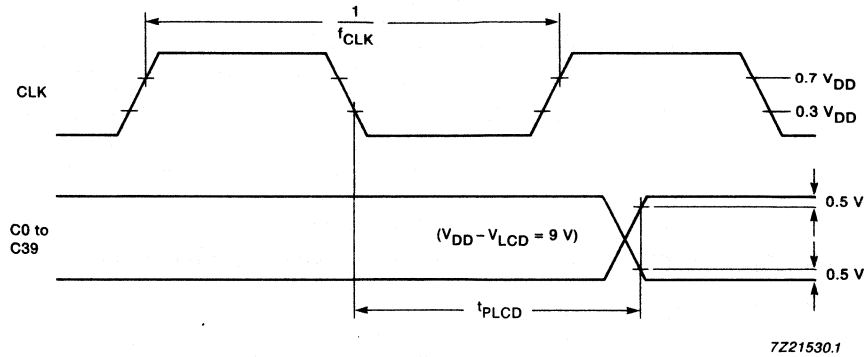


Fig.17 Driver timing waveforms.

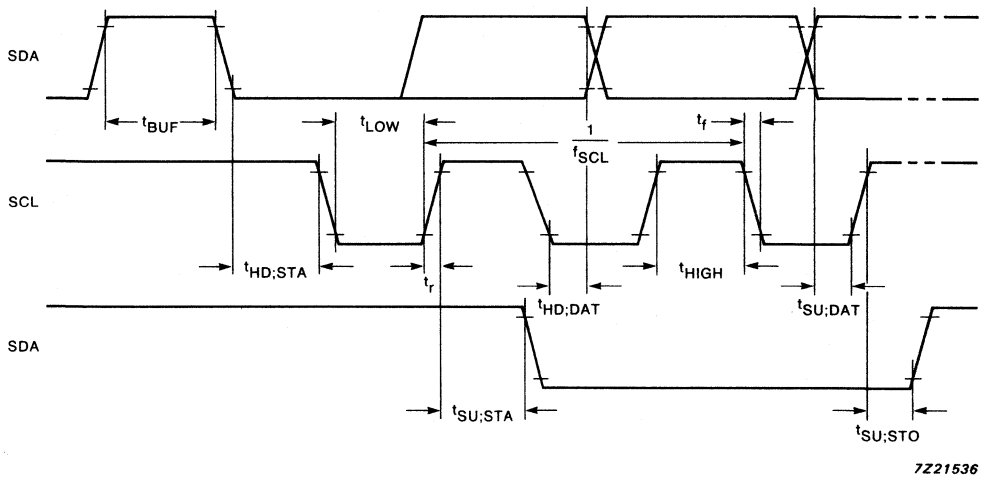


Fig.18 I^2C-bus timing waveforms.

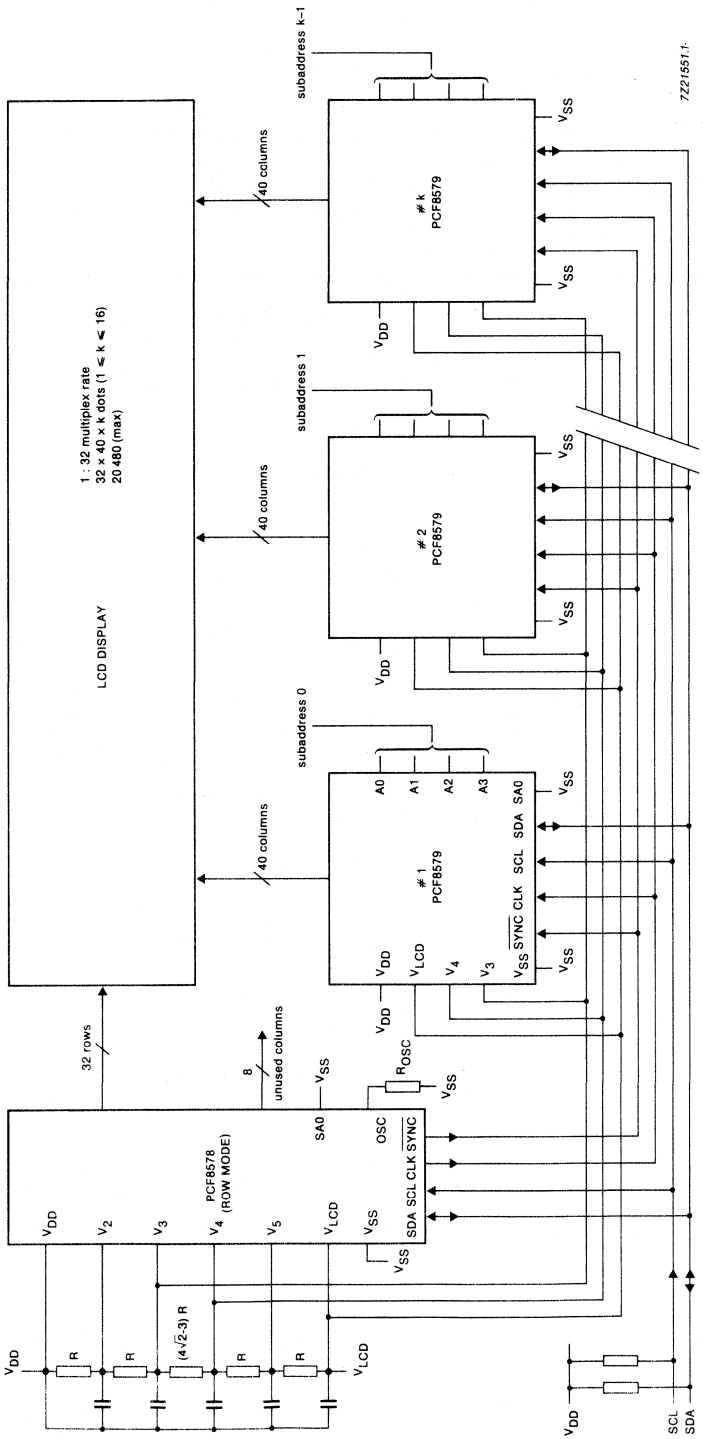


Fig.19 Typical LCD driver system with 1:32 multiplex rate.

DEVELOPMENT DATA

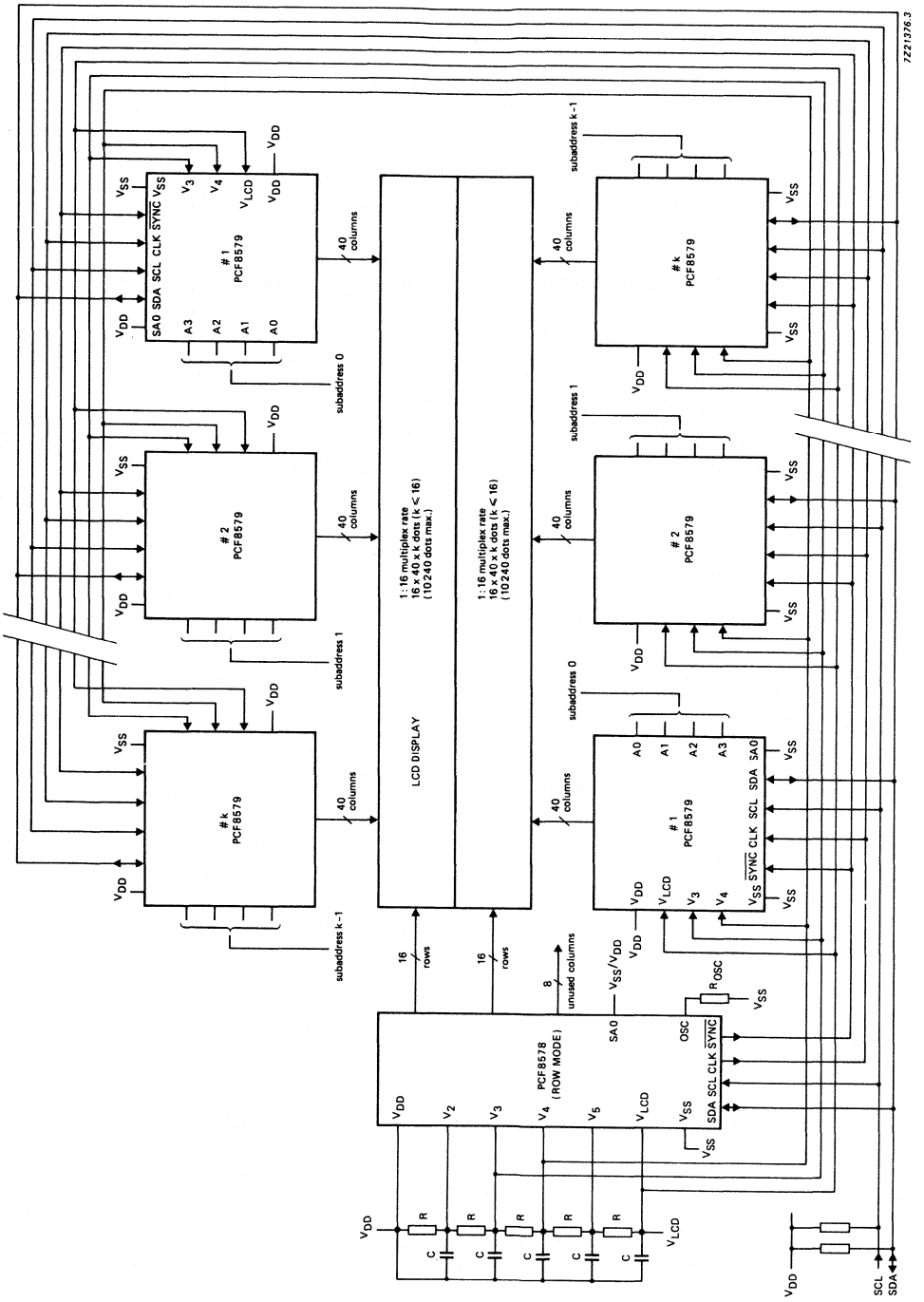


Fig.20 Split screen application with 1:16 multiplex rate for improved contrast.

APPLICATION INFORMATION (continued)

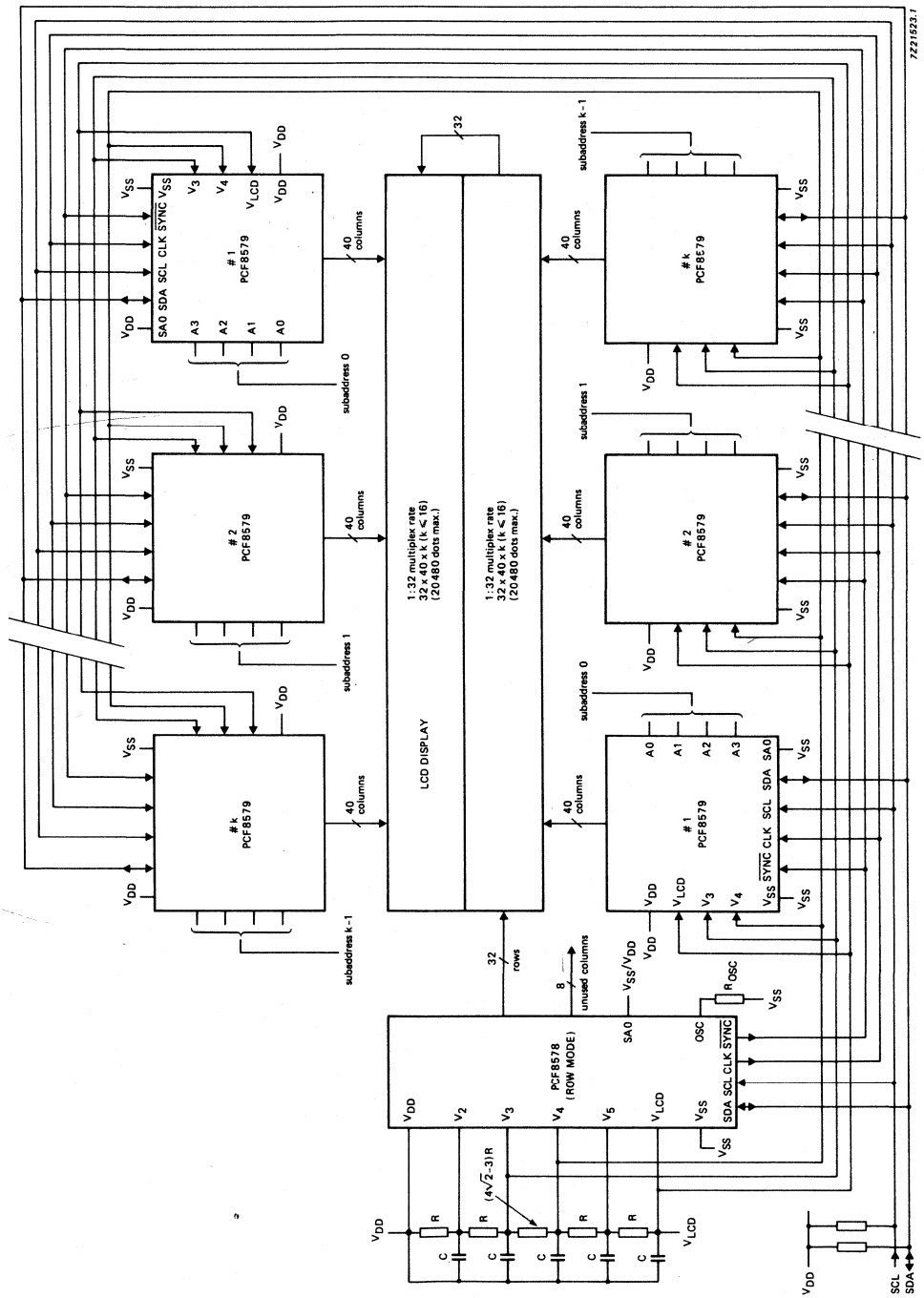


Fig.21 Split screen application using double screen with 1:32 multiplex rate.

DEVELOPMENT DATA

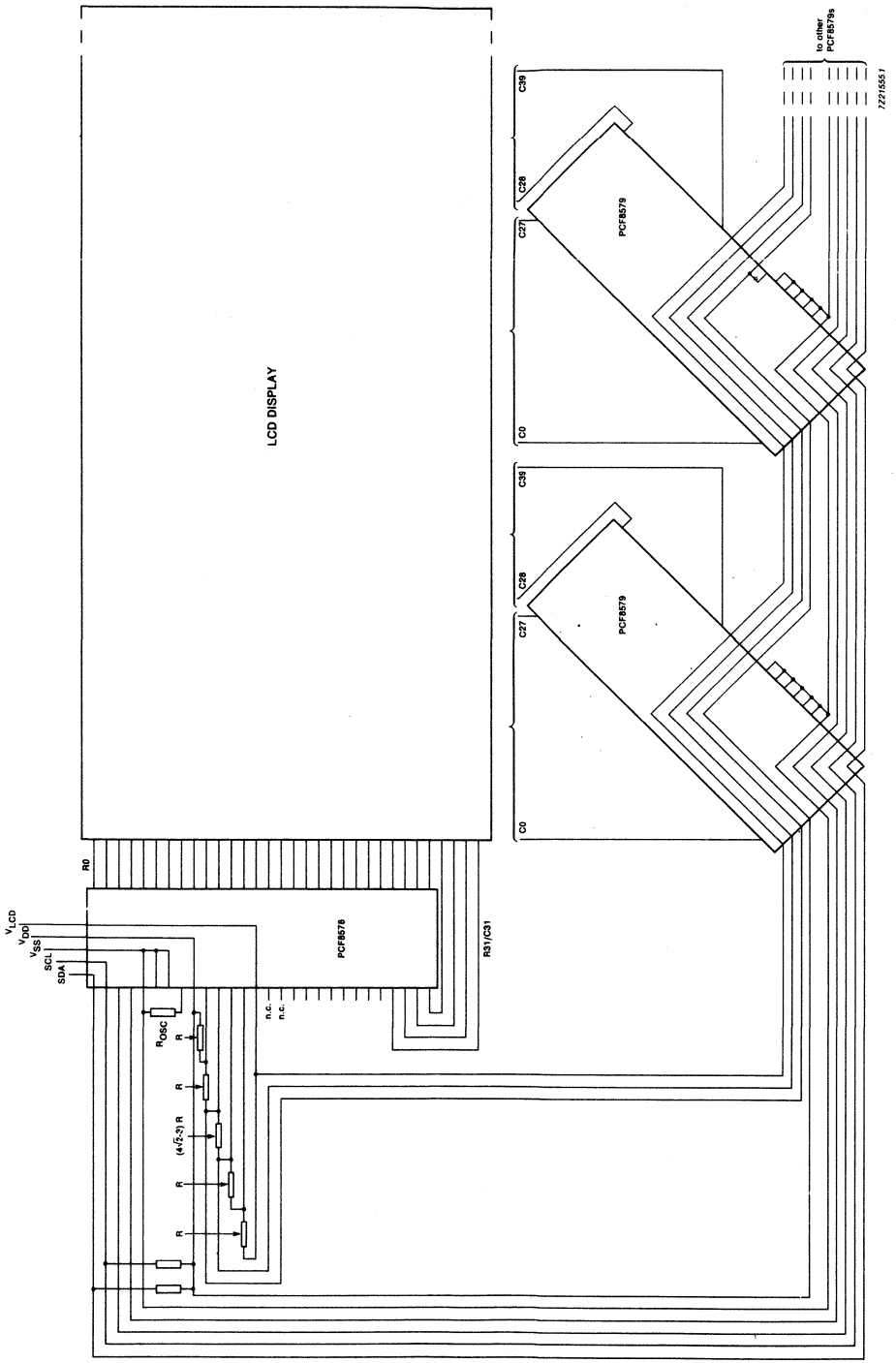
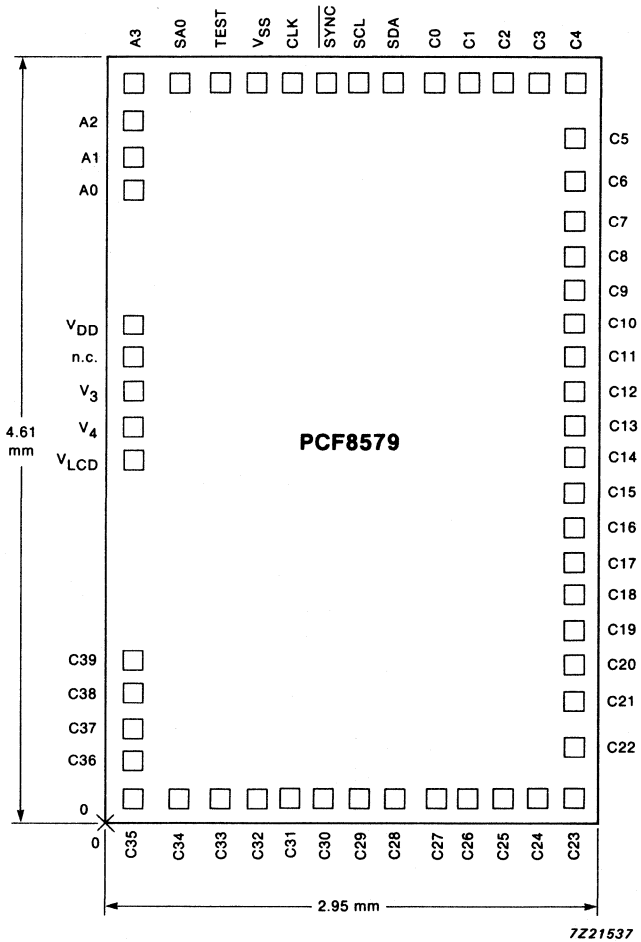


Fig.22 Example of single plane wiring, single screen with 1:32 multiplex rate (PCF8578 in row driver mode).

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 13.6 mm^2
Bonding pad dimensions: 120 μm x 120 μm

Fig.23 Bonding pad locations.

Table 4 Bonding pad locations (dimensions in μm)

All x/y co-ordinates are referenced to the bottom left corner, see Fig.23.

pad	X	Y	pad	X	Y
SDA	1726	4444	C27	1972	160
SCL	1522	4444	C26	2176	160
$\overline{SYNC}$	1318	4444	C25	2380	160
CLK	1114	4444	C24	2584	160
V_{SS}	910	4444	C23	2788	160
TEST	688	4444	C22	2788	472
SA0	442	4444	C21	2788	736
A3	160	4444	C20	2788	976
A2	160	4222	C19	2788	1180
A1	160	4018	C18	2788	1384
A0	160	3814	C17	2788	1588
V_{DD}	160	3010	C16	2788	1792
n.c.	160	2806	C15	2788	1996
V_2	160	2602	C14	2788	2200
V_3	160	2398	C13	2788	2404
V_{LCD}	160	2194	C12	2788	2608
C39	160	994	C11	2788	2812
C38	160	790	C10	2788	3016
C37	160	586	C9	2788	3220
C36	160	382	C8	2788	3424
C35	160	160	C7	2788	3628
C34	442	160	C6	2788	3868
C33	688	160	C5	2788	4132
C32	910	160	C4	2788	4444
C31	1114	160	C3	2584	4444
C30	1318	160	C2	2380	4444
C29	1522	160	C1	2176	4444
C28	1726	160	C0	1972	4444

DEVELOPMENT DATA

CHIP-ON GLASS INFORMATION

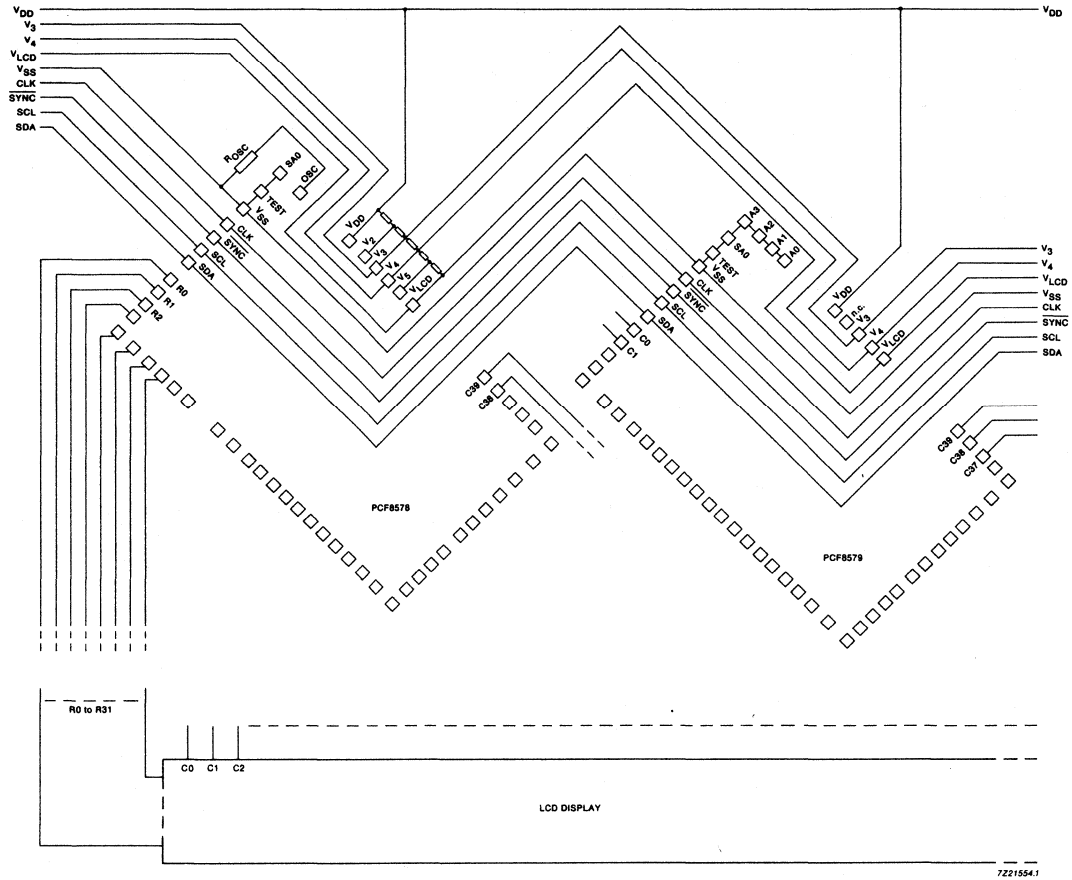


Fig.24 Typical chip-on glass application (viewed from underside of chip).

Note to Fig.24

If inputs SA0 and A0 to A3 are left unconnected they are internally pulled-up to V_{DD}.

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